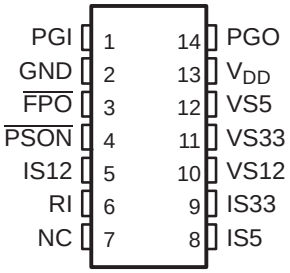
PC POWER SUPPLY SUPERVISOR

Check for Samples: TPS3513

FEATURES

- **Overvoltage Protection and Lockout for 12 V, 5 V, and 3.3 V**
- **Overcurrent Protection and Lockout for 12 V, 5 V, and 3.3 V**
- **Undervoltage Protection and Lockout for 12 V, and Undervoltage Detect for 5 V and 3.3 V**
- **Fault-Protection Output With Open Drain Output Stage**
- **Open-Drain, Power Good Output Signal for Power-Good Input, 3.3 V and 5 V**
- **300-ms Power-Good Delay**
- **75-ms Delay for 5-V and 3.3-V Power Supply Short-Circuit Turnon Protection**
- **2.3 ms $\overline{\text{PSON}}$ Control to $\overline{\text{FPO}}$ Turnoff Delay**
- **38 ms $\overline{\text{PSON}}$ Control Debounce**
- **Wide Supply Voltage Range From 4.5 V to 15 V**

D OR N PACKAGE
(TOP VIEW)

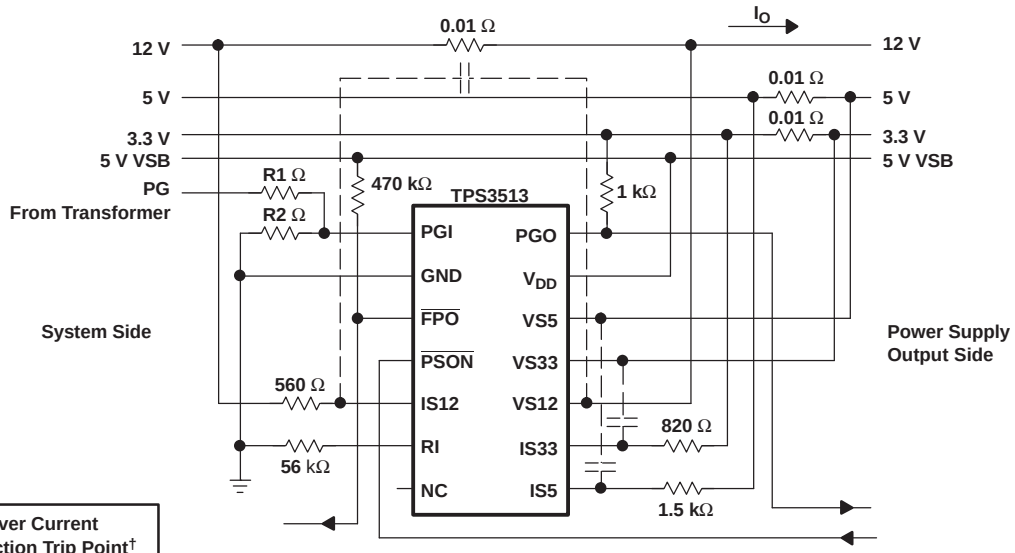


NC – No internal connection

DESCRIPTION

The TPS3513 is designed to optimize PC switching power supply system with minimum external components. It provides undervoltage lockout (UVLO), protection circuits, power good indicator, and on/off control.

TYPICAL APPLICATION



	Max Output Current	Over Current Protection Trip Point†
12 V	6 A	9.2 A
5 V	16 A	24.6 A
3.3 v	9 A	13.5 A

† Over current protection trip point can be programmable.

This integrated circuit can be damaged by ESD. Texas Instruments recommends that all integrated circuits be handled with appropriate precautions. Failure to observe proper handling and installation procedures can cause damage.

ESD damage can range from subtle performance degradation to complete device failure. Precision integrated circuits may be more susceptible to damage because very small parametric changes could cause the device not to meet its published specifications.

DESCRIPTION (CONTINUED)

UVLO thresholds are 4.45 V (on) and 3.65 V (off). Overcurrent protection (OCP) and overvoltage protection (OVP) monitor 3.3 V, 5 V, and 12 V. When an OC or OV condition is detected, the power-good output (PGO) is asserted low and the fault protection output ($\overline{FPO}$) is latched high. $\overline{PSON}$ from low-to-high resets the latch. The OCP function will be enabled 75 ms after $\overline{PSON}$ goes low, and a debounce of typically 38 ms. A built-in 2.3-ms delay with 38-ms debounce from $\overline{PSON}$ to $\overline{FPO}$ output is enabled at turnoff.

An external resistor is connected between the RI pin and the GND pin. This will introduce an accurate $I_{(ref)}$ for OCP function. The $I_{(ref)}$ range is from 12.5 µA to 62.5 µA. The formula for choosing RI resistor is $V_{(RI)}/I_{(ref)}$. Three OCP comparators and the $I_{(ref)}$ section are supplied by VS12. The current draw from the VS12 pin is less than 1 mA.

The power good feature monitors PGI, 3.3 V and 5 V, and issues a power good signal when the output is ready.

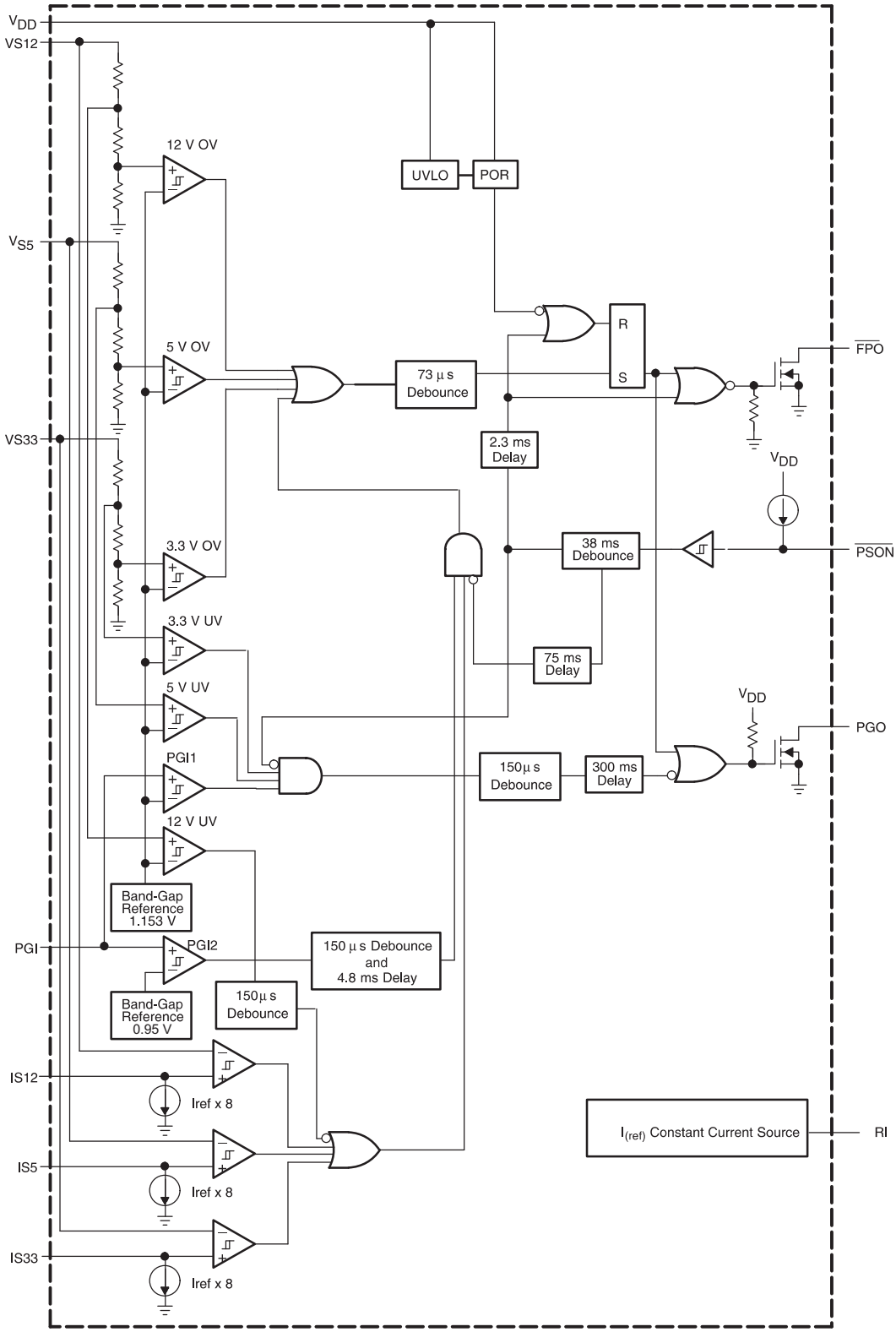
The TPS3513 is characterized for operation from –40°C to 85°C.

Table 1. FUNCTION TABLE(1)

PGI	$\overline{PSON}$	UV CONDITION 3.3 V / 5 V	OV CONDITIONS	UV CONDITION 12 V OC Conditions	$\overline{FPO}$	PGO
< 0.9 V	L	No	No	No	L	L
< 0.9 V	L	No	No	Yes	L	L
< 0.9 V	L	No	Yes	No	H	L
< 0.9 V	L	No	Yes	Yes	H	L
< 0.9 V	L	Yes	No	No	L	L
< 0.9 V	L	Yes	No	Yes	L	L
< 0.9 V	L	Yes	Yes	No	H	L
< 0.9 V	L	Yes	Yes	Yes	H	L
1.0 V < PGI < 1.1 V	L	No	No	No	L	L
1.0 V < PGI < 1.1 V	L	No	No	Yes	H	L
1.0 V < PGI < 1.1 V	L	No	Yes	No	H	L
1.0 V < PGI < 1.1 V	L	No	Yes	Yes	H	L
1.0 V < PGI < 1.1 V	L	Yes	No	No	L	L
1.0 V < PGI < 1.1 V	L	Yes	No	Yes	H	L
1.0 V < PGI < 1.1 V	L	Yes	Yes	No	H	L
1.0 V < PGI < 1.1 V	L	Yes	Yes	Yes	H	L
>1.2 V	L	No	No	No	L	H
>1.2 V	L	No	No	Yes	H	L
>1.2 V	L	No	Yes	No	H	L
>1.2 V	L	No	Yes	Yes	H	L
>1.2 V	L	Yes	No	No	L	L
>1.2 V	L	Yes	No	Yes	H	L
>1.2 V	L	Yes	Yes	No	H	L
>1.2 V	L	Yes	Yes	Yes	H	L
x	H	x	x	x	H	L

(1) x = don't care, $\overline{FPO}$ = L means: fault is not latched, $\overline{FPO}$ = H means: fault is latched, PGO = L means: fault, PGO = H means: No fault

SCHEMATIC


VDD
VS12
VS5
VS33
PGI
IS12
IS5
IS33
12 V OV
5 V OV
3.3 V OV
3.3 V UV
5 V UV
PGI1
12 V UV
PGI2
Band-Gap Reference 1.153 V
Band-Gap Reference 0.95 V
Iref x 8
Iref x 8
Iref x 8
UVLO
POR
R
S
73 µs Debounce
2.3 ms Delay
38 ms Debounce
75 ms Delay
150µs Debounce
300 ms Delay
150 µs Debounce and 4.8 ms Delay
150µs Debounce
FPO
PSON
PGO
VDD
VDD
VDD
I(ref) Constant Current Source
RI

TIMING REQUIREMENTS

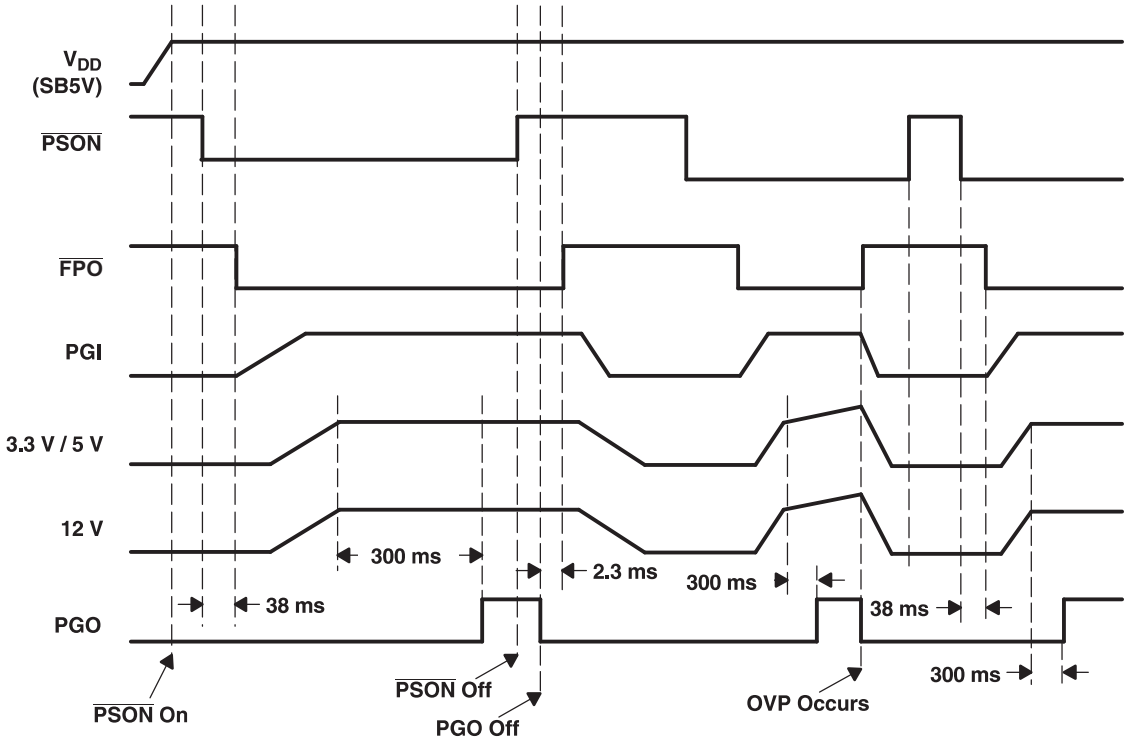


Figure 1. AC Turnon and Overvoltage Protect

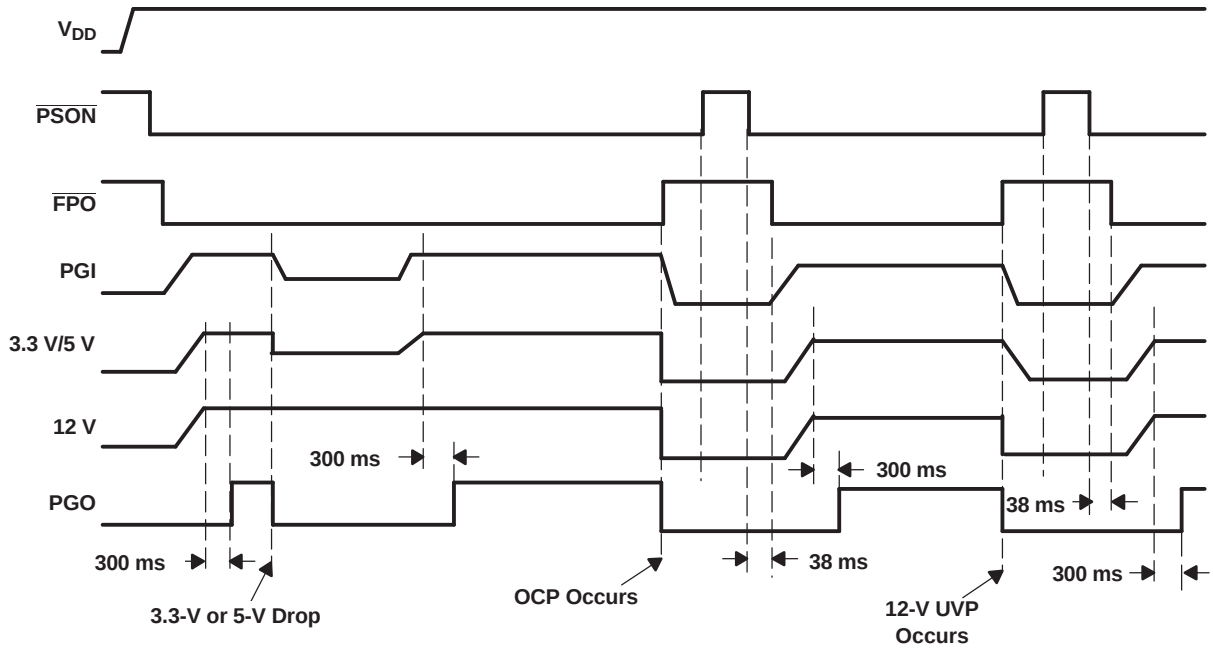


Figure 2. Overcurrent and Undervoltage Detect/Protect

Terminal Functions

TERMINAL NAME	TERMINAL NO.	I/O	DESCRIPTION
$\overline{FPO}$	3	O	Inverted fault protection output, open-drain, output stage. A low level indicates that the fault is not latched, while floating indicates that the fault is latched.
GND	2		Ground
IS12	5	I	12-V overcurrent protection
IS5	8	I	5-V overcurrent protection
IS33	9	I	3.3-V overcurrent protection
NC	7		No internal connection
PGI	1	I	Power-good input. A low level indicates that power is not good, while a high (>1.2V) indicates that power is good.
PGO	14	O	Power-good output, open drain output stage. A low level indicates that power is not good, while floating indicates that power is good.
$\overline{PSON}$	4	I	On/off control. Pull low to enable the PC Power Supply; float to disable it.
RI	6	I	Current sense setting
V_{DD}	13	I	Supply voltage
VS12	10	I	12-V overvoltage/undervoltage protection
VS33	11	I	3.3-V overvoltage protect/undervoltage detect
VS5	12	I	5-V overvoltage protect/undervoltage detect

DETAILED DESCRIPTION

Power-Good and Power-Good Delay

A PC power supply is commonly designed to provide a power-good signal, which is defined by the computer manufacturers. PGO is a power-good signal and should be asserted high by the PC power supply to indicate that the 5-VDC and 3.3-VDC outputs are above the undervoltage threshold limit. At this time the converter should be able to provide enough power to assure continuous operation within the specification. Conversely, when either the 5-VDC or the 3.3-VDC output voltages fall below the undervoltage threshold, or when main power has been removed for a sufficiently long time so that power supply operation is no longer assured, PGO should be deasserted to a low state.

The power-good (PGO), DC enable ($\overline{PSON}$), and the 5-V/3.3-V supply rails are shown in Figure 3.

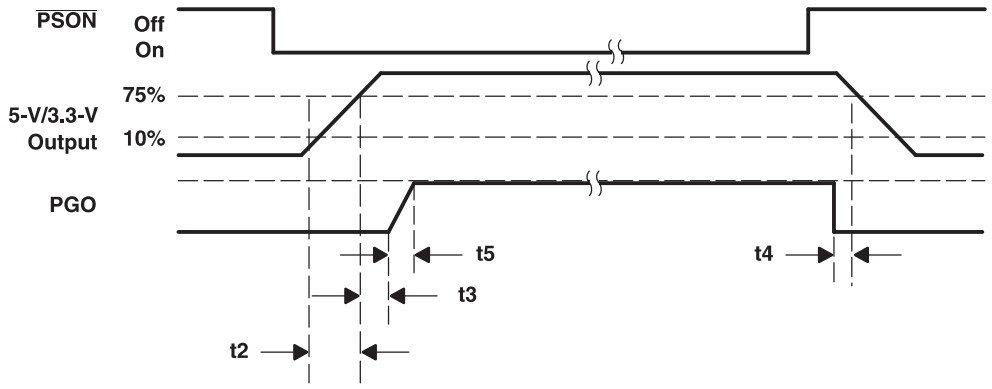


Figure 3. Timing of $\overline{PSON}$ and PGO

Although there is no requirement to meet specific timing parameters, the following signal timings are recommended:

2 ms ≤ t2 ≤ 20 ms, 100 ms < t3 < 2000 ms, t4 > 1 ms, t5 ≤ 10 ms

Furthermore, motherboards should be designed to comply with the above recommended timing. If timings other than these are implemented or required, this information should be clearly specified.

The TPS3513 family of power-supply supervisors provides a power-good output (PGO) for the 3.3-V and 5-V supply voltage rails and a separate power-good input (PGI). An internal timer is used to generate a 300-ms power-good delay.

If the voltage signals at PGI, VS33, and VS5 rise above the undervoltage threshold, the open-drain, power-good output (PGO) will go high after a delay of 300 ms. When the PGI voltage or any of the 3.3-V, 5-V rail drops below the undervoltage threshold, PGO will be disabled immediately.

Power-Supply Remote On/Off ($\overline{\text{PSON}}$) and Fault Protect Output ($\overline{\text{FPO}}$)

Since the latest personal computer generation focuses on easy turnon and power saving functions, the PC power supply will require two characteristics. One is a dc power supply remote on/off function; the other is standby voltage to achieve very low power consumption of the PC system. Thus, the main power needs to be shut down.

The power supply remote on/off ($\overline{\text{PSON}}$) is an active-low signal that turns on all of the main power rails including the 3.3-V, 5-V, -5-V, and -12-V power rails. When this signal is held high by the PC motherboard or left open circuited, the signal of the fault protect output ($\overline{\text{FPO}}$) also goes high. Thus, the main power rails should not deliver current and should be held at 0 V.

When the $\overline{\text{FPO}}$ signal is held high due to an occurring fault condition, the fault status will be latched and the outputs of the main power rails should not deliver current and should be held at 0 V. Toggling the power-supply remote on/off ($\overline{\text{PSON}}$) from low-to-high will reset the fault-protection latch. During this fault condition only the standby power is not affected.

When $\overline{\text{PSON}}$ goes from high to low or low-to-high, the 38-ms debounce block will be active to avoid that a glitch on the input will disable/enable the $\overline{\text{FPO}}$ output. During this period, the undervoltage function is disabled to prevent turnon failure.

Power should be delivered to the rails only if the $\overline{\text{PSON}}$ signal is held at ground potential, thus, $\overline{\text{FPO}}$ is active low. The $\overline{\text{FPO}}$ pin can be connected to 5 VDC (or up to 15 VDC) through a pullup resistor.

Under-Voltage Protection

The TPS3513 provides undervoltage protection (UVP) for the 12-V rail and undervoltage detect for the 3.3-V and 5-V rails. When an undervoltage condition appears at the VS12 input pin for more than 150 µs, the $\overline{\text{FPO}}$ output goes high and PGO goes low. Also, this fault condition will be latched until $\overline{\text{PSON}}$ is toggled from low-to-high or VDD is removed.

In flyback or forward type off-line switching power supplies, usually designed for small power, the overload protection design is very simple. Most of these type of power supplies are only sensing the input current for an overload condition. The trigger-point needs to be set much higher than the maximum load in order to prevent false turnon.

However, this will cause one critical issue. In case that the connected load is larger than the maximum allowable load but smaller than the trigger-point, the system will always become over-heated and cause failure and damage.

Overcurrent Protection

In bridge or forward type, off-line switching power supplies, usually designed for medium to large power, the overload protection design needs to be very precise. Most of these types of power supplies are sensing the output current for an overload condition. The trigger-point needs to be set higher than the maximum load in order to prevent false turnon.

The TPS3513 provides overcurrent protection (OCP) for the 3.3-V, 5-V, and 12-V rails. When an over current condition appears at the OCP comparator input pins for more than 73 µs, the $\overline{\text{FPO}}$ output goes high and PGO goes low. Also, this fault condition will be latched until $\overline{\text{PSON}}$ is toggled from low-to-high or VDD is removed.

The resistor connected between the RI pin and the GND pin will introduce an accurate $I_{(ref)}$ for the OCP function. Of course, a more accurate resistor tolerance will be better. The formula for choosing the RI resistor is $V_{(RI)}/I_{(ref)}$. The $I_{(ref)}$ range is from 12.5 µA to 62.5 mA. Three OCP comparators and the $I_{(ref)}$ section are supplied by VS12. Current drawn from the VS12 pin is less than 1 mA.

Following is an example on calculating OCP for the 12-V rail:

$RI = V_{(RI)}/I_{(ref)} = 1.15\ V/20\ \mu A = 56\ k\Omega$

$I_{(ref)}$ x C x $R_{(IS12)}$ = $R_{(sense)}$ x $I_{(OCP\_Trip)}$
$I_{(OCP\_Trip)}$ = 20 µA x 8 x 560 Ω/0.01 Ω = 9.2 A
C = Current ratio (see recommended operating conditions)

Overvoltage Protection

The overvoltage protection (OVP) of the TPS3513 monitors 3.3 V, 5 V, and 12 V. When an overvoltage condition appears at one of the 3.3-V, 5-V, or 12-V input pins for more than 73 µs, the $\overline{FPO}$ output goes high and PGO goes low. Also, this fault condition will be latched until $\overline{PSON}$ is toggled from low-to-high or VDD is removed. During fault conditions, most power supplies have the potential to deliver higher output voltages than those normally specified or required. In unprotected equipment, it is possible for output voltages to be high enough to cause internal or external damage of the system. To protect the system under these abnormal conditions, it is common practice to provide overvoltage protection within the power supply.

ABSOLUTE MAXIMUM RATINGS

over operating free-air temperature range (unless otherwise noted)(1)

			UNIT
V_{DD}	Supply voltage(2)		16 V
V_I	Input voltage(2)	$\overline{PSON}$, IS5, IS33, PGI	8 V
	Input voltage	VS33, VS5	16 V
V_O	Output voltage	$\overline{FPO}$	V_{DD} + 0.3 V or 16 V (whichever is less)
		PGO	V_{DD} + 0.3 V or 8 V (whichever is less)
	All other pins(2)		–0.3 V to 16 V
	Continuous total power dissipation		See Dissipation Rating Table
T_A	Operating free-air temperature range		–40°C to 85°C
T_{stg}	Storage temperature range		–65°C to 150°C
	Soldering temperature		260°C

(1) Stresses beyond those listed under *absolute maximum ratings* may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under *recommended operating conditions* is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
(2) All voltage values are with respect to GND.

DISSIPATION RATING TABLE

PACKAGE	$T_A \le 25°C$ POWER RATING	DERATING FACTOR ABOVE $T_A = 25°C$	$T_A = 70°C$ POWER RATING	$T_A = 85°C$ POWER RATING
D	956 mW	7.65 mW/°C	612 mW	497 mW
N	1512 mW	12.1 mW/°C	968 mW	786 mW

RECOMMENDED OPERATING CONDITIONS

at specified temperature range

			MIN	MAX	UNIT
V_{DD}	Supply voltage		4.5	15	V
V_I	Input voltage	$\overline{PSON}$, VS5, VS33, IS5, IS33		7	V
		VS12, IS12		15	
		PGI		V_{DD} + 0.3 V (max = 7 V)	V
V_O	Output voltage	$\overline{FPO}$		15	V
		PGO		7	
$I_{O(Sink)}$	Output sink current	$\overline{FPO}$		20	mA
		PGO		10	
t_r	Supply voltage rising time	See (1)	1		ms
$I_{O(RI)}$	Output current	RI	12.5	62.5	µA
T_A	Operating free-air temperature range		40	85	°C

(1) V_{DD} rising and falling slew rate must be less than 14V/ms.

ELECTRICAL CHARACTERISTICS

over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER			TEST CONDITIONS	MIN	TYP	MAX	UNIT
OVER-VOLTAGE PROTECTION AND OVER-CURRENT PROTECTION							
	Overvoltage threshold	VS33		3.7	3.9	4.1	V
		VS5		5.7	6.1	6.5	
		VS12		13.2	13.8	14.4	
$I_{(ref)}$	Ratio of current sense sink current to current sense setting pin (RI) source current		Resistor at RI = 30 kΩ, 0.1% resistor	7.6	8	8.4	
I_{lkg}	Leakage current ($\overline{FPO}$)		$V_{(\overline{FPO})}$ = 5 V			5	µA
V_{OL}	Low-level output voltage ($\overline{FPO}$)		$I_{(sink)}$ = 20 mA, V_{DD} = 5 V			0.7	V
	Noise deglitch time OVP		V_{DD} = 5 V	35	73	110	µs
$V_{(RI)}$	Current source reference voltage		V_{DD} = 5 V	1.1	1.15	1.2	V
UNDERVOLTAGE LOCKOUT SECTION							
	Start threshold voltage					4.45	V
	Minimum operation voltage after start-up			3.65			V
PGI AND PGO							
$V_{IT(PGI)}$	Input threshold voltage	PGI1		1.10	1.15	1.20	V
		PGI2		0.9	0.95	1	
	Undervoltage threshold	VS33		2	2.2	2.4	V
		VS5		3.3	3.5	3.7	
		VS12		8.5	9	9.5	
	Input offset voltage for OCP comparators			5		5	mV
I_{lkg}	Leakage current (PGO)		PGO = 5 V			5	µA
V_{OL}	Low-level output voltage (PGO)		$I_{(sink)}$ = 10 mA, V_{DD} = 4.5 V			0.4	V
	Short-circuit protection delay	3.3 V, 5 V		49	75	114	ms
$t_{d(1)}$	Delay time	PGI to PGO	V_{DD} = 5 V	200	300	450	ms
		PGI to $\overline{FPO}$	3.2	4.8	7.2		
	Noise deglitch time	PGI to PGO	V_{DD} = 5 V	88	150	225	µs
		PGI to $\overline{FPO}$					
		12-V UVP to $\overline{FPO}$					
$\overline{PSON}$ CONTROL							
I_I	Input pullup current		$\overline{PSON}$ = 0 V		120		µA

ELECTRICAL CHARACTERISTICS (continued)

over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
V_{IH}	High-level input voltage		2.4			V
V_{IL}	Low-level input voltage				1.2	V
$t_{(b)}$	Debounce time ($\overline{PSON}$)	V_{DD} = 5 V	24	38	57	ms
$t_{d(2)}$	Delay time ($\overline{PSON}$ to $\overline{FPO}$)	V_{DD} = 5 V	t_b +1.1	t_b+2.3	t_b+4	ms
TOTAL DEVICE						
I_{DD}	Supply current	$\overline{PSON}$ = 5 V			1	mA

TYPICAL CHARACTERISTICS

SUPPLY CURRENT vs SUPPLY VOLTAGE

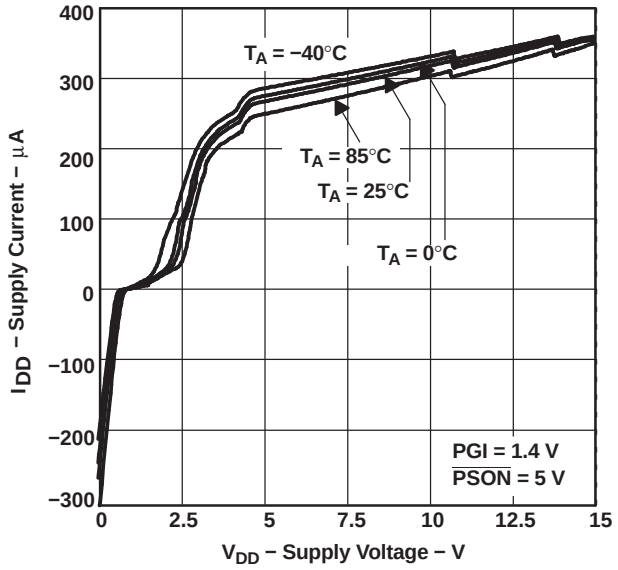


Figure 4.

INPUT CURRENT (PSON) vs INPUT VOLTAGE (PSON)

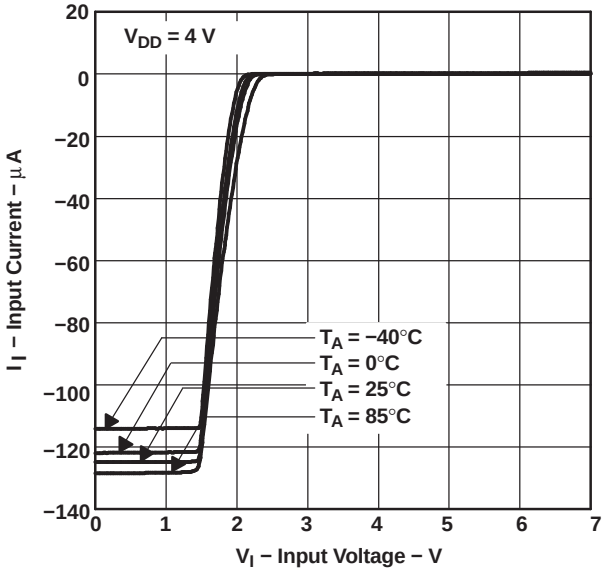


Figure 5.

LOW-LEVEL OUTPUT VOLTAGE (FPO) vs LOW-LEVEL OUTPUT CURRENT (FPO)

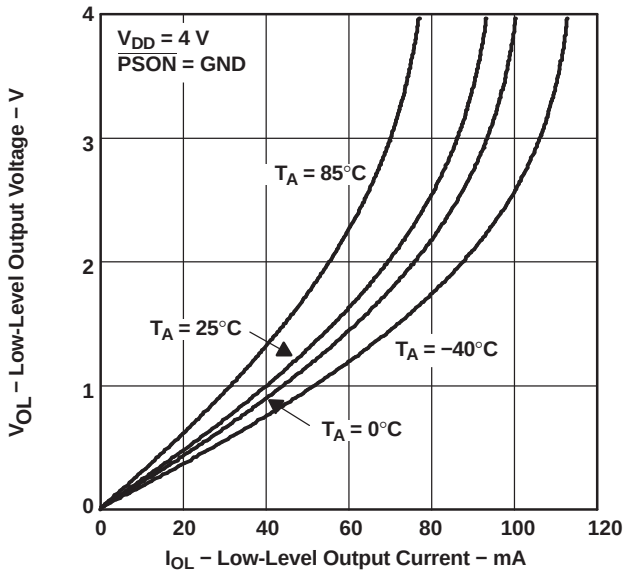


Figure 6.

LOW-LEVEL OUTPUT VOLTAGE (FPO) vs LOW-LEVEL OUTPUT CURRENT (FPO)

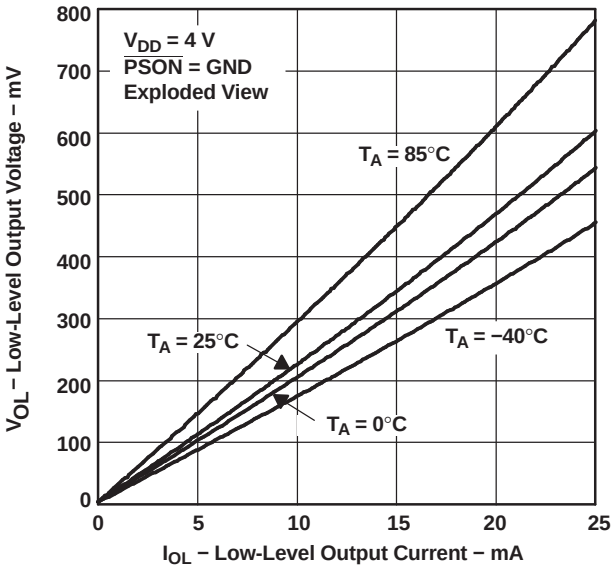


Figure 7.

TYPICAL CHARACTERISTICS (continued)

LOW-LEVEL OUTPUT VOLTAGE (PGO)
vs
LOW-LEVEL OUTPUT CURRENT (PGO)

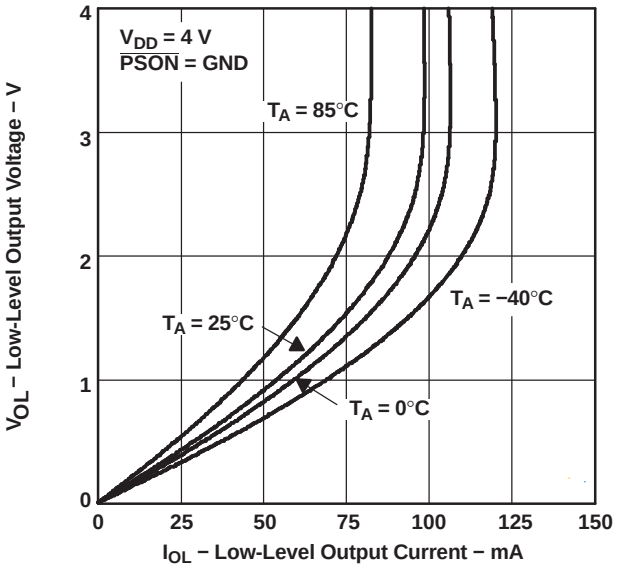


Figure 8.

LOW-LEVEL OUTPUT VOLTAGE (PGO)
vs
LOW-LEVEL OUTPUT CURRENT (PGO)

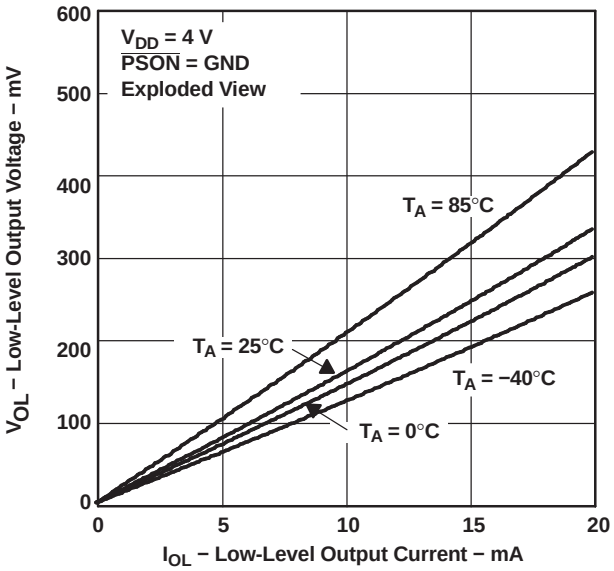


Figure 9.

NORMALIZED SENSE THRESHOLD VOLTAGE
vs
FREE-AIR TEMPERATURE AT V_{DD}

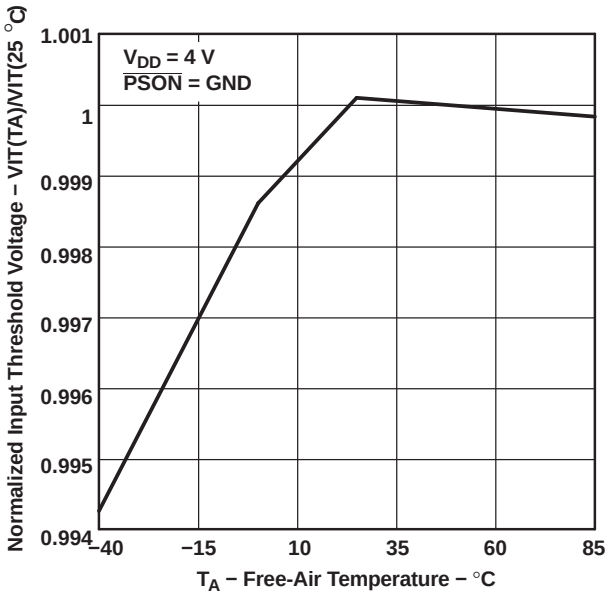


Figure 10.

CURRENT RATIO
vs
FREE-AIR TEMPERATURE

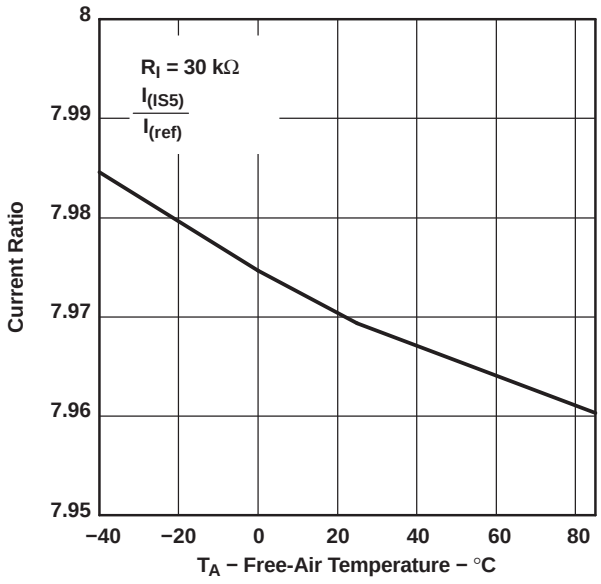


Figure 11.

REVISION HISTORY

Note: Page numbers of current version may differ from previous versions.

Changes from Revision A (June 2005) to Revision B	Page
• Deleted space between OV in the OV Conditions column of Function Table. Also changed 2 H's in FPO column to L's (5th row from bottom and 13th row from bottom)	2
• Changed schematic, Figure 1, and Figure 3 image objects.	3
• Added text to descriptions for $\overline{\text{FPO}}$, PGI, PGO, and $\overline{\text{PSON}}$ pins for clarification.	5
• Changed $t_{b+1.1}$ in MIN column, delay time row to t_b+1.1	9

PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead finish/ Ball material (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
TPS3513D	OBSOLETE	SOIC	D	14		TBD	Call TI	Call TI	-40 to 85	TPS3513D	
TPS3513DR	ACTIVE	SOIC	D	14	2500	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-40 to 85	TPS3513D	Samples
TPS3513N	ACTIVE	PDIP	N	14	25	RoHS & Green	NIPDAU	N / A for Pkg Type	-40 to 85	TPS3513N	Samples

(1) The marketing status values are defined as follows:
ACTIVE: Product device recommended for new designs.
LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
PREVIEW: Device has been announced but is not in production. Samples may or may not be available.
OBSOLETE: TI has discontinued the production of the device.

(2) **RoHS:** TI defines "RoHS" to mean semiconductor products that are compliant with the current EU RoHS requirements for all 10 RoHS substances, including the requirement that RoHS substance do not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, "RoHS" products are suitable for use in specified lead-free processes. TI may reference these types of products as "Pb-Free".
RoHS Exempt: TI defines "RoHS Exempt" to mean products that contain lead but are compliant with EU RoHS pursuant to a specific EU RoHS exemption.
Green: TI defines "Green" to mean the content of Chlorine (Cl) and Bromine (Br) based flame retardants meet JS709B low halogen requirements of <=1000ppm threshold. Antimony trioxide based flame retardants must also meet the <=1000ppm threshold requirement.

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

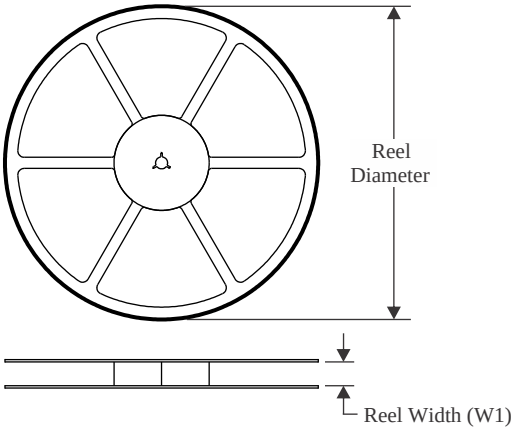
(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

(6) Lead finish/Ball material - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

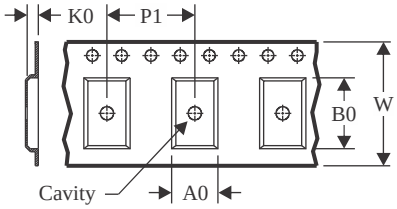
In no event shall TI's liability arising out of such information exceed the total purchase price of the TI part(s) at issue in this document sold by TI to Customer on an annual basis.

TAPE AND REEL INFORMATION

REEL DIMENSIONS

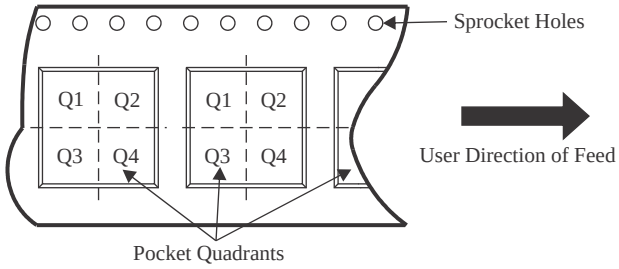


TAPE DIMENSIONS



A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

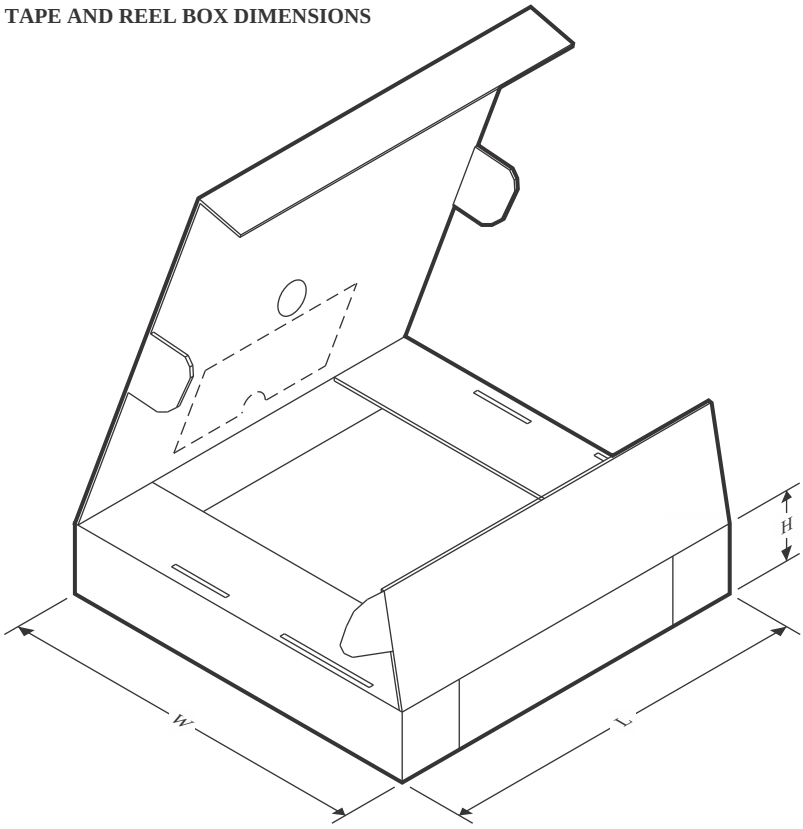
QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
TPS3513DR	SOIC	D	14	2500	330.0	16.4	6.5	9.0	2.1	8.0	16.0	Q1

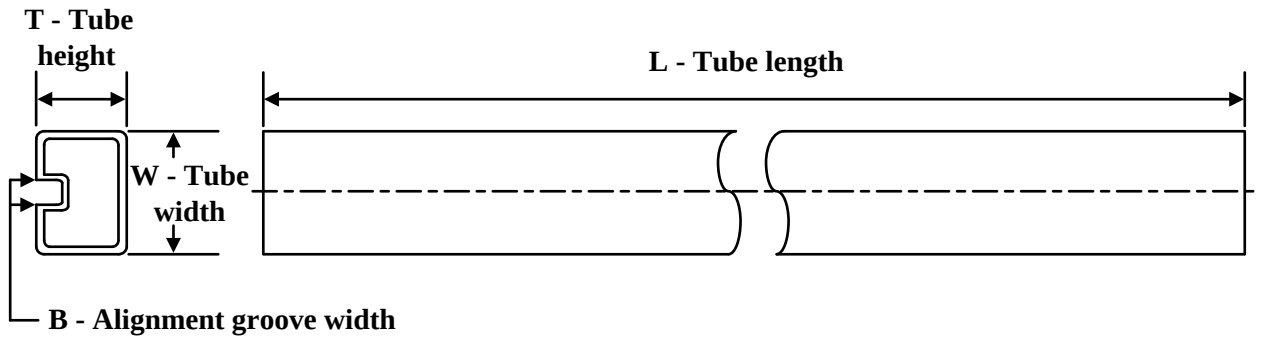
TAPE AND REEL BOX DIMENSIONS



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
TPS3513DR	SOIC	D	14	2500	340.5	336.1	32.0

TUBE



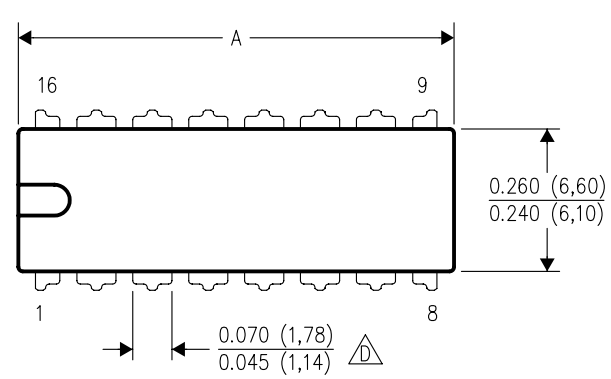
*All dimensions are nominal

Device	Package Name	Package Type	Pins	SPQ	L (mm)	W (mm)	T (µm)	B (mm)
TPS3513N	N	PDIP	14	25	506	13.97	11230	4.32

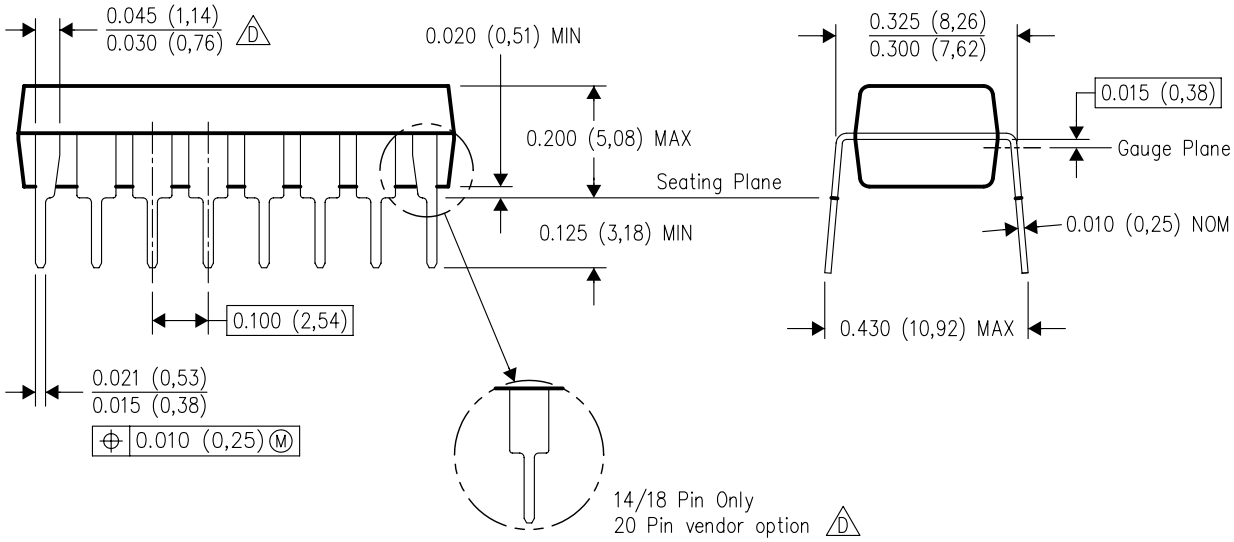
N (R–PDIP–T**)

PLASTIC DUAL–IN–LINE PACKAGE

16 PINS SHOWN

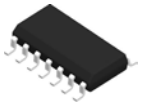


DIM \ PINS **	14	16	18	20
A MAX	0.775 (19,69)	0.775 (19,69)	0.920 (23,37)	1.060 (26,92)
A MIN	0.745 (18,92)	0.745 (18,92)	0.850 (21,59)	0.940 (23,88)
MS–001 VARIATION (C)	AA	BB	AC	AD



4040049/E 12/2002

NOTES:
A. All linear dimensions are in inches (millimeters).
B. This drawing is subject to change without notice.
C. Falls within JEDEC MS–001, except 18 and 20 pin minimum body length (Dim A).
D. The 20 pin end lead shoulder width is a vendor option, either half or full width.

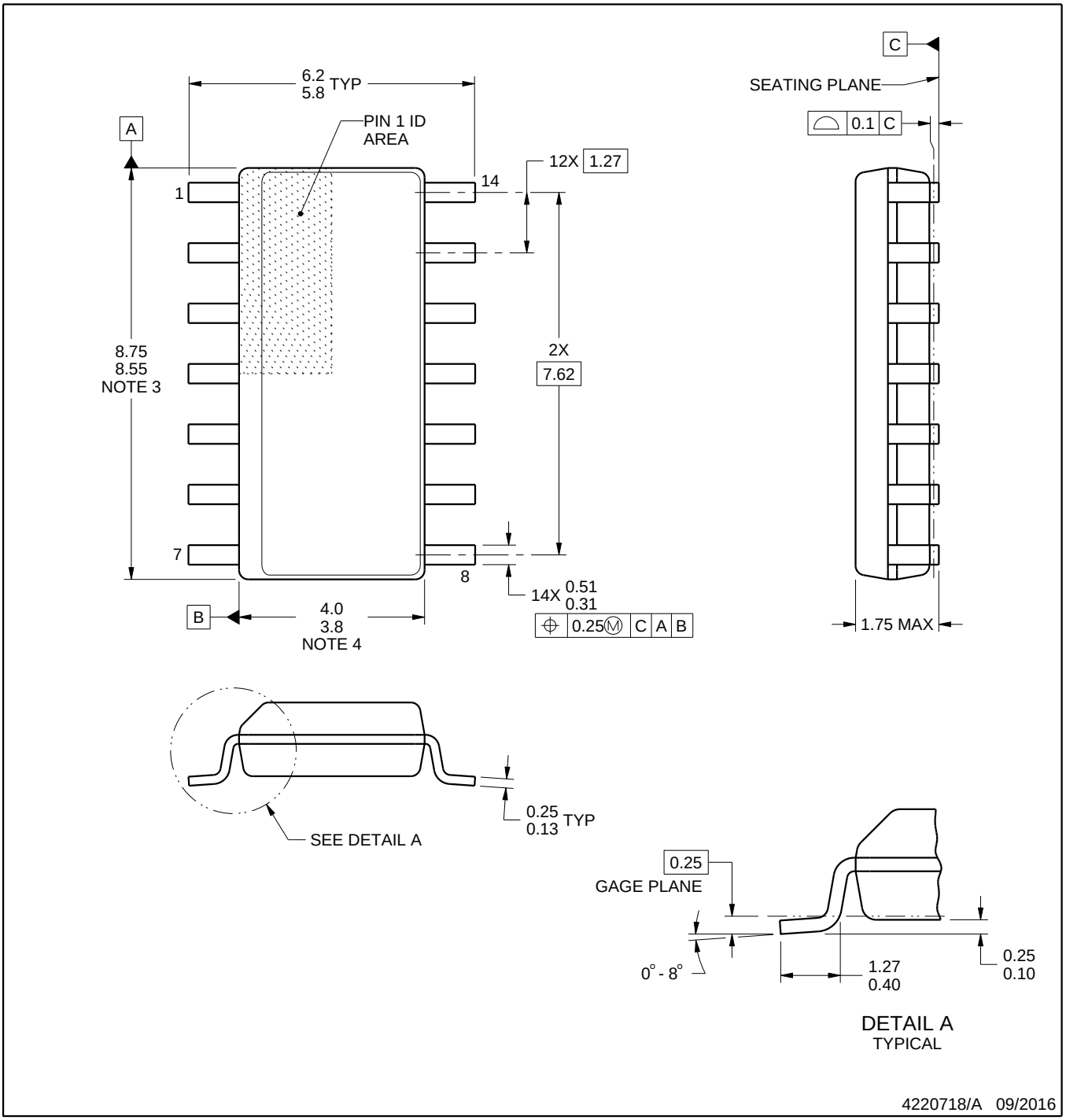


PACKAGE OUTLINE

D0014A

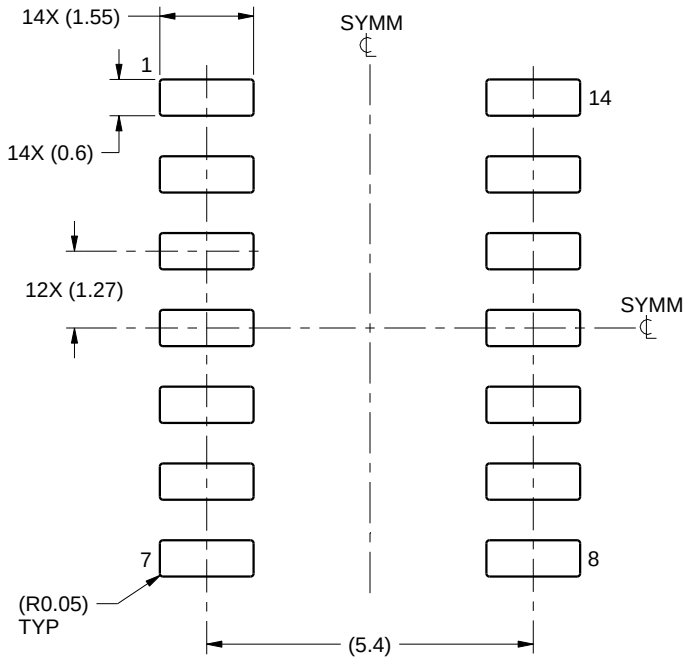
SOIC - 1.75 mm max height

SMALL OUTLINE INTEGRATED CIRCUIT

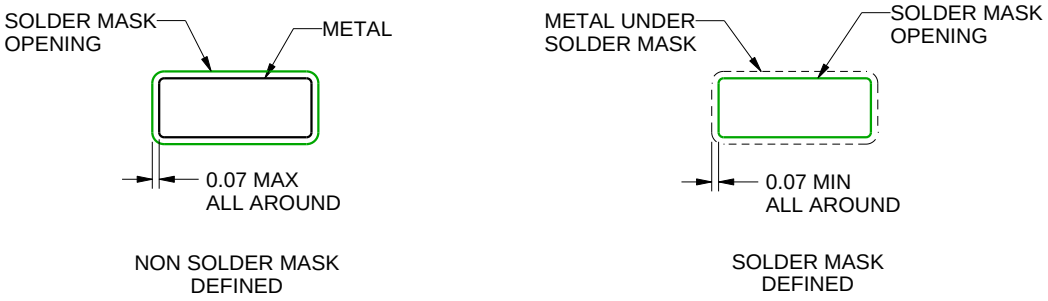


NOTES:

1. All linear dimensions are in millimeters. Dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.15 mm, per side.
4. This dimension does not include interlead flash. Interlead flash shall not exceed 0.43 mm, per side.
5. Reference JEDEC registration MS-012, variation AB.



LAND PATTERN EXAMPLE
SCALE:8X



SOLDER MASK DETAILS

4220718/A 09/2016

NOTES: (continued)

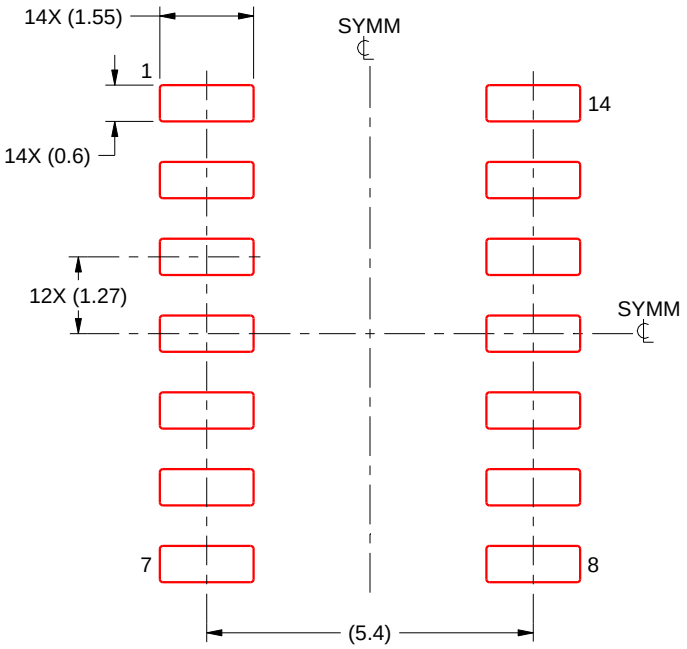
6. Publication IPC-7351 may have alternate designs.
7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.

EXAMPLE STENCIL DESIGN

D0014A

SOIC - 1.75 mm max height

SMALL OUTLINE INTEGRATED CIRCUIT



SOLDER PASTE EXAMPLE
BASED ON 0.125 mm THICK STENCIL
SCALE:8X

4220718/A 09/2016

NOTES: (continued)

8. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
9. Board assembly site may have different recommendations for stencil design.

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