TPS54231 2-A, 28-V Input, Step-Down DC-DC Converter With Eco-mode™

1 Features

- 3.5- to 28-V Input Voltage Range
- Adjustable Output Voltage Down to 0.8 V
- Integrated 80-mΩ High-Side MOSFET Supports up to 2 A Continuous Output Current
- High Efficiency at Light Loads with a Pulse Skipping Eco-mode™
- Fixed 570-kHz Switching Frequency
- Typical 1-µA Shutdown Quiescent Current
- Adjustable Slow-Start Limits Inrush Currents
- Programmable UVLO Threshold
- Overvoltage Transient Protection
- Cycle-by-Cycle Current Limit, Frequency Fold Back and Thermal Shutdown Protection
- Available in Easy-to-Use SOIC8 Package
- Supported by WEBENCH® Software Tool (www.TI.com/WEBENCH)

2 Applications

- Consumer Applications such as Set-Top Boxes, CPE Equipment, LCD Displays, Peripherals, and Battery Chargers
- Industrial and Car Audio Power Supplies
- 5-V, 12-V and 24-V Distributed Power Systems

3 Description

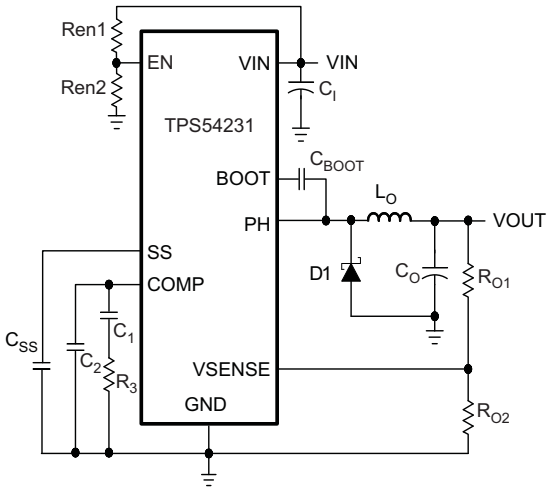
The TPS54231 device is a 2-V, 2-A non-synchronous buck converter that integrates a low $R_{DS(on)}$ high-side MOSFET. To increase efficiency at light loads, a pulse skipping Eco-mode™ feature is automatically activated. Furthermore, the 1-µA shutdown supply current allows the device to be used in battery powered applications. Current mode control with internal slope compensation simplifies the external compensation calculations and reduces component count while allowing the use of ceramic output capacitors. A resistor divider programs the hysteresis of the input undervoltage lockout. An overvoltage transient protection circuit limits voltage overshoots during startup and transient conditions. A cycle-by-cycle current limit scheme, frequency fold back and thermal shutdown protect the device and the load in the event of an overload condition. The TPS54231 device is available in an 8-pin SOIC package that has been internally optimized to improve thermal performance.

Device Information(1)

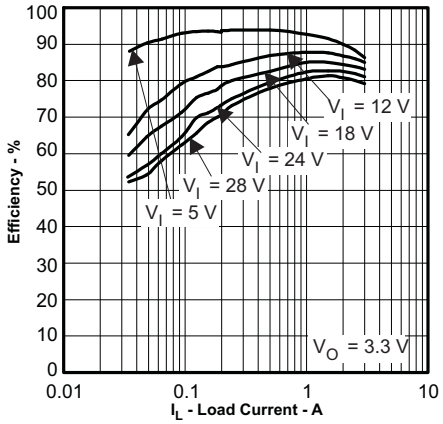
PART NUMBER	PACKAGE	BODY SIZE (NOM)
TPS54231	SOIC (8)	4.90 mm × 3.90 mm

(1) For all available packages, see the orderable addendum at the end of the datasheet.

4 Simplified Schematic



Efficiency



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5 Revision History

NOTE: Page numbers for previous revisions may differ from page numbers in the current version.

Changes from Revision C (July 2012) to Revision D — **Page**

- Added *Handling Ratings* table, *Feature Description* section, *Device Functional* Modes, *Application and Implementation* section, *Power Supply Recommendations* section, *Layout* section, *Device and Documentation Support* section, and *Mechanical, Packaging, and Orderable Information* section. ... 1

Changes from Revision B (February 2012) to Revision C — **Page**

- Added 5.3 to the MAX column of the ELEC CHAR table, section CURRENT LIMIT ... 6
- Deleted Maximum Power Dissipation versus Junction Temperature graph ... 23

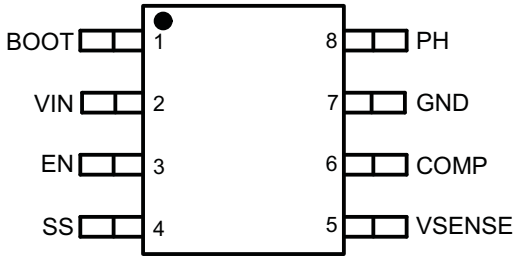
Changes from Revision A (March 2010) to Revision B — **Page**

- Removed SWIFT™ from the data sheet title ... 1
- Deleted Features Item: For SWIFT™ Documentation, See the TI Website at http://www.ti.com/swift ... 1

Changes from Original (October 2008) to Revision A **Page**

6 Pin Configuration and Functions

D Package
8-Pin SOIC
Top View



Pin Functions

PIN		I/O	DESCRIPTION
NO.	NAME		
1	BOOT	O	A 0.1-µF bootstrap capacitor is required between the BOOT and PH pins. If the voltage on this capacitor falls below the minimum requirement, the high-side MOSFET is forced to switch off until the capacitor is refreshed.
2	VIN	I	This pin is the 3.5- to 28-V input supply voltage.
3	EN	I	This pin is the enable pin. To disable, pull below 1.25 V. Float this pin to enable. Programming the input undervoltage lockout with two resistors is recommended.
4	SS	I	This pin is slow-start pin. An external capacitor connected to this pin sets the output rise time.
5	VSENSE	I	This pin is the inverting node of the transconductance (gm) error amplifier.
6	COMP	O	This pin is the error-amplifier output and input to the PWM comparator. Connect frequency compensation components to this pin.
7	GND	—	Ground pin
8	PH	O	The PH pin is the source of the internal high-side power MOSFET.

7 Specifications

7.1 Absolute Maximum Ratings(1)

over operating free-air temperature range (unless otherwise noted)

		MIN	MAX	UNIT
Input voltage	VIN	–0.3	30	V
	EN	–0.3	6	
	BOOT		38	
	VSENSE	–0.3	3	
	COMP	–0.3	3	
	SS	–0.3	3	
Output voltage	BOOT-PH		8	V
	PH	–0.6	30	
	PH (10 ns transient from ground to negative peak)		–5	
Source current	EN		100	µA
	BOOT		100	mA
	VSENSE		10	µA
	PH		6	A
Sink current	VIN		6	A
	COMP		100	µA
	SS		200	
Operating junction temperature, T_J		–40	150	°C

(1) Stresses beyond those listed under absolute maximum ratings may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under recommended operating conditions is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

7.2 Handling Ratings

			MIN	MAX	UNIT
T_{stg}	Storage temperature range		–65	150	°C
$V_{(ESD)}$	Electrostatic discharge	Human body model (HBM), per ANSI/ESDA/JEDEC JS-001, all pins(1)	–2	2	kV
		Charged device model (CDM), per JEDEC specification JESD22-C101, all pins(2)	–500	500	V

(1) JEDEC document JEP155 states that 500-V HBM allows safe manufacturing with a standard ESD control process.
(2) JEDEC document JEP157 states that 250-V CDM allows safe manufacturing with a standard ESD control process.

7.3 Recommended Operating Conditions

over operating free-air temperature range (unless otherwise noted)

		MIN	MAX	UNIT
	Operating Input Voltage on (VIN pin)	3.5	28	V
T_J	Operating junction temperature	–40	150	°C

7.4 Thermal Information

THERMAL METRIC(1)		D 8 PINS	UNIT
$R_{\theta JA}$	Junction-to-ambient thermal resistance	116.3	°C/W
$R_{\theta JC(top)}$	Junction-to-case (top) thermal resistance	53.7	
$R_{\theta JB}$	Junction-to-board thermal resistance	57.1	
ψ_{JT}	Junction-to-top characterization parameter	12.9	
ψ_{JB}	Junction-to-board characterization parameter	56.5	

(1) For more information about traditional and new thermal metrics, see the *IC Package Thermal Metrics* application report, SPRA953.

7.5 Electrical Characteristics

T_J = –40°C to 150°C, VIN = 3.5 to 28 V (unless otherwise noted)

PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNIT
SUPPLY VOLTAGE (VIN PIN)					
Internal undervoltage lockout threshold	Rising and falling			3.5	V
Shutdown supply current	EN = 0V, VIN = 12V, –40°C to 85°C		1	4	µA
Operating – non switching supply current	VSENSE = 0.85 V		75	110	µA
ENABLE AND UVLO (EN PIN)					
Enable threshold	Rising and falling		1.25	1.35	V
Input current	Enable threshold – 50 mV		-1		µA
Input current	Enable threshold + 50 mV		-4		µA
VOLTAGE REFERENCE					
Voltage reference		0.772	0.8	0.828	V
HIGH-SIDE MOSFET					
On resistance	BOOT-PH = 3 V, VIN = 3.5 V		115	200	mΩ
	BOOT-PH = 6 V, VIN = 12 V		80	150	
ERROR AMPLIFIER					
Error amplifier transconductance (gm)	–2 µA < $I_{(COMP)}$ < 2 µA, $V_{(COMP)}$ = 1 V		92		µmhos
Error amplifier DC gain(1)	VSENSE = 0.8 V		800		V/V
Error amplifier unity gain bandwidth(1)	5 pF capacitance from COMP to GND pins		2.7		MHz
Error amplifier source/sink current	$V_{(COMP)}$ = 1 V, 100-mV overdrive		±7		µA
Switch current to COMP transconductance	VIN = 12 V		9		A/V
PULSE SKIPPING ECO-MODE					
Pulse skipping Eco-mode™ switch current threshold			100		mA
CURRENT LIMIT					
Current limit threshold	VIN = 12 V	2.3	3.5	5.3	A
THERMAL SHUTDOWN					
Thermal Shutdown			165		°C
SLOW START (SS PIN)					
Charge current	$V_{(SS)}$ = 0.4 V		2		µA
SS to VSENSE matching	$V_{(SS)}$ = 0.4 V		10		mV

(1) Specified by design.

7.6 Switching Characteristics

T_J = –40°C to 150°C, VIN = 3.5 to 28 V (unless otherwise noted)

PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNIT
SWITCHING FREQUENCY					
TPS54231 device switching frequency	VIN = 12 V	400	570	740	kHz
Minimum controllable on time	VIN = 12 V, 25°C		105	130	ns
Maximum controllable duty ratio(1)	BOOT-PH = 6 V	90%	93%		

(1) Specified by design.

7.7 Typical Characteristics

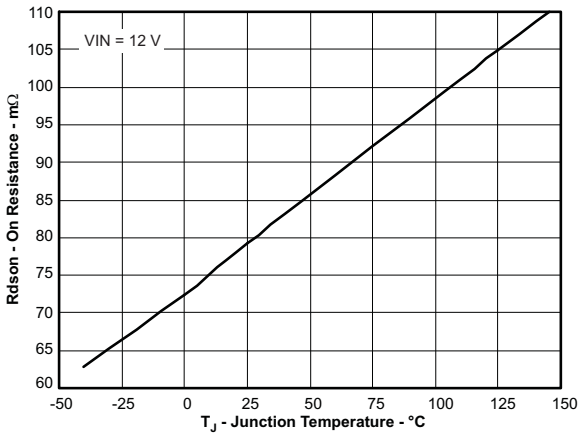


Figure 1. ON Resistance vs Junction Temperature

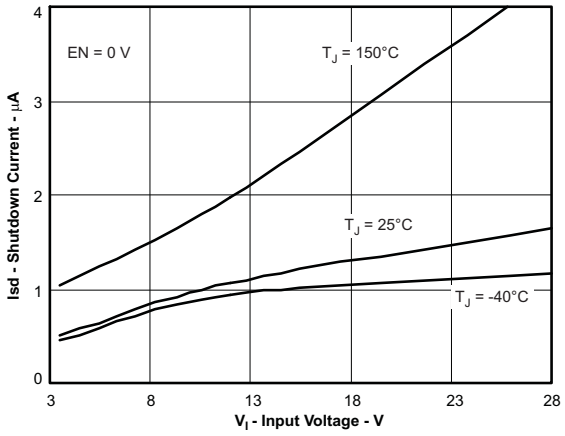


Figure 2. Shutdown Quiescent Current vs Input Voltage

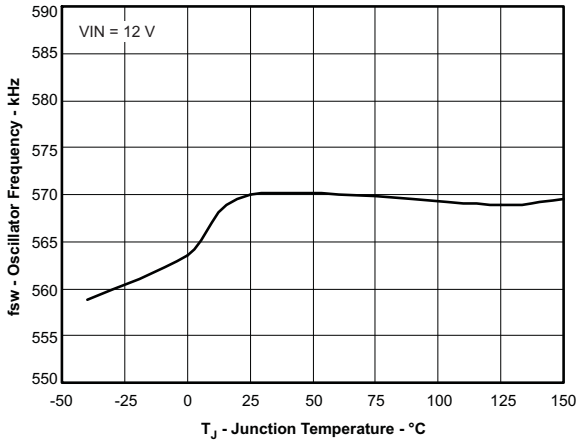


Figure 3. Switching Frequency vs Junction Temperature

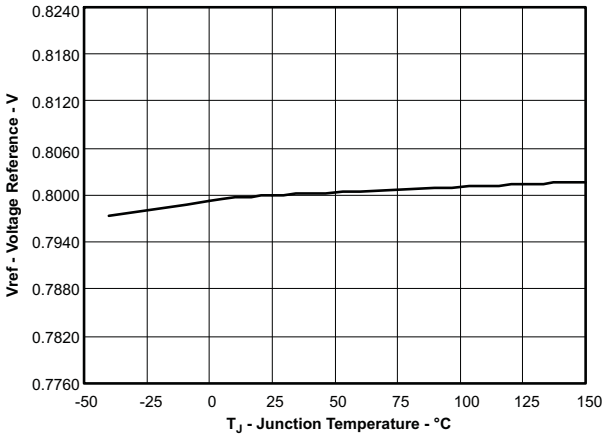


Figure 4. Voltage Reference vs Junction Temperature

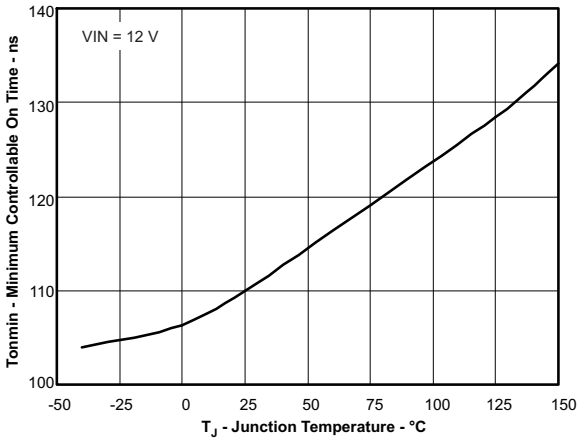


Figure 5. Minimum Controllable ON Time vs Junction Temperature

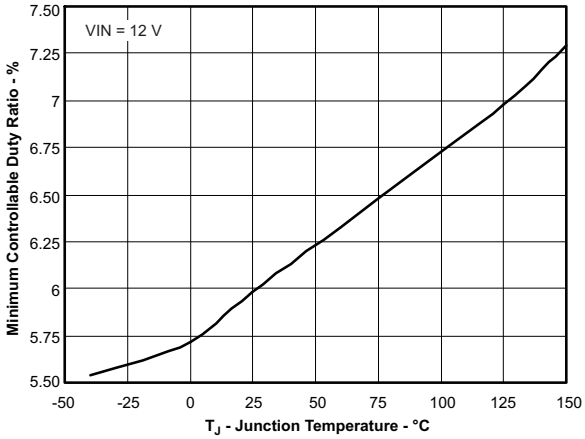


Figure 6. Minimum Controllable Duty Ratio vs Junction Temperature

Typical Characteristics (continued)

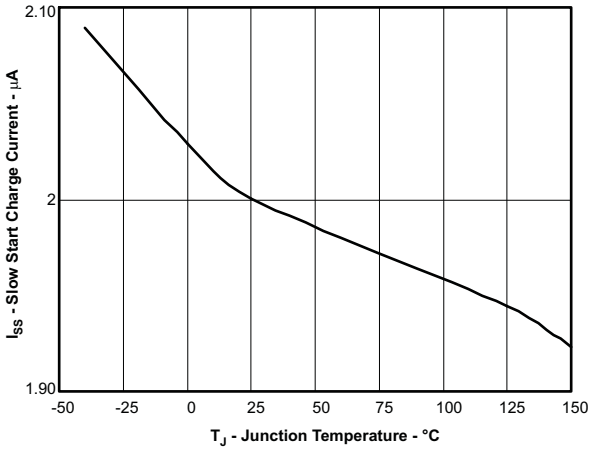


Figure 7. SS Charge Current vs Junction Temperature

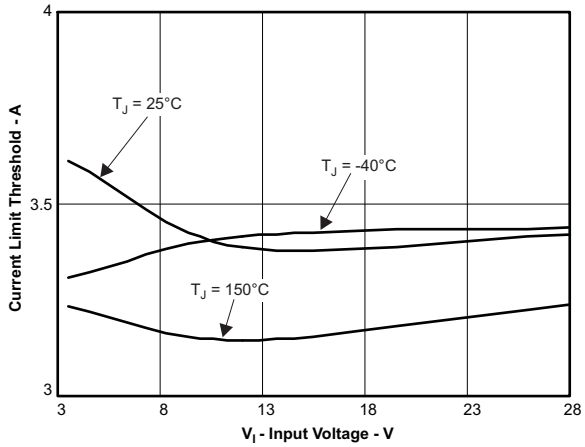


Figure 8. Current-Limit Threshold vs Input Voltage

8 Detailed Description

8.1 Overview

The TPS54231 device is a 28-V, 2-A, step-down (buck) converter with an integrated high-side n-channel MOSFET. To improve performance during line and load transients, the device implements a constant-frequency, current mode control which reduces output capacitance and simplifies external frequency compensation design. The TPS54231 device has a pre-set switching frequency of 570 kHz.

The TPS54231 device requires a minimum input voltage of 3.5 V for normal operation. The EN pin has an internal pullup current source that can be used to adjust the input-voltage undervoltage lockout (UVLO) with two external resistors. In addition, the pullup current provides a default condition when the EN pin is floating for the device to operate. The operating current is 75 µA (typical) when not switching and under no load. When the device is disabled, the supply current is 1 µA (typical).

The integrated 80-mΩ high-side MOSFET allows for high-efficiency power-supply designs with continuous output currents up to 2 A.

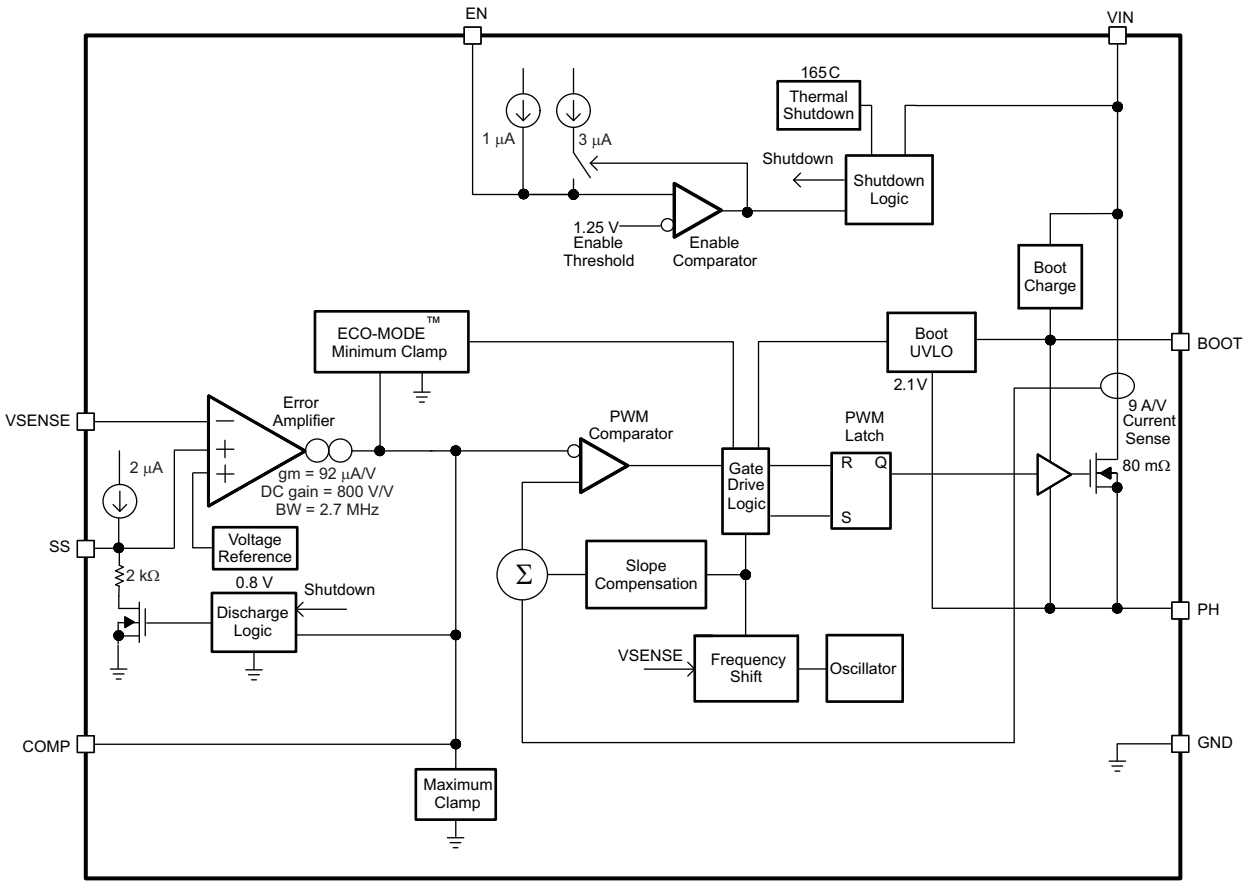
The TPS54231 device reduces the external component count by integrating the boot recharge diode. The bias voltage for the integrated high-side MOSFET is supplied by an external capacitor on the BOOT to PH pin. The boot capacitor voltage is monitored by an UVLO circuit and turns the high-side MOSFET off when the voltage falls below a preset threshold of 2.1 V (typical). The output voltage can be stepped down to as low as the reference voltage.

By adding an external capacitor, the slow-start time of the TPS54231 device can be adjustable which enables flexible output filter selection.

To improve the efficiency at light load conditions, the TPS54231 device enters a special pulse skipping Eco-mode when the peak inductor current drops below 100 mA (typical).

The frequency foldback reduces the switching frequency during startup and overcurrent conditions to help control the inductor current. The thermal shut down provides the additional protection under fault conditions.

8.2 Functional Block Diagram



8.3 Feature Description

8.3.1 Fixed-Frequency PWM Control

The TPS54231 device uses a fixed-frequency, peak-current mode control. The internal switching frequency of the TPS54231 device is fixed at 570 kHz.

8.3.2 Voltage Reference (V_{ref})

The voltage reference system produces a ±2% initial accuracy voltage reference (±3.5% over temperature) by scaling the output of a temperature-stable bandgap circuit. The typical voltage reference is designed at 0.8 V.

8.3.3 Bootstrap Voltage (BOOT)

The TPS54231 device has an integrated boot regulator and requires a 0.1-µF ceramic capacitor between the BOOT and PH pins to provide the gate-drive voltage for the high-side MOSFET. A ceramic capacitor with an X7R- or X5R-grade dielectric is recommended because of the stable characteristics over temperature and voltage. To improve drop out, the TPS54231 device is designed to operate at 100% duty cycle as long as the BOOT-to-PH pin voltage is greater than 2.1 V (typical).

8.3.4 Enable and Adjustable Input Undervoltage Lockout (VIN UVLO)

The EN pin has an internal pullup current-source that provides the default condition of the device while operating when the EN pin floats.

Feature Description (continued)

The TPS54231 device is disabled when the VIN pin voltage falls below internal VIN UVLO threshold. Using an external VIN UVLO to add hysteresis is recommended unless the VIN voltage is greater than (V_{OUT} + 2 V). To adjust the VIN UVLO with hysteresis, use the external circuitry connected to the EN pin as shown in Figure 9. When the EN pin voltage exceeds 1.25 V, an additional 3 µA of hysteresis is added. Use Equation 1 and Equation 2 to calculate the resistor values required for the desired VIN UVLO threshold voltages. The V_{STOP} threshold should always be greater than 3.5 V.

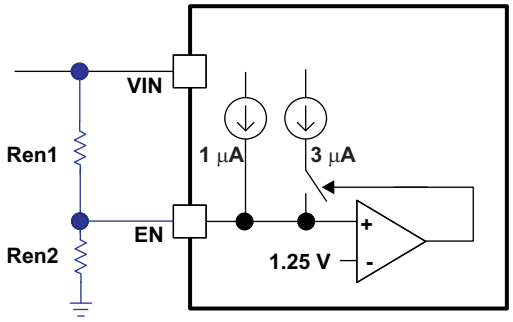


Figure 9. Adjustable Input Undervoltage Lockout

$$Ren1 = \frac{V_{START} - V_{STOP}}{3\ \mu A} \quad (1)$$

where

- V_{START} is the input start threshold voltage
- V_{STOP} is the input stop threshold voltage

$$Ren2 = \frac{V_{EN}}{\frac{V_{START} - V_{EN}}{Ren1} + 1\ \mu A} \quad (2)$$

where

- V_{EN} is the enable threshold voltage of 1.25 V

8.3.5 Programmable Slow Start Using SS Pin

Programming the slow-start time externally is highly recommended because no slow-start time is implemented internally. The TPS54231 device effectively uses the lower voltage of the internal voltage reference or the SS pin voltage as the reference voltage of the power supply that is fed into the error amplifier and regulates the output accordingly. A capacitor (C_{SS}) on the SS pin to ground implements a slow-start time. The TPS54231 device has an internal pullup current-source of 2 µA that charges the external slow-start capacitor. Use Equation 3 to calculate the for the slow-start time (10% to 90%).

$$T_{SS}(ms) = \frac{C_{SS}(nF) \times V_{ref}(V)}{I_{SS}(\mu A)} \quad (3)$$

where

- V_{ref} = 0.8 V
- I_{SS} = 2 µA

The slow-start time should be set between 1 ms to 10 ms to ensure good startup behavior. The value of the slow-start capacitor should not exceed 27 nF.

During normal operation, the TPS54231 device stops switching If during normal operation, the input voltage drops below the VIN UVLO threshold, the EN pin is pulled below 1.25 V, or a thermal shutdown event occurs.

Feature Description (continued)

8.3.6 Error Amplifier

The TPS54231 device has a transconductance amplifier for the error amplifier. The error amplifier compares the VSENSE voltage to the internal effective voltage reference presented at the input of the error amplifier. The transconductance of the error amplifier is 92 µA/V during normal operation. Frequency compensation components are connected between the COMP pin and ground.

8.3.7 Slope Compensation

To prevent the sub-harmonic oscillations when operating the device at duty cycles greater than 50%, the TPS54231 device adds a built-in slope compensation which is a compensating ramp to the switch-current signal.

8.3.8 Current-Mode Compensation Design

To simplify design efforts using the TPS54231 device, the typical designs for common applications are listed in Table 1. For designs using ceramic output capacitors, proper derating of ceramic output capacitance is recommended when performing the stability analysis because the actual ceramic capacitance drops considerably from the nominal value when the applied voltage increases. See the *Detailed Design Procedure* section for the detailed guidelines or use the WEBENCH Software tool (www.TI.com/WEBENCH).

Table 1. Typical Designs (Refer to the *Simplified Schematic*)

V_{IN} (V)	V_{OUT} (V)	f_{SW} (kHz)	L_o (µH)	C_o	R_{O1} (kΩ)	R_{O2} (kΩ)	C_2 (pF)	C_1 (pF)	R_3 (kΩ)
12	5	570	15	Ceramic 33 µF	10	1.91	47	1800	21
12	3.3	570	10	Ceramic 47µF	10	3.24	47	4700	21
12	1.8	570	6.8	Ceramic 100 µF	10	8.06	47	4700	21
12	0.9	570	4.7	Ceramic 100 µF, ×2	10	80.6	47	4700	21
12	5	570	15	Aluminum 330 µF, 160 mΩ	10	1.91	47	220	40.2
12	3.3	570	10	Aluminum 470 µF, 160 mΩ	10	3.24	47	220	21
12	1.8	570	6.8	SP 100 µF, 15 mΩ	10	8.06	47	4700	40.2
12	0.9	570	4.7	SP 220 µF, 12 mΩ	10	80.6	47	4700	40.2

8.3.9 Overcurrent Protection and Frequency Shift

The TPS54231 device implements current mode control that uses the COMP pin voltage to turn off the high-side MOSFET on a cycle-by-cycle basis. During each cycle the switch current and the COMP pin voltage are compared. When the peak inductor current intersects the COMP pin voltage, the high-side switch is turned off. During overcurrent conditions that pull the output voltage low, the error amplifier responds by driving the COMP pin high, causing the switch current to increase. The COMP pin has a maximum clamp internally, which limit the output current.

The TPS54231 device provides robust protection during short circuits. Overcurrent runaway in possible in the output inductor during a short circuit at the output. The TPS54231 device solves this issue by increasing the off time during short-circuit conditions by lowering the switching frequency. The switching frequency is divided by 1, 2, 4, and 8 as the voltage ramps from 0 to 0.8 V on VSENSE pin. The relationship between the switching frequency and the VSENSE pin voltage is listed in Table 2.

Table 2. Switching Frequency Conditions

SWITCHING FREQUENCY	VSENSE PIN VOLTAGE
570 kHz	VSENSE ≥ 0.6 V
570 kHz / 2	0.6 V > VSENSE ≥ 0.4 V
570 kHz / 4	0.4 V > VSENSE ≥ 0.2 V
570 kHz / 8	0.2 V > VSENSE

8.3.10 Overvoltage Transient Protection

The TPS54231 device incorporates an overvoltage transient-protection (OVTP) circuit to minimize output voltage overshoot when recovering from output fault conditions or strong unload transients. The OVTP circuit includes an overvoltage comparator to compare the VSENSE pin voltage and internal thresholds. When the VSENSE pin voltage goes above 109% × V_{ref}, the high-side MOSFET is forced off. When the VSENSE pin voltage falls below 107% × V_{ref}, the high-side MOSFET is enabled again.

8.3.11 Thermal Shutdown

The device implements an internal thermal shutdown to protect the device if the junction temperature exceeds 165°C. The thermal shutdown forces the device to stop switching when the junction temperature exceeds the thermal trip threshold. When the die temperature decreases below 165°C, the device reinitiates the power-up sequence.

8.4 Device Functional Modes

8.4.1 Eco-mode™

The TPS54231 device is designed to operate in pulse skipping Eco-mode at light load currents to boost light load efficiency. When the peak inductor current is lower than 100 mA (typical), the COMP pin voltage falls to 0.5 V (typical) and the device enters Eco-mode . When the device is in Eco-mode, the COMP pin voltage is clamped at 0.5 V internally which prevents the high-side integrated MOSFET from switching. The peak inductor current must rise above 100 mA for the COMP pin voltage to rise above 0.5 V and exit Eco-mode. Because the integrated current comparator catches the peak inductor current only, the average load current entering Eco-mode varies with the applications and external output filters.

8.4.2 Operation With V_{IN} < 3.5 V

The device is recommended to operate with input voltages above 3.5 V. The typical VIN UVLO threshold is not specified and the device can operate at input voltages down to the UVLO voltage. At input voltages below the actual UVLO voltage, the device does not switch. If the EN pin is externally pulled up or left floating, the device becomes active when the VIN pin passes the UVLO threshold. Switching begins when the slow-start sequence is initiated.

8.4.3 Operation With EN Control

The enable threshold voltage is 1.25 V (typical). With the EN pin is held below that voltage the device is disabled and switching is inhibited even if the VIN pin is above the UVLO threshold. The IC quiescent current is reduced in this state. If the EN voltage increases above the threshold while the VIN pin is above the UVLO threshold, the device becomes active. Switching is enabled, and the slow-start sequence is initiated.

9 Application and Implementation

NOTE

Information in the following applications sections is not part of the TI component specification, and TI does not warrant its accuracy or completeness. TI's customers are responsible for determining suitability of components for their purposes. Customers should validate and test their design implementation to confirm system functionality.

9.1 Application Information

The TPS54231 device is typically used as a step-down converter, which converts a voltage from 3.5 V to 28 V to a lower voltage. WEBENCH software is available to aid in the design and analysis of circuits.

For additional design needs, see the following devices:

PARAMETER	TPS54231	TPS54232	TPS54233	TPS54331	TPS54332
I_O(max)	2 A	2 A	2 A	3 A	3.5 A
Input voltage range	3.5 to 28 V	3.5 to 28 V	3.5 to 28 V	3.5 to 28 V	3.5 to 28 V
Switching frequency (typ)	570 kHz	1000 kHz	285 kHz	570 kHz	1000 kHz
Switch current limit (min)	2.3 A	2.3 A	2.3 A	3.5 A	4.2 A
Pin and Package	8SOIC	8SOIC	8SOIC	8SOIC	8SO PowerPAD™

9.2 Typical Application

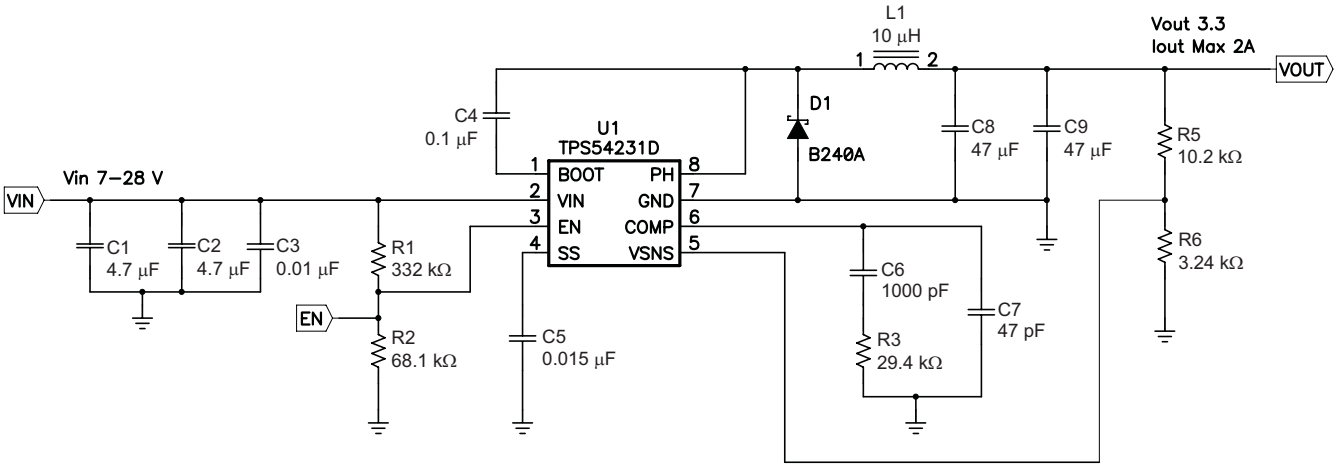


Figure 10. Typical Application Schematic

9.2.1 Design Requirements

For this design example, use the parameters listed in Table 3 as the input parameters.

Table 3. Design Parameters

DESIGN PARAMETER	EXAMPLE VALUE
Input voltage range	7 to 28 V
Output voltage	3.3 V
Input ripple voltage	300 mV
Output ripple voltage	30 mV
Output current rating	2 A
Operating Frequency	570 kHz

9.2.2 Detailed Design Procedure

The following design procedure can be used to select component values for the TPS54231 device. Alternately, the WEBENCH Software can be used to generate a complete design. The WEBENCH Software uses an iterative design procedure and accesses a comprehensive database of components when generating a design. This section presents a simplified discussion of the design process.

9.2.2.1 Switching Frequency

The switching frequency for the TPS54231 device is fixed at 570 kHz.

9.2.2.2 Output Voltage Set Point

The output voltage of the TPS54231 device is externally adjustable using a resistor divider network. As shown in Figure 10, this divider network is comprised of R5 and R6. The relationship of the output voltage to the resistor divider is given by Equation 4 and Equation 5.

$$R6 = \frac{R5 \times V_{REF}}{V_{OUT} - V_{REF}} \tag{4}$$

$$V_{OUT} = V_{REF} \times \left[\frac{R5}{R6} + 1\right] \tag{5}$$

Select a value of R5 to be approximately 10 kΩ. Slightly increasing or decreasing the value of R5 can result in closer output-voltage matching when using standard value resistors. In this design, R4 = 10.2 kΩ and R = 3.24 kΩ, resulting in a 3.31-V output voltage. The 0-Ω resistor R4 is provided as a convenient location to break the control loop for stability testing.

9.2.2.3 Input Capacitors

The TPS54231 device requires an input decoupling capacitor and, depending on the application, a bulk input capacitor. The typical recommended value for the decoupling capacitor is 10 µF. A high-quality ceramic type X5R or X7R is recommended. The voltage rating should be greater than the maximum input voltage. A smaller value can be used as long as all other requirements are met; however a value of 10 µF has been shown to work well in a wide variety of circuits. Additionally, some bulk capacitance may be required, especially if the TPS54231 device circuit is not located within about 2 inches from the input voltage source. The value for this capacitor is not critical but should be rated to handle the maximum input voltage including ripple voltage, and should filter the output so that input ripple voltage is acceptable. For this design two 4.7-µF capacitors are used for the input decoupling capacitor. The capacitors are X7R dielectric rated for 50 V. The equivalent series resistance (ESR) is approximately 2 mΩ, and the current rating is 3 A. Additionally, a small 0.01-µF capacitor is included for high frequency filtering.

Use Equation 6 to calculate the input ripple voltage.

$$\Delta V_{IN} = \frac{I_{OUT(MAX)} \times 0.25}{C_{BULK} \times f_{SW}} + \left(I_{OUT(MAX)} \times ESR_{MAX}\right) \tag{6}$$

where

- $I_{OUT(MAX)}$ is the maximum load current
- f_{SW} is the switching frequency
- C_{BULK} is the bulk capacitor value
- ESR_{MAX} is the maximum series resistance of the bulk capacitor

The maximum RMS ripple current must also be checked. For worst case conditions, use Equation 7 to calculate the maximum-RMS input ripple current, $I_{CIN(RMS)}$.

$$I_{CIN(RMS)} = \frac{I_{OUT(MAX)}}{2} \tag{7}$$

In this case, the input ripple voltage is 113 mV and the RMS ripple current is 1 A.

NOTE

The actual input voltage ripple is greatly affected by parasitics associated with the layout and the output impedance of the voltage source.

The actual input voltage ripple for this circuit is listed in Table 3 and is larger than the calculated value. This measured value is still below the specified input limit of 300 mV. The maximum voltage across the input capacitors would be $V_{IN(MAX)}$ plus ΔV_{IN} / 2. The selected bulk and bypass capacitors are each rated for 50 V and the ripple current capacity is greater than 3 A, both providing ample margin. The maximum ratings for voltage and current must not be exceeded under any circumstance.

9.2.2.4 Output Filter Components

Two components need to be selected for the output filter, L1 and C2. Because the TPS54231 device is an externally compensated device, a wide range of filter component types and values can be supported.

9.2.2.4.1 Inductor Selection

To calculate the minimum value of the output inductor, use Equation 8.

$$L_{MIN} = \frac{V_{OUT(MAX)} \times \left(V_{IN(MAX)} - V_{OUT}\right)}{V_{IN(MAX)} \times K_{IND} \times I_{OUT} \times f_{SW}} \quad (8)$$

where

- K_{IND} is a coefficient that represents the amount of inductor ripple current relative to the maximum output current

In general, this value is at the discretion of the designer; however, the following guidelines may be used. For designs using low-ESR output capacitors such as ceramics, a value as high as K_{IND} = 0.3 may be used. When using higher ESR output capacitors, K_{IND} = 0.2 yields better results.

For this design example, use K_{IND} = 0.3 and the minimum inductor value is calculated as 8.5 µH. For this design, a large value was selected: 10 µH.

For the output filter inductor, do not exceed the RMS current and saturation current ratings. Use Equation 9 to calculate the inductor ripple current (I_{LPP}).

$$I_{LPP} = \frac{V_{OUT} \times \left(V_{IN(MAX)} - V_{OUT}\right)}{V_{IN(MAX)} \times L_{OUT} \times f_{SW} \times 0.8} \quad (9)$$

Use Equation 10 to calculate the RMS inductor current.

$$I_{L(RMS)} = \sqrt{I^2_{OUT(MAX)} + \frac{1}{12} \times I^2_{LPP}} \quad (10)$$

Use Equation 11 to calculate the peak inductor current.

$$I_{L(PK)} = I_{OUT(MAX)} + \frac{I_{LPP}}{2} \quad (11)$$

For this design, the RMS inductor current is 2.008 A and the peak inductor current is 2.32 A. The selected inductor is a Coilcraft MSS1038-103NL, 10 µH. This inductor has a saturation current rating of 3.04 A and an RMS current rating of 2.90 A, which meets these requirements. Smaller or larger inductor values can be used depending on the amount of ripple current the designer wants to allow so long as the other design requirements are met. Larger value inductors will have lower AC current and result in lower output voltage ripple, while smaller inductor values will increase AC current and output voltage ripple. In general, inductor values for use with the TPS54231 device are in the range of 6.8 µH to 47µH.

9.2.2.4.2 Capacitor Selection

The important design factors for the output capacitor are DC voltage rating, ripple current rating, and equivalent series resistance (ESR). The DC voltage and ripple current ratings cannot be exceeded. The ESR is important because along with the inductor current it determines the amount of output ripple voltage. The actual value of the output capacitor is not critical, but some practical limits do exist. Consider the relationship between the desired closed-loop crossover frequency of the design and LC corner frequency of the output filter. In general, keeping the closed-loop crossover frequency at less than 1/5 of the switching frequency is desired. With high switching frequencies such as the 570-kHz frequency of this design, internal circuit limitations of the TPS54231 device limit the practical maximum crossover frequency to about 25 kHz. In general, the closed-loop crossover frequency should be higher than the corner frequency determined by the load impedance and the output capacitor. Use Equation 12 to calculate the limits of the minimum capacitor value for the output filter.

$$C_{O(MIN)} = 1 / (2 \times \pi \times R_O \times F_{CO(MAX)}) \quad (12)$$

where

- R_O is the output load impedance (V_O / I_O)
- $F_{CO(MAX)}$ is the desired crossover frequency

For a desired maximum crossover of 25 kHz the minimum value for the output capacitor is approximately 3.6 µF. This value may not satisfy the output ripple voltage requirement. Use Equation 13 to estimate the output ripple voltage.

$$V_{OPP} = I_{LPP} \left[\frac{(D - 0.5)}{4 \times f_{SW} \times C_O} + R_{ESR} \right] \quad (13)$$

where

- D = Duty cycle (V_{OUT} / V_{IN})
- C_O = Output Capacitance
- R_{ESR} = Equivalent series resistance of the output capacitors

The peak-to-peak output voltage ripple consists of two terms. The first term is because of the AC ripple current (I_{LPP}) charging and discharging the output capacitance in each switching cycle and the second term is because of the AC ripple current in the ESR of the output capacitor. These two terms could be out of phase and may add or subtract depending on the duty cycle. The required capacitance and ESR of the output filter capacitor must be selected to meet the allowable output ripple voltage requirement as specified in the initial design parameters.

Use Equation 14 to calculate the maximum RMS ripple current in the output capacitor.

$$I_{COUT(RMS)} = \frac{1}{\sqrt{12}} \times I_{LPP} \quad (14)$$

For this design example, two 47-µF ceramic output capacitors are selected for C8 and C9. These capacitors are TDK C3216X5R0J476M, rated at 6.3 V with a maximum ESR of 2 mΩ and a ripple current rating in excess of 3 A. The calculated total RMS ripple current is 184 mA (92 mA each) and the maximum total ESR required is 56 mΩ. These output capacitors exceed the requirements by a wide margin and result in a reliable, high-performance design.

NOTE

The actual capacitance in circuit may be less than the catalog value when the output is operating at the desired output of 3.3 V.

The selected output capacitor must be rated for a voltage greater than the desired output voltage plus half of the ripple voltage. Any derating amount must also be included. Other capacitor types work well with the TPS54231 device, depending on the needs of the application.

9.2.2.5 Compensation Components

The external compensation used with the TPS54231 device allows for a wide range of output filter configurations. A large range of capacitor values and types of dielectric are supported. The design example uses ceramic X5R dielectric output capacitors, but other types are supported.

A Type II compensation scheme is recommended for the TPS54231 device. The compensation components are selected to set the desired closed-loop crossover frequency and phase margin for output filter components. The Type II compensation has the following characteristics: a DC gain component, a low frequency pole, and a mid frequency zero-pole pair. The required compensation components are a resistor, R_Z, in series with a capacitor, R_Z, from the COMP pin to ground and a capacitor, C_P, in parallel with R_Z and C_Z from the COMP pin to ground.

Use Equation 15 to calculate the DC gain.

$$G_{DC} = \frac{V_{ggm} \times V_{REF}}{V_O}$$

where

- V_{ggm} = 800
- V_{REF} = 0.8 V

(15)

Use Equation 16 to calculate the low-frequency pole.

$$F_{PO} = 1/\left(2 \times \pi \times R_{OA} \times C_Z\right)$$

(16)

Use Equation 17 to calculate the mid-frequency zero.

$$F_{Z1} = 1/\left(2 \times \pi \times R_Z \times C_Z\right)$$

(17)

Use Equation 18 to calculate the mid-frequency pole.

$$F_{P1} = 1/\left(2 \times \pi \times R_Z \times C_P\right)$$

(18)

The first step is to select the closed-loop crossover frequency. In general, the closed-loop crossover frequency should be less than 1/8 of the minimum operating frequency. However, for the TPS54231 device, not exceeding 25 kHz for the maximum closed-loop crossover frequency is recommended. The second step is to calculate the required gain and phase boost of the crossover network. By definition, the gain of the compensation network must be the inverse of the gain of the modulator and output filter. For this design example, where the ESR zero is much higher than the closed-loop crossover frequency, the gain of the modulator and output filter can be approximated by Equation 19:

$$\text{Gain} = -20 \log\left(2 \times \pi \times R_{SENSE} \times F_{CO} \times C_O\right) + 3$$

where

- R_{SENSE} = 1 Ω / 9
- F_{CO} = Closed-loop crossover frequency
- C_O = Output capacitance

(19)

Use Equation 20 to calculate the phase loss.

$$PL = a\tan\left(2 \times \pi \times F_{CO} \times R_{ESR} \times C_O\right) - a\tan\left(2 \times \pi \times F_{CO} \times R_O \times C_O\right) - 10$$

where

- R_{ESR} = Equivalent series resistance of the output capacitor
- $R_O = V_O / I_O$

(20)

Now that the phase loss is known, the required amount of phase boost to meet the phase margin requirement can be determined. Use Equation 21 to calculate the required phase boost.

$$PB = \left(PM - 90\,\text{deg}\right) + PL$$

where

- PM = the desired phase margin
- PL = the phase loss calculated in Equation 20

(21)

A zero-pole pair of the compensation network will be placed symmetrically around the intended closed-loop frequency to provide maximum phase boost at the crossover point. The amount of separation can be determined by Equation 22. Use Equation 23 and Equation 24 to calculate the resultant zero and pole frequencies.

$$k = \tan\left(\frac{PB}{2} + 45\,\text{deg}\right) \tag{22}$$

$$F_{Z1} = \frac{F_{CO}}{k} \tag{23}$$

$$F_{P1} = F_{CO} \times k \tag{24}$$

The low-frequency pole is set so that the gain at the crossover frequency is equal to the inverse of the gain of the modulator and output filter. Because of the relationships of the pole and zero frequencies, use Equation 25 to calculate the value of R_Z.

$$R_Z = \frac{2 \times \pi \times F_{CO} \times V_O \times C_O \times R_{OA} \times 0.91}{GM_{COMP} \times V_{ggm} \times V_{REF}} \tag{25}$$

where

- V_O = Output voltage
- C_O = Output capacitance
- F_{CO} = Desired crossover frequency
- R_{OA} = 8.696 MΩ
- GM_{COMP} = 9 A/V
- V_{ggm} = 800
- V_{REF} = 0.8 V

With the value of R_Z known, use Equation 26 and Equation 27 to calculate the values of C_Z and C_P.

$$C_Z = \frac{1}{2 \times \pi \times F_{Z1} \times R_z} \tag{26}$$

$$C_P = \frac{1}{2 \times \pi \times F_{P1} \times R_z} \tag{27}$$

For this design, the two 47-µF output capacitors are used. For ceramic capacitors, the actual output capacitance is less than the rated value when the capacitors have a DC bias voltage applied which occurs in a DC-DC converter. The actual output capacitance may be as low as 41 µF. The combined ESR is approximately 0.002 Ω.

The desired crossover frequency is 25 kHz.

Using Equation 19 and Equation 20, the output stage gain and phase loss are equivalent as:

Gain = 5.9 dB

PL = –93.8 degrees

For 60 degrees of phase margin, Equation 21 requires 63.9 degrees of phase boost.

Use Equation 22, Equation 23, and Equation 24 to calculate the zero and pole frequencies of the following values:

F_{Z1} = 5798 Hz

F_{P1} = 107.8 kHz

Use Equation 25 to calculate the value of R_Z.

$$Rz = \frac{2 \times \pi \times 25000 \times 3.3 \times 41 \times 10^{-6} \times 8.696 \times 10^{6} \times 0.91}{9 \times 800 \times 0.8} = 29.2 \times 10^{3}\ \Omega \tag{28}$$

With the value of R_Z set to the standard value of 29.4 kΩ, the values of C_z and C_P can be calculated using Equation 26 and Equation 27.

$$Cz = \frac{1}{2 \times \pi \times 5798 \times 29400} = 934 \text{ pF} \quad (29)$$

$$Cp = \frac{1}{2 \times \pi \times 107800 \times 29400} = 50 \text{ pF} \quad (30)$$

Referring to Figure 10 and using standard values for R3, C6, and C7, the calculated values are as follows:

R3 = 29.4 kΩ

C6 = 1000 pF

C7 = 47 pF

Figure 16 shows the measured overall loop response for the circuit. The actual closed-loop crossover frequency is higher than intended at about 25 kHz which is primarily because of variation in the actual values of the output filter components and tolerance variation of the internal feed-forward gain circuitry. Overall, the design has greater than 60 degrees of phase margin and will be completely stable over all combinations of line and load variability.

9.2.2.6 Bootstrap Capacitor

Every TPS54231 design requires a bootstrap capacitor, C4. The bootstrap capacitor must be 0.1 µF. The bootstrap capacitor is located between the PH pin and BOOT pin. The bootstrap capacitor should be a high-quality ceramic type with X7R or X5R grade dielectric for temperature stability.

9.2.2.7 Catch Diode

The TPS54231 device is designed to operate using an external catch diode between the PH and GND pins. The selected diode must meet the absolute maximum ratings for the application. The Reverse voltage must be higher than the maximum voltage at the PH pin, which is $V_{IN(MAX)}$ + 0.5 V. The peak current must be greater than $I_{OUT(MAX)}$ plus on half the peak-to-peak inductor current. The forward-voltage drop should be small for higher efficiencies. The catch diode conduction time is (typically) longer than the high-side FET on time, so attention paid to diode parameters can make a marked improvement in overall efficiency. Additionally, check that the selected device is capable of dissipating the power losses. For this design, a Diodes, Inc. B240A is selected, with a reverse voltage of 40 V, forward current of 2 A, and a forward voltage drop of 0.5 V.

9.2.2.8 Output Voltage Limitations

Because of the internal design of the TPS54231 device, any given input voltage has both upper and lower output voltage limits. The upper limit of the output-voltage set point is constrained by the maximum duty cycle of 91% and is with Equation 31.

$$V_{O(MAX)} = 0.91 \times \left(\left(V_{IN(MIN)} - I_{O(MAX)} \times R_{DS(on)max} \right) + V_D \right) - \left(I_{O(MAX)} \times R_L \right) - V_D \quad (31)$$

where

- $V_{IN(MIN)}$ = Minimum input voltage
- $I_{O(MAX)}$ = Maximum load current
- V_D = Catch diode forward voltage
- R_L = Output inductor series resistance

The equation assumes the maximum ON resistance for the internal high-side FET.

The lower limit is constrained by the minimum controllable on time which can be as high as 130 ns at 25°C junction temperature.

Use Equation 32 to calculate the approximate minimum output voltage for a given input voltage and minimum load current.

$$V_{O(MIN)} = 0.096 \times \left(\left(V_{IN(MAX)} - I_{O(MIN)} \times R_{DS(on)min} \right) + V_D \right) - \left(I_{O(MIN)} \times R_L \right) - V_D$$

where

- $V_{IN(MAX)}$ = Maximum input voltage
- $I_{O(MIN)}$ = Minimum load current
- V_D = Catch diode forward voltage
- R_L = Output inductor series resistance (32)

The normal ON resistance for the high-side FET in Equation 32 is assumed. Equation 32 accounts for worst case variation of operating-frequency set point. Any design operating near the operational limits of the device should be carefully checked to ensure proper functionality.

9.2.2.9 Power Dissipation Estimate

The following formulas show how to estimate the device power dissipation under continuous-conduction mode (CCM) operations. These formulas should not be used if the device is working in the discontinuous conduction mode (DCM) or pulse-skipping Eco-mode.

The device power dissipation includes:

1. Conduction loss:

   $Pcon = I_{OUT}^2 \times R_{DS(on)} \times V_{OUT} / V_{IN}$

   where

   - I_{OUT} is the output current (A)
   - $R_{DS(on)}$ is the on-resistance of the high-side MOSFET (Ω)
   - V_{OUT} is the output voltage (V)
   - V_{IN} is the input voltage (V)
2. Switching loss:

   $Psw = 0.5 \times 10^{-9} \times V_{IN}^2 \times I_{OUT} \times f_{SW}$

   where

   - f_{SW} is the switching frequency (Hz)
3. Gate charge loss:

   $Pgc = 22.8 \times 10^{-9} \times f_{SW}$
4. Quiescent current loss:

   $Pq = 0.075 \times 10^{-3} \times V_{IN}$

Therefore:

$Ptot = Pcon + Psw + Pgc + Pq$

where

- Ptot is the total device power dissipation (W)

For given T_A :

$T_J = T_A + Rth \times Ptot$

where

- T_J is the junction temperature (°C)
- T_A is the ambient temperature (°C)
- Rth is the thermal resistance of the package (°C/W)

For given T_{JMAX} = 150°C:

$T_{AMAX} = T_{JMAX} – Rth \times Ptot$

where

- T_{AMAX} is maximum ambient temperature (°C)
- T_{JMAX} is maximum junction temperature (°C)

9.2.3 Application Curves

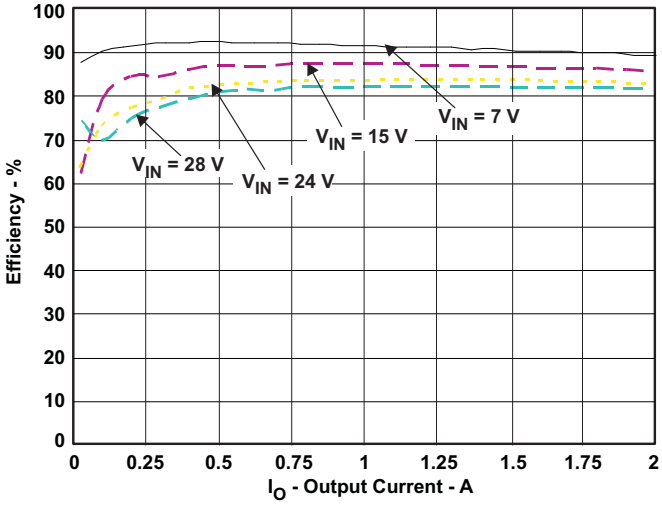


Figure 11. Efficiency

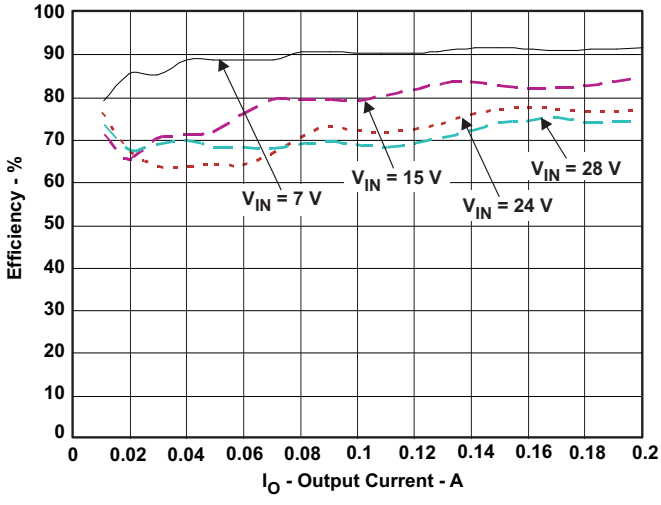


Figure 12. Low Current Efficiency

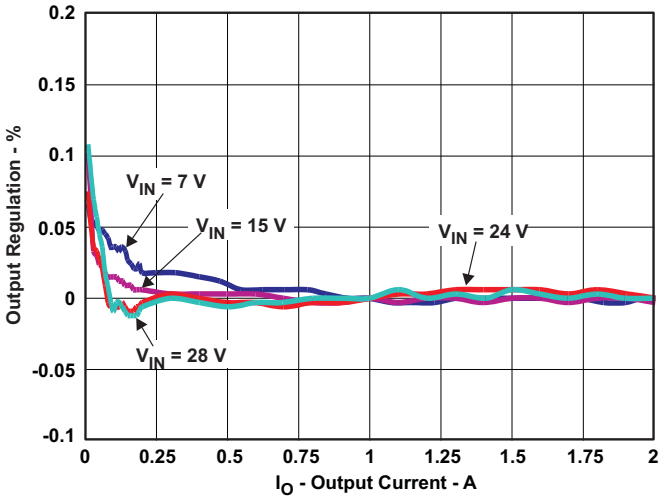


Figure 13. Load Regulation

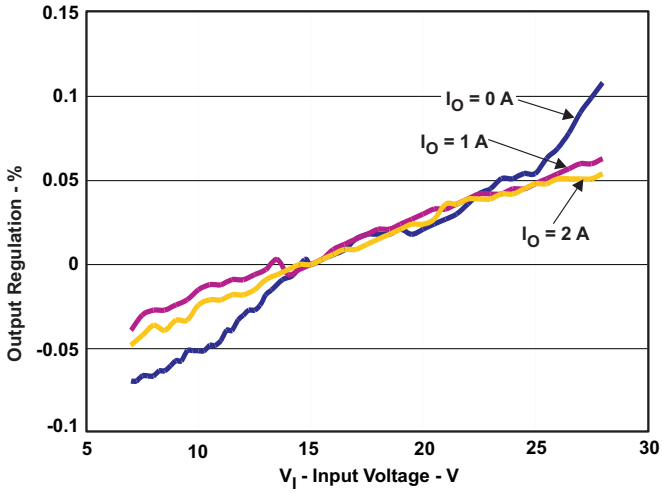


Figure 14. Line Regulation

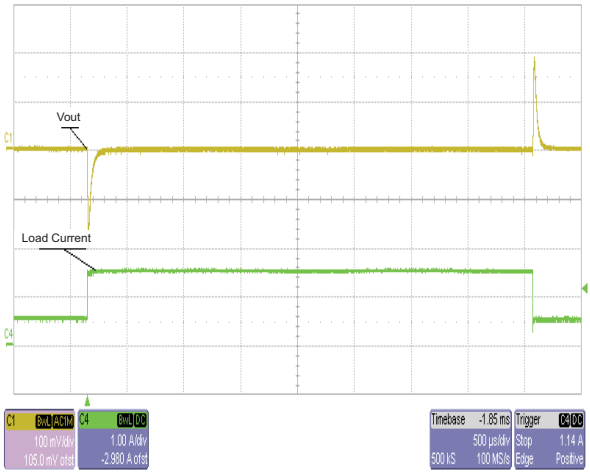


Figure 15. Transient Response

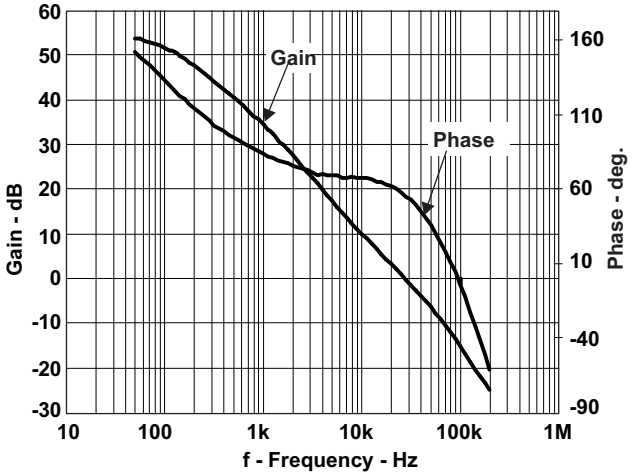


Figure 16. Loop Response

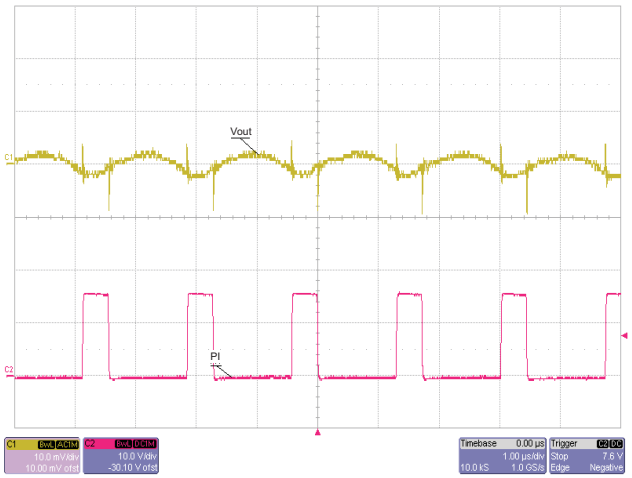


Figure 17. Output Ripple

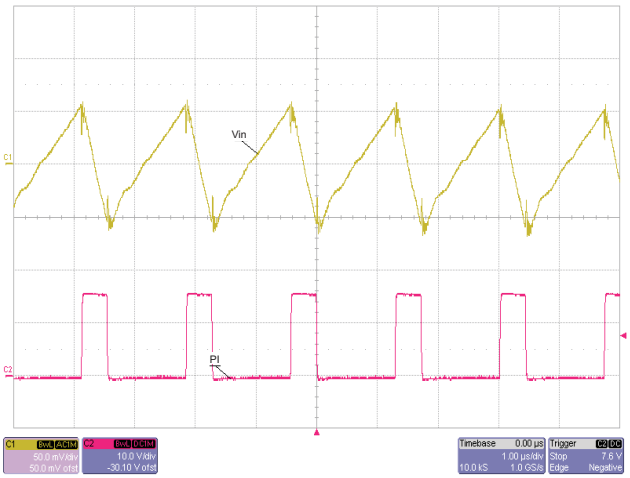


Figure 18. Input Ripple

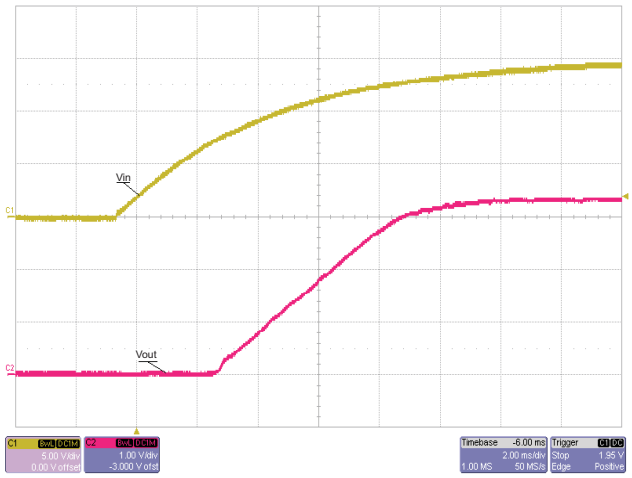


Figure 19. Startup

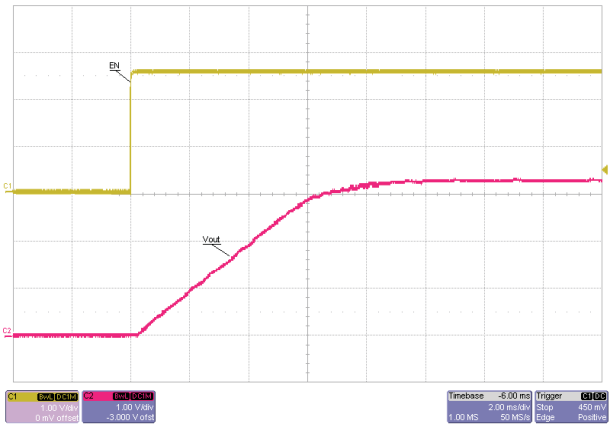


Figure 20. Startup Relative to Enable

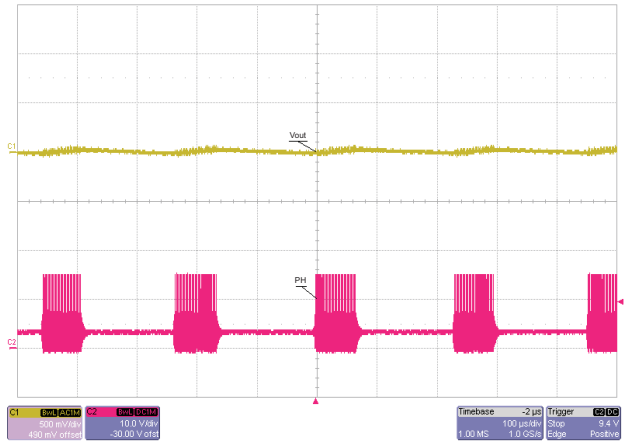


Figure 21. Eco-mode

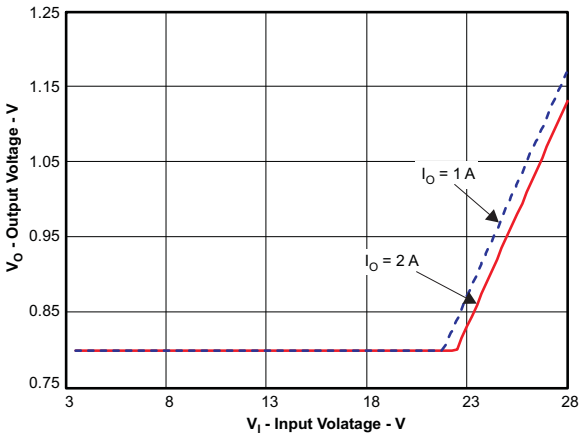


Figure 22. Typical Minimum Output Voltage vs Input Voltage

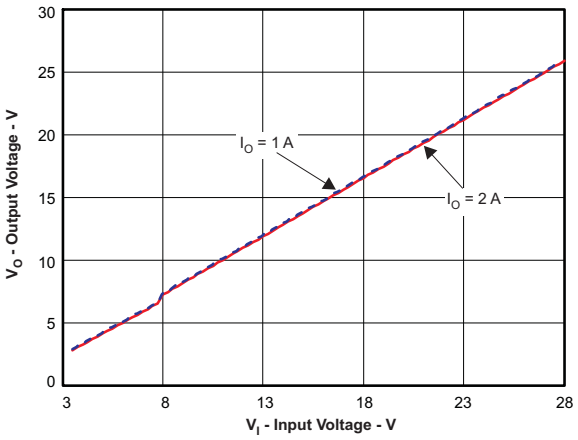


Figure 23. Typical Maximum Output Voltage vs Input Voltage

10 Power Supply Recommendations

The device is designed to operate from an input-voltage supply range between 3.5 V and 28 V. This input supply should be well regulated. If the input supply is located more than a few inches from the converter additional bulk capacitance may be required in addition to the ceramic bypass capacitors. An electrolytic capacitor with a value of 100 µF is a typical choice.

11 Layout

11.1 Layout Guidelines

The VIN pin should be bypassed to ground with a low-ESR ceramic bypass capacitor. Care should be taken to minimize the loop area formed by the bypass capacitor connections, the VIN pin, and the anode of the catch diode. The typical recommended bypass capacitance is 10-µF ceramic with a X5R or X7R dielectric and the optimum placement is closest to the VIN pins and the source of the anode of the catch diode. Figure 24 shows a PCB layout example. The GND pin should be tied to the PCB ground plane at the pin of the IC. The source of the low-side MOSFET should be connected directly to the top side PCB ground area used to tie together the ground sides of the input and output capacitors as well as the anode of the catch diode. The PH pin should be routed to the cathode of the catch diode and to the output inductor. Because the PH connection is the switching node, the catch diode and output inductor should be located very close to the PH pins, and the area of the PCB conductor minimized to prevent excessive capacitive coupling. For operation at full rated load, the top-side ground area must provide adequate heat dissipating area. The TPS54231 device uses a fused lead frame so that the GND pin acts as a conductive path for heat dissipation from the die. Many applications have larger areas of internal or back-side ground plane available, and the top-side ground area can be connected to these areas using multiple vias under or adjacent to the device to help dissipate heat. The additional external components can be placed approximately as shown. Obtain acceptable performance with alternate layout schemes may be possible, however this layout has been shown to produce good results and is intended as a guideline.

11.2 Layout Example

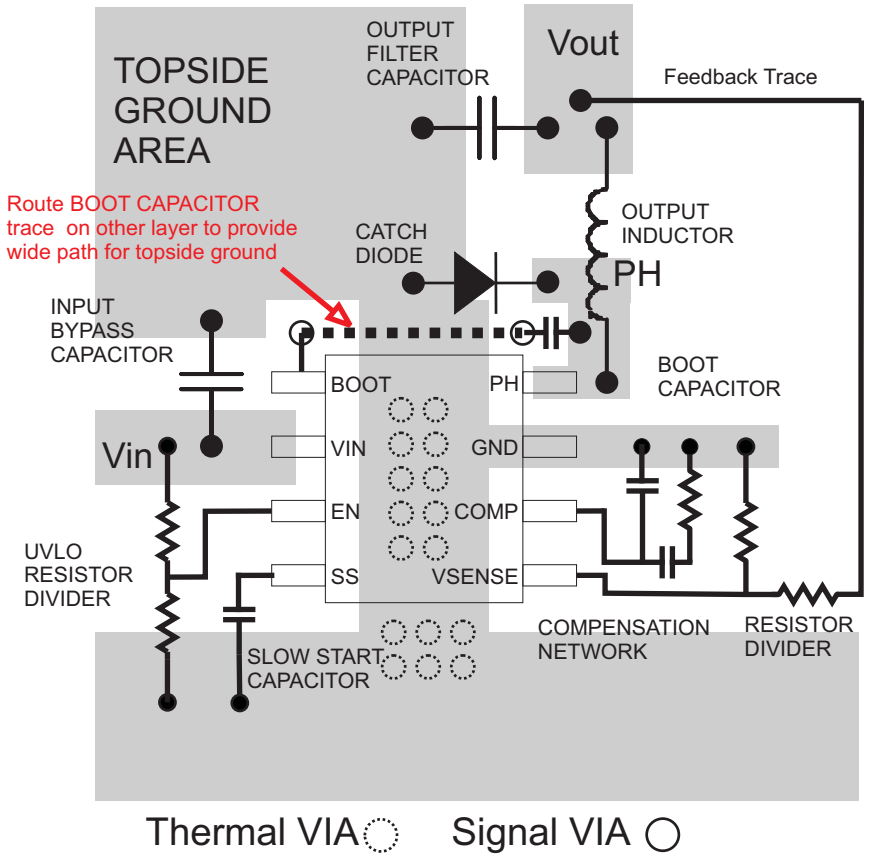


Figure 24. TPS54231 device Board Layout

11.3 Estimated Circuit Area

The estimated printed circuit board area for the components used in the design of Figure 10 is 0.68 in^2. This area does not include test points or connectors.

11.4 Electromagnetic Interference (EMI) Considerations

As EMI becomes a rising concern in more and more applications, the internal design of the TPS54231 device takes measures to reduce the EMI. The high-side MOSFET gate drive is designed to reduce the PH pin voltage ringing. The internal IC rails are isolated to decrease the noise sensitivity. A package bond wire scheme is used to lower the parasitics effects.

To achieve the best EMI performance, external component selection and board layout are equally important. Follow the steps listed in the *Detailed Design Procedure* section to prevent potential EMI issues.

12 Device and Documentation Support

12.1 Device Support

12.1.1 Development Support

For the WEBENCH Software Tool, go to www.TI.com/WEBENCH.

12.2 Trademarks

Eco-mode, SWIFT, PowerPAD are trademarks of Texas Instruments.
WEBENCH is a registered trademark of Texas Instruments.
All other trademarks are the property of their respective owners.

12.3 Electrostatic Discharge Caution

These devices have limited built-in ESD protection. The leads should be shorted together or the device placed in conductive foam during storage or handling to prevent electrostatic damage to the MOS gates.

12.4 Glossary

SLYZ022 — *TI Glossary*.

This glossary lists and explains terms, acronyms, and definitions.

13 Mechanical, Packaging, and Orderable Information

The following pages include mechanical, packaging, and orderable information. This information is the most current data available for the designated devices. This data is subject to change without notice and revision of this document. For browser-based versions of this data sheet, refer to the left-hand navigation.

PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead finish/ Ball material (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
TPS54231D	ACTIVE	SOIC	D	8	75	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-40 to 150	54231	Samples
TPS54231DR	ACTIVE	SOIC	D	8	2500	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-40 to 150	54231	Samples
TPS54231DRG4	ACTIVE	SOIC	D	8	2500	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-40 to 150	54231	Samples

(1) The marketing status values are defined as follows:
ACTIVE: Product device recommended for new designs.
LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
PREVIEW: Device has been announced but is not in production. Samples may or may not be available.
OBSOLETE: TI has discontinued the production of the device.

(2) **RoHS:** TI defines "RoHS" to mean semiconductor products that are compliant with the current EU RoHS requirements for all 10 RoHS substances, including the requirement that RoHS substance do not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, "RoHS" products are suitable for use in specified lead-free processes. TI may reference these types of products as "Pb-Free".
RoHS Exempt: TI defines "RoHS Exempt" to mean products that contain lead but are compliant with EU RoHS pursuant to a specific EU RoHS exemption.
Green: TI defines "Green" to mean the content of Chlorine (Cl) and Bromine (Br) based flame retardants meet JS709B low halogen requirements of <=1000ppm threshold. Antimony trioxide based flame retardants must also meet the <=1000ppm threshold requirement.

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

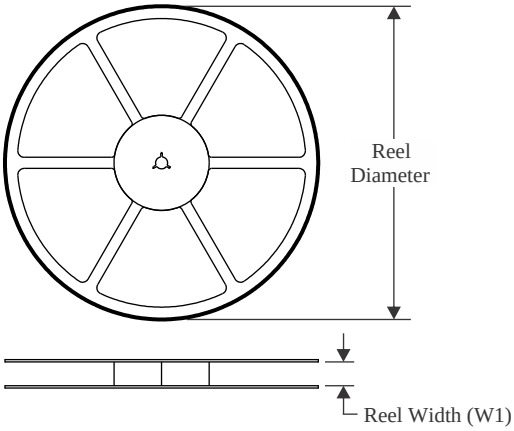
(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

(6) Lead finish/Ball material - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

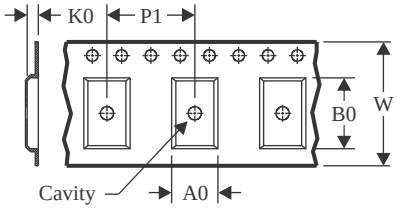
In no event shall TI's liability arising out of such information exceed the total purchase price of the TI part(s) at issue in this document sold by TI to Customer on an annual basis.

TAPE AND REEL INFORMATION

REEL DIMENSIONS

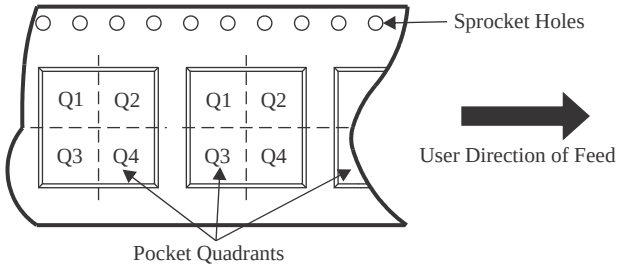


TAPE DIMENSIONS



A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

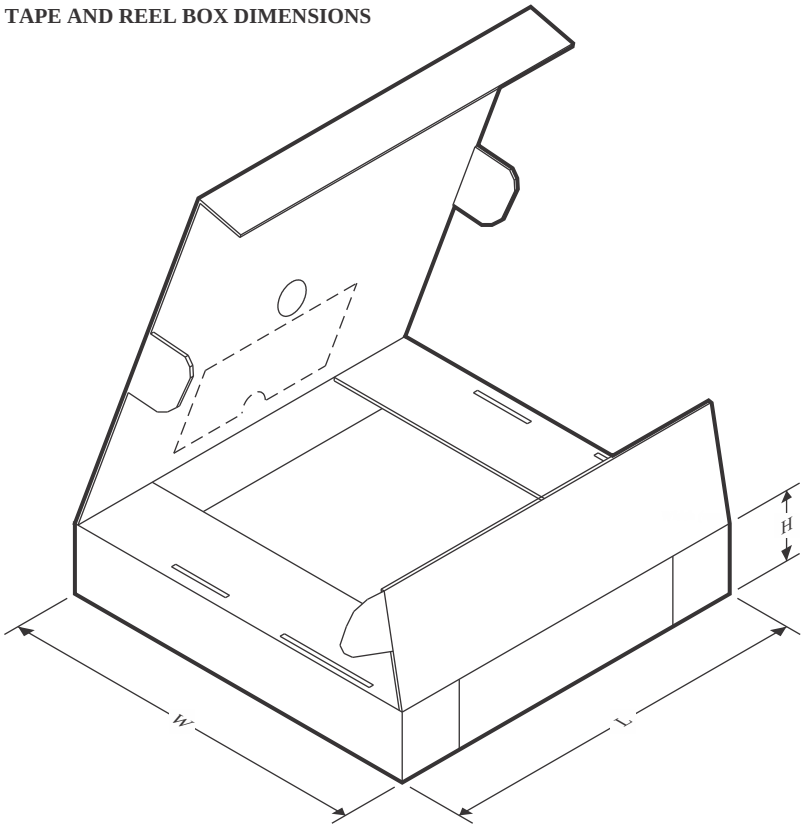
QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
TPS54231DR	SOIC	D	8	2500	330.0	12.5	6.4	5.2	2.1	8.0	12.0	Q1

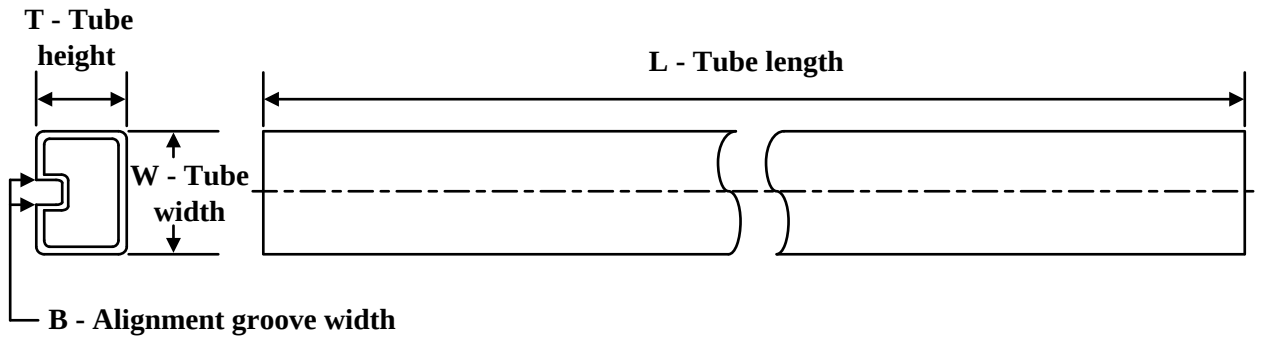
TAPE AND REEL BOX DIMENSIONS



*All dimensions are nominal

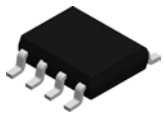
Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
TPS54231DR	SOIC	D	8	2500	353.0	353.0	32.0

TUBE



*All dimensions are nominal

Device	Package Name	Package Type	Pins	SPQ	L (mm)	W (mm)	T (µm)	B (mm)
TPS54231D	D	SOIC	8	75	507	8	3940	4.32

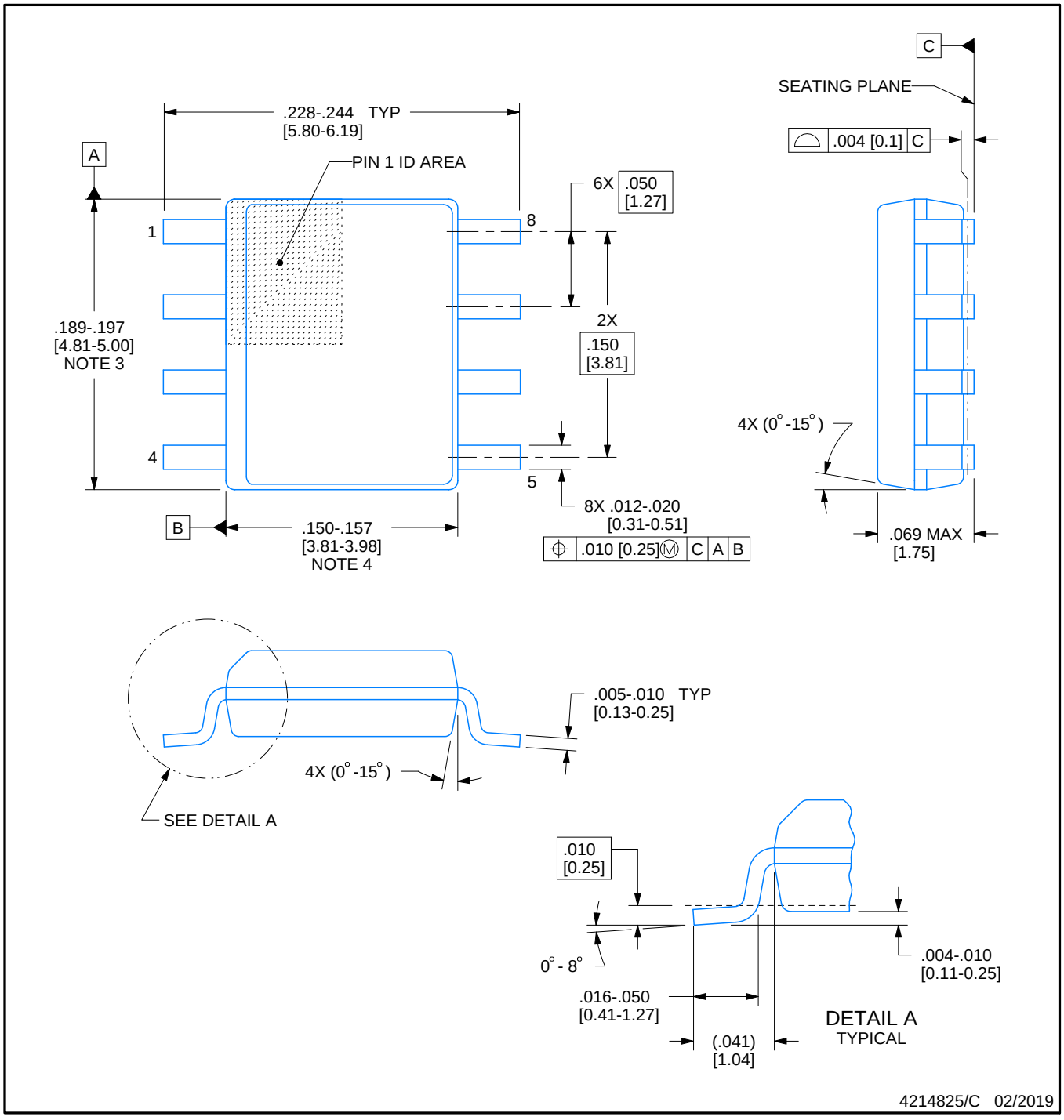


PACKAGE OUTLINE

D0008A

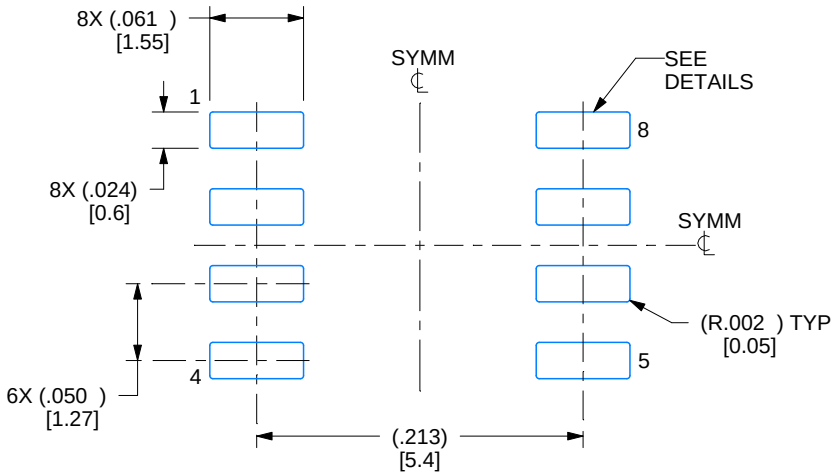
SOIC - 1.75 mm max height

SMALL OUTLINE INTEGRATED CIRCUIT

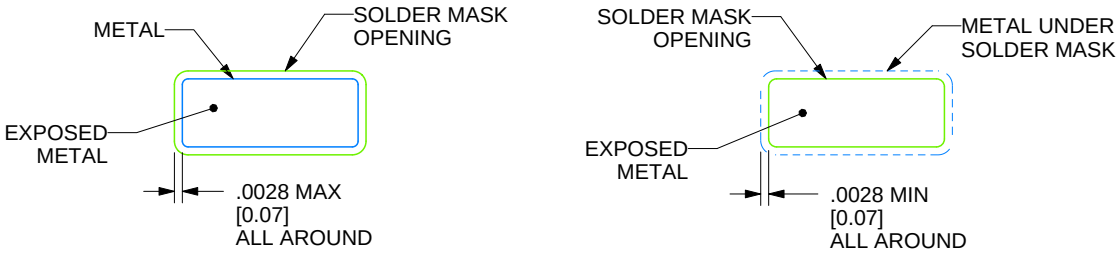


NOTES:

1. Linear dimensions are in inches [millimeters]. Dimensions in parenthesis are for reference only. Controlling dimensions are in inches. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed .006 [0.15] per side.
4. This dimension does not include interlead flash.
5. Reference JEDEC registration MS-012, variation AA.



LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE:8X



SOLDER MASK DETAILS

4214825/C 02/2019

NOTES: (continued)

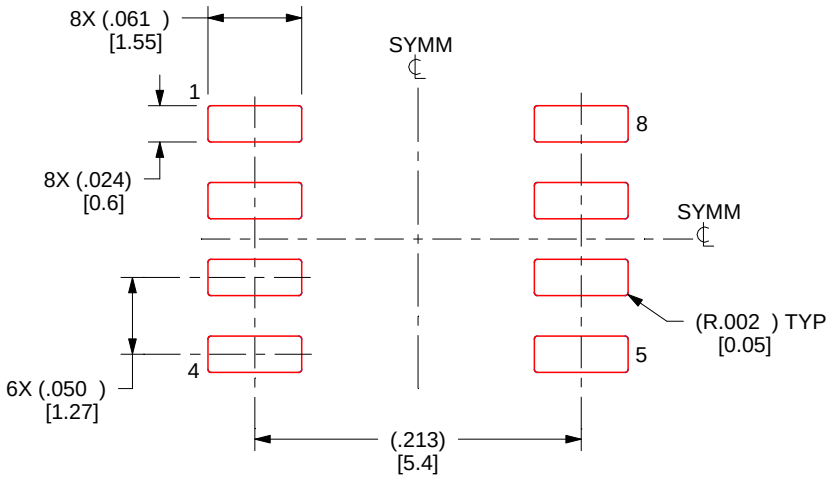
6. Publication IPC-7351 may have alternate designs.
7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.

EXAMPLE STENCIL DESIGN

D0008A

SOIC - 1.75 mm max height

SMALL OUTLINE INTEGRATED CIRCUIT



SOLDER PASTE EXAMPLE
BASED ON .005 INCH [0.125 MM] THICK STENCIL
SCALE:8X

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NOTES: (continued)

8. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
9. Board assembly site may have different recommendations for stencil design.

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Mailing Address: Texas Instruments, Post Office Box 655303, Dallas, Texas 75265