TPS548A20 1.5-V to 20-V (4.5-V to 25-V Bias) Input, 15-A Synchronous Step-Down SWIFT™ Converter

1 Features

- Integrated SWIFT™ 9.9-mΩ and 4.3-mΩ MOSFETs Support 15-A Continuous I_{OUT}
- Wide Conversion Input Voltage Range: 1.5 V to 20 V (with Snubber)
- Output Voltage Range from 0.6 V to 5.5 V
- Supports All Ceramic Output Capacitors
- Reference Voltage: 600 mV with ±0.5% Tolerance from –40°C to 85°C ambient temperature
- D-CAP3™ Control Mode With Fast Load-Step Response
- Hiccup Over Current Protection
- Auto-Skipping Eco-Mode™ for High Light-Load Efficiency
- FCCM for Tight Output Ripple and Voltage Tolerance Requirements
- Pre-charged Startup Capability
- Eight Selectable Frequency Settings from 200 kHz to 1 MHz
- 4.5 mm x 3.5 mm, 28-Pin, VQFN-CLIP Package
- Supported at the WEBENCH™ Design Center

2 Applications

- Server, Cloud-Computing, Storage
- Telecom & Networking, Point-of-Load (POL)
- IPCs, Factory Automation, PLC, Test Measurement
- Performance DSPs, FPGAs

3 Description

The TPS548A20 is a small-sized, synchronous buck converter with an adaptive on-time D-CAP3 control mode. The device offers ease-of-use and low bill-of-material count for space-conscious power systems.

This device features high-performance integrated MOSFETs, accurate 0.6-V reference, and an integrated boost switch. Competitive features include very-low external-component count, fast load-transient response, auto-skip mode operation, internal soft-start control, and no requirement for compensation.

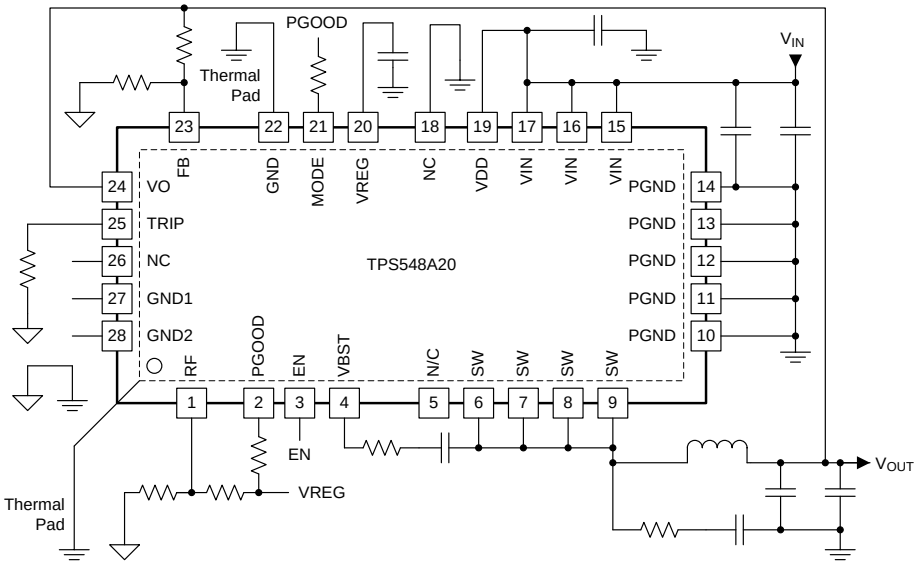
A forced continuous conduction mode helps meet tight voltage regulation accuracy requirements for performance DSPs and FPGAs. The TPS548A20 is available in a 28-pin VQFN-CLIP package and is specified from –40°C to 125°C ambient temperature.

Device Information(1)

PART NUMBER	PACKAGE	BODY SIZE (NOM)
TPS548A20	VQFN-CLIP (28)	4.50 mm x 3.50 mm

(1) For all available packages, see the orderable addendum at the end of the datasheet.

Simplified Application



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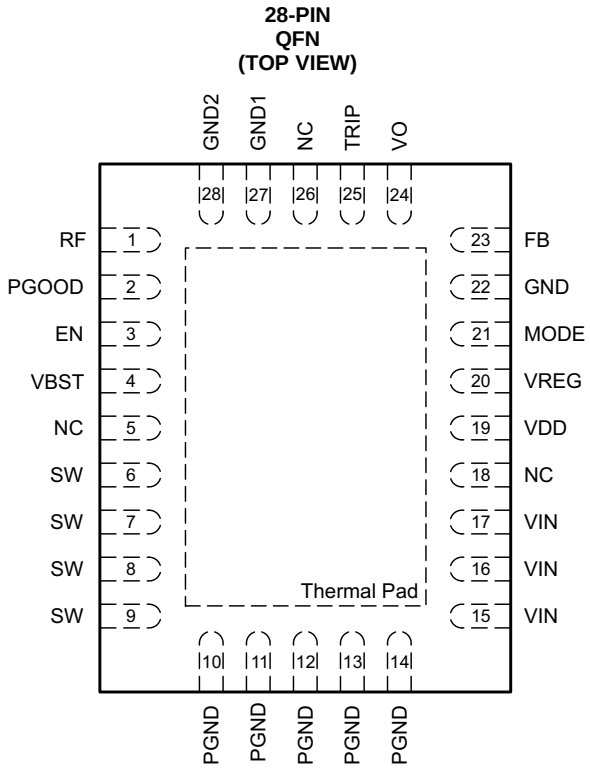
4 Revision History

Changes from Original (October 2015) to Revision A **Page**

- Updated document status from *Product Preview* to *Production Data* ... 1

5 Pin Configuration and Functions



Pin Functions

PIN		I/O(1)	DESCRIPTION
NAME	NO.		
EN	3	I	The enable pin turns on the DC-DC switching converter.
FB	23	I	V_{OUT} feedback input. Connect this pin to a resistor divider between the VOUT pin and GND.
GND	22	G	This pin is the ground of internal analog circuitry and driver circuitry. Connect GND to the PGND plane with a short trace (For example, connect this pin to the thermal pad with a single trace and connect the thermal pad to PGND pins and PGND plane).
GND1	27	G	Connect this pin to ground. GND1 is the input of unused internal circuitry and must connect to ground.
GND2	28		
MODE	21	I	The MODE pin sets the forced continuous-conduction mode (FCCM) or auto-skip mode operation. It also selects the ramp coefficient of D-CAP3 mode.
NC	5	—	Not connected. These pins are floating internally.
	18		
	26		
PGND	10	G	These ground pins are connected to the return of the internal low-side MOSFET.
	11		
	12		
	13		
	14		
PGOOD	2	O	Open-drain power-good status signal which provides startup delay after the FB voltage falls within the specified limits. After the FB voltage moves outside the specified limits, PGOOD goes low within 2 µs.
RF	1	I	

(1) I = Input, O = Output, P = Supply, G = Ground

Pin Functions (continued)

PIN		I/O[1]	DESCRIPTION
NAME	NO.		
SW	6	I/O	SW is the output switching terminal of the power converter. Connect this pin to the output inductor.
	7		
	8		
	9		
TRIP	25	I/O	TRIP is the OCL detection threshold setting pin. I_{TRIP} = 10 µA at T_A = 25°C, 3000 ppm/°C current is sourced and sets the OCL trip voltage. See the *Current Sense and Overcurrent Protection* section for detailed OCP setting.
VBST	4	P	VBST is the supply rail for the high-side gate driver (boost terminal). Connect the bootstrap capacitor from this pin to the SW node. Internally connected to VREG via bootstrap PMOS switch.
VDD	19	P	Power-supply input pin for controller. Input of the VREG LDO. The input range is from 4.5 to 25 V.
VIN	15	P	VIN is the conversion power-supply input pins.
	16		
	17		
VREG	20	O	VREG is the 5-V LDO output. This voltage supplies the internal circuitry and gate driver.
VO	24	I	VOUT voltage input to the controller.

6 Specifications

6.1 Absolute Maximum Ratings

over operating free-air temperature range (unless otherwise noted)[1]

			MIN	MAX	UNIT
Input voltage range[2]	EN		–0.3	7.7	V
	SW	DC	–3	25	
		Transient < 10 ns	–5	27	
	VBST		–0.3	31	
	VBST[3]		–0.3	6	
	VBST when transient < 10 ns			33	
	VDD		–0.3	28	
	VIN		–0.3	25	
	FB, MODE, VO		–0.3	6	
Output voltage range	PGOOD		–0.3	7.7	V
	TRIP, VREG		–0.3	6	
Junction temperature, T_J			–40	150	°C
Storage temperature, T_{stg}			–55	150	°C

(1) Stresses beyond those listed under *Absolute Maximum Ratings* may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under *Recommended Operating Conditions* is not implied. Exposure to absolute-maximum-rated conditions for extended periods my affect device reliability.
(2) All voltages are with respect to network ground terminal.
(3) Voltage values are with respect to the SW terminal.

6.2 ESD Ratings

			VALUE	UNIT
$V_{(ESD)}$	Electrostatic discharge	Human-body model (HBM), per ANSI/ESDA/JEDEC JS-001[1]	±2500	V
		Charged-device model (CDM), per JEDEC specification JESD22-C101[2]	±1500	

(1) JEDEC document JEP155 states that 500-V HBM allows safe manufacturing with a standard ESD control process.
(2) JEDEC document JEP157 states that 250-V CDM allows safe manufacturing with a standard ESD control process.

6.3 Recommended Operating Conditions

over operating free-air temperature range (unless otherwise noted)

		MIN	MAX	UNIT
Input voltage range	EN	–0.1	7	V
	SW	–3	20	
	VBST	–0.1	25.5	
	VBST(1)	–0.1	5.5	
	VDD	4.5	25	
	VIN	1.5	20	
	FB, MODE, VO	–0.1	5.5	
Output voltage range	PGOOD	–0.1	7	V
	TRIP, VREG	–0.1	5.5	
Ambient temperature, T_A		–40	125	°C

(1) Voltage values are with respect to the SW pin.

6.4 Electrical Characteristics

over operating free-air temperature range, VDD = 12V, V_{REG} = 5 V, V_{EN} = 5 V (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
SUPPLY CURRENT						
I_{VDD}	VDD bias current	T_A = 25°C, No load Power conversion enabled (no switching)		1350	1850	µA
$I_{VDDSTBY}$	VDD standby current	T_A = 25°C, No load Power conversion disabled		850	1150	µA
$I_{VIN(leak)}$	VIN leakage current	T_A = 25°C, V_{EN} = 0 V			0.5	µA
VREF OUTPUT						
V_{VREF}	Reference voltage	FB w/r/t GND, T_A = 25°C	597	600	603	mV
$V_{VREFTOL}$	Reference voltage tolerance	FB w/r/t GND, -40°C ≤ T_J ≤ 85°C	–0.5		0.5	%
		FB w/r/t GND, –40°C ≤ T_J ≤ 125°C	–1.0		1.0	
OUTPUT VOLTAGE						
I_{FB}	FB input current	V_{FB} = 600 mV		50	100	nA
I_{VODIS}	VO discharge current	V_{VO} = 0.5 V, Power Conversion Disabled		6		uA
SMPS FREQUENCY						
f_{SW}	VO switching frequency	V_{IN} = 12 V, V_{VO} = 3.3 V, R_{RF}<0.041		250		kHz
		V_{IN} = 12 V, V_{VO} = 3.3 V, R_{RF}=0.096		300		
		V_{IN} = 12 V, V_{VO} = 3.3 V, R_{RF}=0.16		400		
		V_{IN} = 12 V, V_{VO} = 3.3 V, R_{RF}=0.229		500		
		V_{IN} = 12 V, V_{VO} = 3.3 V, R_{RF}=0.297		600		
		V_{IN} = 12 V, V_{VO} = 3.3 V, R_{RF}=0.375		750		
		V_{IN} = 12 V, V_{VO} = 3.3 V, R_{RF}=0.461		850		
		V_{IN} = 12 V, V_{VO} = 3.3 V, R_{RF}>0.557		1000		
$t_{ON(min)}$	Minimum on-time	T_A = 25°C(1)		60		ns
$t_{OFF(min)}$	Minimum off-time	T_A = 25°C	175	240	310	ns
INTERNAL BOOTSTRAP SW						
V_F	Forward Voltage	$V_{VREG–VBST}$, T_A = 25°C, I_F = 10 mA		0.15	0.25	V
I_{VBST}	VBST leakage current	T_A = 25°C, V_{VBST} = 33 V, V_{SW} = 28 V		0.01	1.5	µA

(1) Specified by design. Not production tested.

Electrical Characteristics (continued)

over operating free-air temperature range, VDD = 12V, V_{REG} = 5 V, V_{EN} = 5 V (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
LOGIC THRESHOLD						
V_{ENH}	EN enable threshold voltage		1.3	1.4	1.5	V
V_{ENL}	EN disable threshold voltage		1.1	1.2	1.3	V
V_{ENHYST}	EN hysteresis voltage			0.22		V
V_{ENLEAK}	EN input leakage current		–1	0	1	µA
SOFT-START						
t_{SS}	Soft-start time			4		ms
POWERGOOD COMPARATOR						
V_{PGTH}	PGOOD threshold	PGOOD in from higher	104	108	111	%
		PGOOD in from lower	89	92	96	%
		PGOOD out to higher	113	116	120	%
		PGOOD out to lower	80	84	87	%
t_{PGDLY}	PGOOD delay time	Delay for PGOOD going in	0.8	1.0	1.2	ms
		Delay for PGOOD coming out		2		µs
I_{PG}	PGOOD sink current	V_{PGOOD} = 0.5 V	4	6		mA
I_{PGLK}	PGOOD leakage current	V_{PGOOD} = 5.0 V	–1	0	1	µA
POWER-ON DELAY						
t_{PODLY}	Power-on delay time	Delay from enable to switching		1.124		ms
CURRENT DETECTION						
I_{OCL}	Current limit threshold, valley	R_{TRIP} = 49 kΩ	11.5	15.0	17.5	A
		R_{TRIP} = 28 kΩ	6.5	8	11	
I_{OCLN}	Negative current limit threshold, valley	R_{TRIP} = 49 kΩ	-18.0	–14.9	-10.5	A
		R_{TRIP} = 28 kΩ	-11.5	-8.0	-6.0	
V_{ZC}	Zero cross detection offset			0		mV
PROTECTIONS						
$V_{VREGUVLO}$	VREG undervoltage-lockout (UVLO) threshold voltage	Wake-up	3.25	3.34	3.41	V
		Shutdown	3.00	3.12	3.19	
$V_{VDDUVLO}$	VDD UVLO threshold voltage	Wake-up (default)	4.15	4.25	4.35	V
		Shutdown	3.95	4.05	4.15	
V_{OVP}	Overvoltage-protection (OVP) threshold voltage	OVP detect voltage	116	120	124	%
t_{OVPDLY}	OVP propagation delay	With 100-mV overdrive		300		ns
V_{UVP}	Undervoltage-protection (UVP) threshold voltage	UVP detect voltage	64	68	71	%
t_{UVPDLY}	UVP delay	UVP filter delay		1		ms
THERMAL SHUTDOWN						
T_{SDN}	Thermal shutdown threshold(1)	Shutdown temperature		140		°C
		Hysteresis		40		
LDO VOLTAGE						
V_{REG}	LDO output voltage	V_{IN} = 12 V, I_{LOAD} = 10 mA	4.65	5	5.45	V
V_{DOVREG}	LDO low droop drop-out voltage	V_{IN} = 4.5 V, I_{LOAD} = 30 mA, T_A = 25°C			365	mV
I_{LDOMAX}	LDO over-current limit	V_{IN} = 12 V, T_A = 25°C	170	200		mA
INTERNAL MOSFETS						
$R_{DS(on)H}$	High-side MOSFET on-resistance	T_A = 25°C		9.9	11.4	mΩ
$R_{DS(on)L}$	Low-side MOSFET on-resistance	T_A = 25°C		4.3	4.94	mΩ

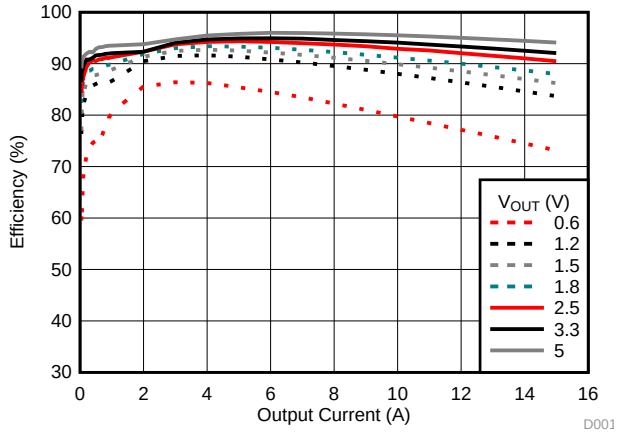
6.5 Thermal Information

THERMAL METRIC[1]		TPS548A20 RVE (VQFN-CLIP) 28 PINS	UNIT
θ_{JA}	Junction-to-ambient thermal resistance	37.5	°C/W
θ_{JCtop}	Junction-to-case (top) thermal resistance	34.1	°C/W
θ_{JB}	Junction-to-board thermal resistance	18.1	°C/W
ψ_{JT}	Junction-to-top characterization parameter	1.8	°C/W
ψ_{JB}	Junction-to-board characterization parameter	18.1	°C/W
θ_{JCbot}	Junction-to-case (bottom) thermal resistance	2.2	°C/W

(1) For more information about traditional and new thermal metrics, see the *Semiconductor and IC Package Thermal Metrics* application report (SPRA953).

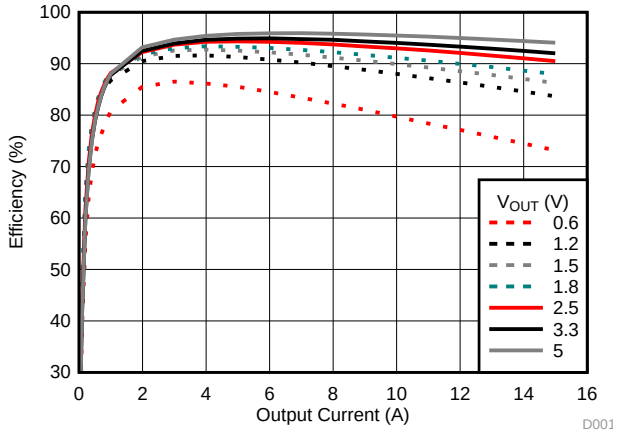
6.6 Typical Characteristics

T_A = 25°C (unless otherwise noted)



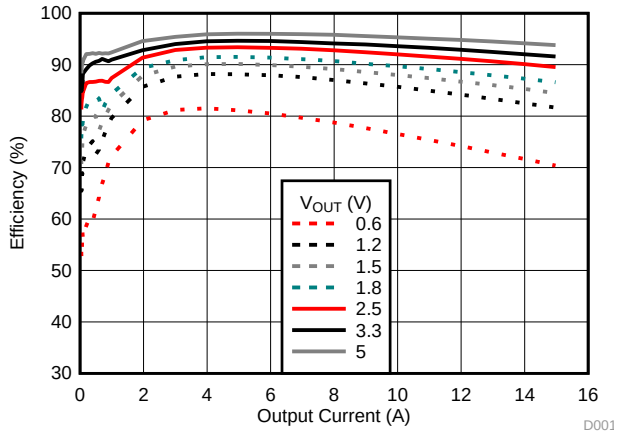
f_{SW} = 500 kHz Auto-skip Mode
V_{IN} = 12 V

Figure 1. Efficiency vs. Output Current



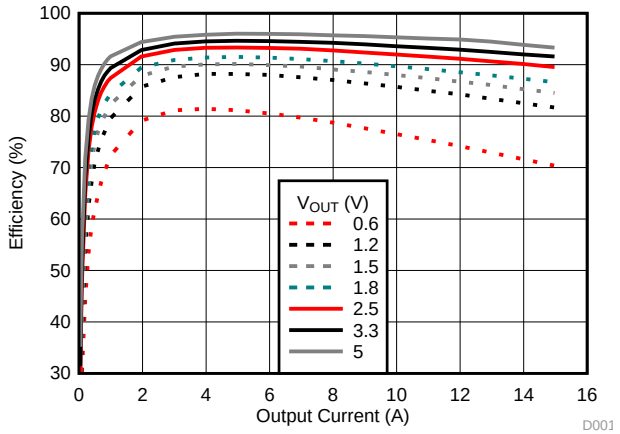
f_{SW} = 500 kHz FCCM
V_{IN} = 12 V

Figure 2. Efficiency vs. Output Current



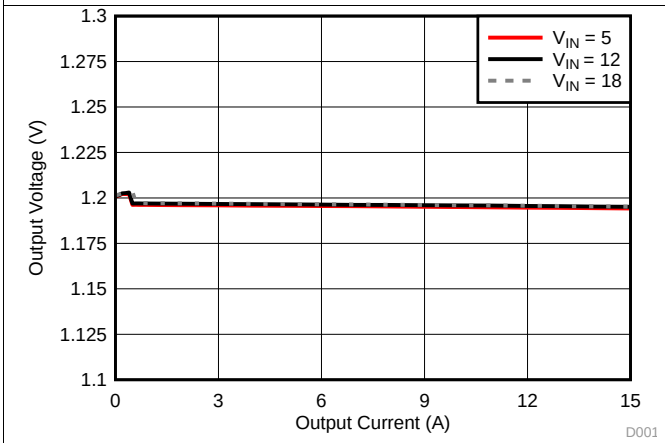
f_{SW} = 970 kHz Auto-skip Mode
V_{IN} = 12 V

Figure 3. Efficiency vs. Output Current



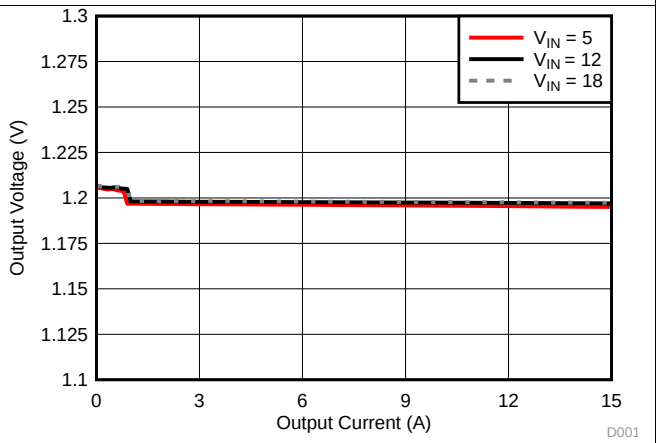
f_{SW} = 970 kHz FCCM
V_{IN} = 12 V

Figure 4. Efficiency vs. Output Current



f_{SW} = 500 kHz V_{OUT} = 1.2 V

Figure 5. DC Load Regulation

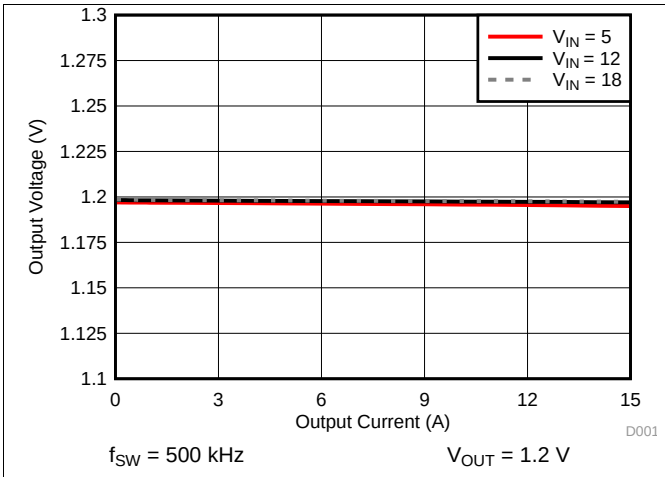


f_{SW} = 970 kHz V_{OUT} = 1.2 V

Figure 6. DC Load Regulation

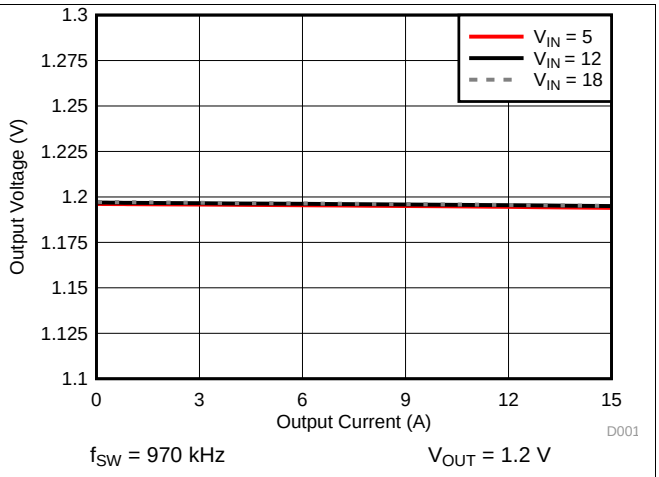
Typical Characteristics (continued)

T_A = 25°C (unless otherwise noted)



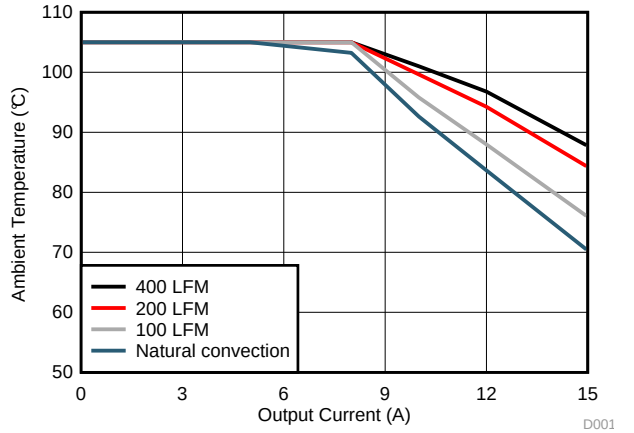
f_{SW} = 500 kHz V_{OUT} = 1.2 V

Figure 7. DC Load Regulation



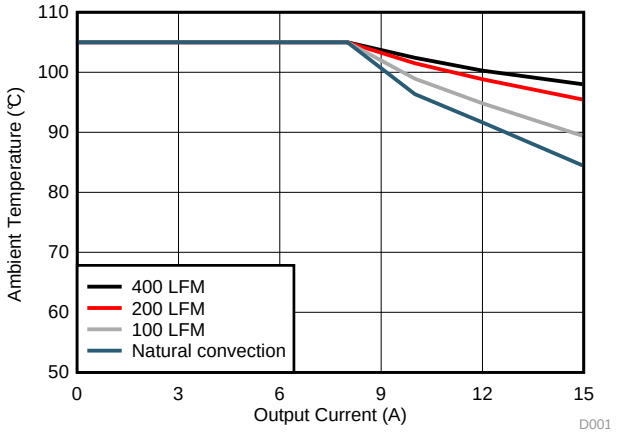
f_{SW} = 970 kHz V_{OUT} = 1.2 V

Figure 8. DC Load Regulation



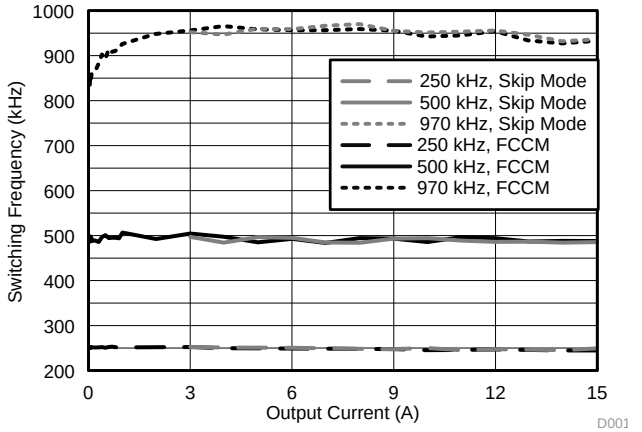
f_{SW} = 500 kHz V_{IN} = 12 V
V_{OUT} = 5 V

Figure 9. Safe Operating Area



f_{SW} = 500 kHz V_{IN} = 12 V
V_{OUT} = 1 V

Figure 10. Safe Operating Area

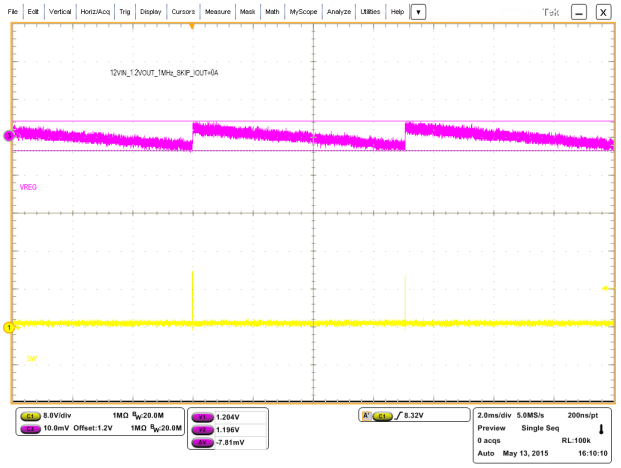


V_{IN} = 12 V V_{OUT} = 1.2 V

Figure 11. Switching Frequency vs. Output Current

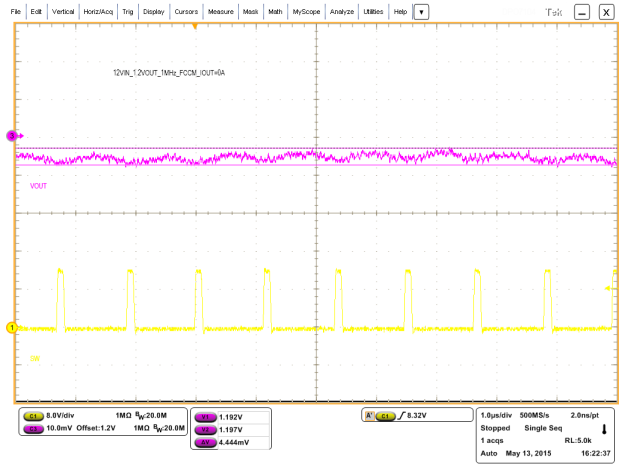
Typical Characteristics (continued)

T_A = 25°C (unless otherwise noted)



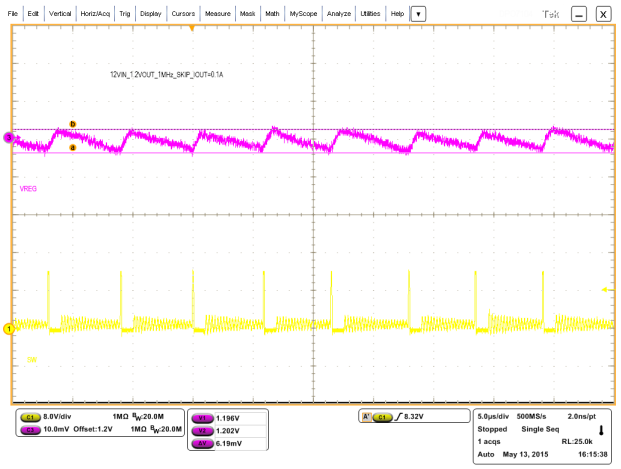
f_{SW} = 1 MHz
V_{OUT} = 1.2 V
V_{IN} = 12 V
I_{LOAD} = 0 A

Figure 12. Skip Mode Steady-State Operation



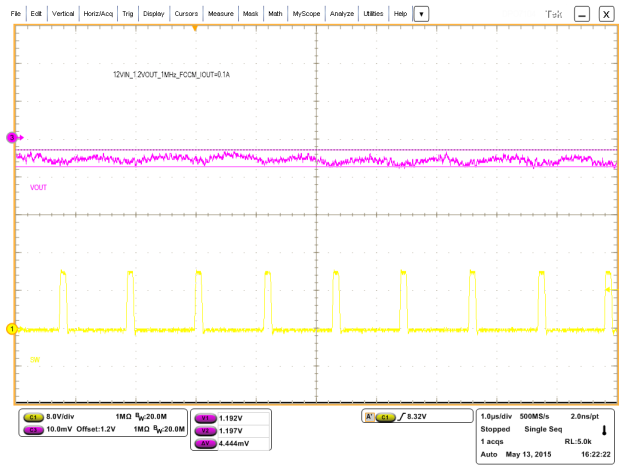
f_{SW} = 1 MHz
V_{OUT} = 1.2 V
V_{IN} = 12 V
I_{LOAD} = 0 A

Figure 13. FCCM Steady-State Operation



f_{SW} = 1 MHz
V_{OUT} = 1.2 V
V_{IN} = 12 V
I_{LOAD} = 0.1 A

Figure 14. Skip Mode Steady-State Operation



f_{SW} = 1 MHz
V_{OUT} = 1.2 V
V_{IN} = 12 V
I_{LOAD} = 0.1 A

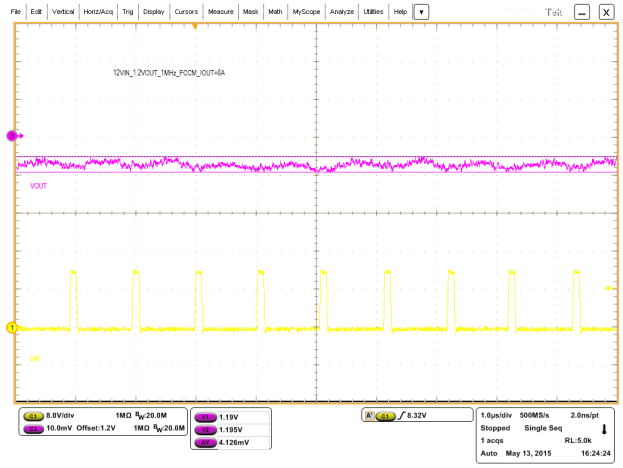
Figure 15. Steady-State Operation

Typical Characteristics (continued)

T_A = 25°C (unless otherwise noted)

f_{SW} = 1 MHz
V_{OUT} = 1.2 V
V_{IN} = 12 V
I_{LOAD} = 8 A

Figure 16. Skip Mode Steady-State Operation

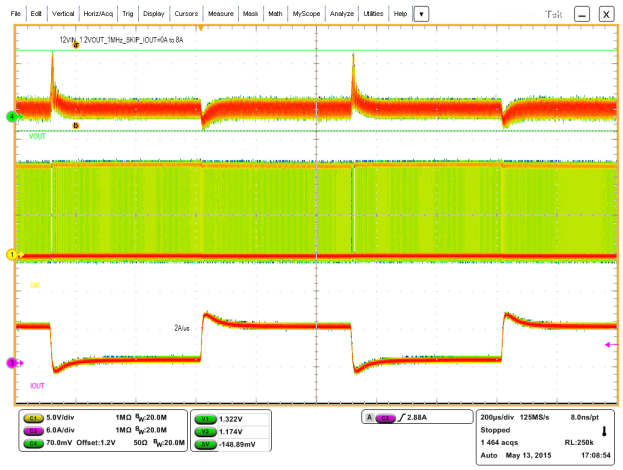


f_{SW} = 1 MHz
V_{OUT} = 1.2 V
V_{IN} = 12 V
I_{LOAD} = 8 A

Figure 17. Skip Mode Steady-State Operation

I_{LOAD} from 0 A to 8 A
V_{IN} = 12 V
f_{SW} = 1 MHz
Div = 2 A/µs
V_{OUT} = 1.2 V

Figure 18. Auto-skip Mode Load Transient

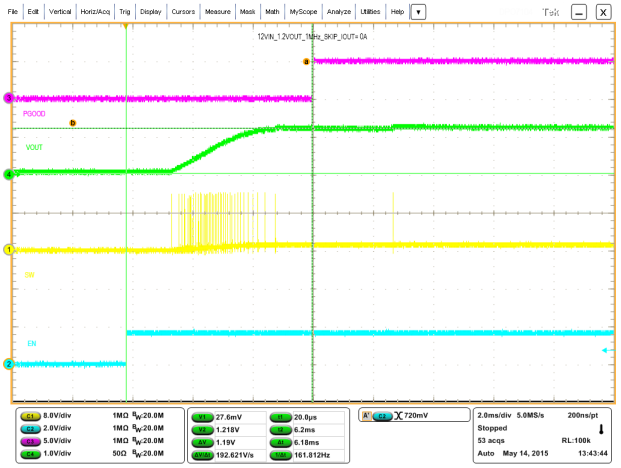


I_{LOAD} from 0 A to 8 A
V_{IN} = 12 V
f_{SW} = 1 MHz
Div = 2 A/µs
V_{OUT} = 1.2 V

Figure 19. Load Transient

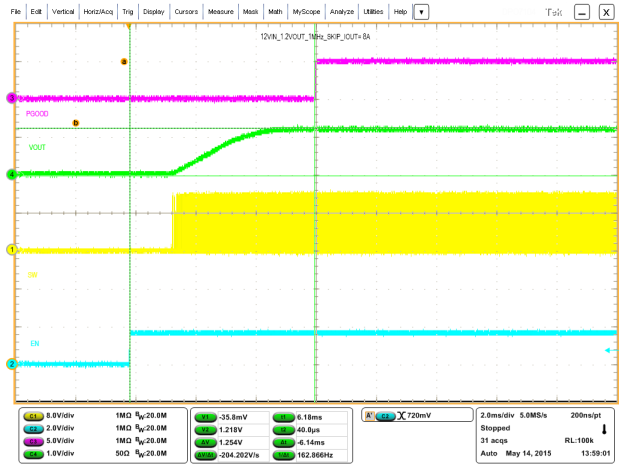
Typical Characteristics (continued)

T_A = 25°C (unless otherwise noted)



f_{SW} = 1 MHz
V_{IN} = 12 V
V_{OUT} = 1.2 V

Figure 20. Auto-skip Mode Start-Up



f_{SW} = 1 MHz
V_{IN} = 12 V
V_{OUT} = 1.2 V

Figure 21. FCCM Mode Start-Up

I_{LOAD} = 0 A
V_{IN} = 12 V
V_{OUT} = 1.2 V
f_{SW} = 1 MHz

Figure 22. Skip Mode Pre-Bias Start-Up

I_{LOAD} = 0 A
V_{IN} = 12 V
V_{OUT} = 1.2 V
f_{SW} = 1 MHz

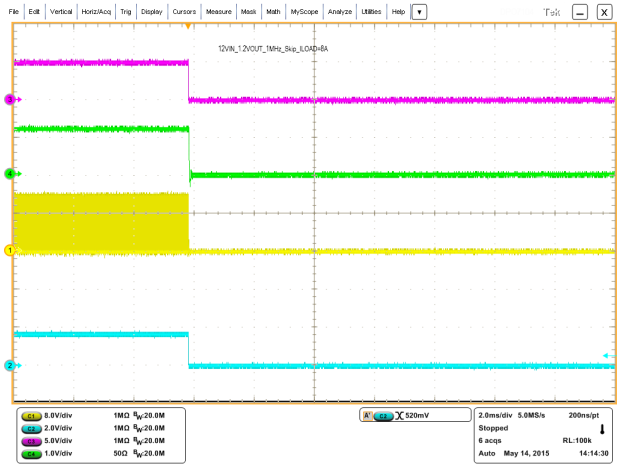
Figure 23. FCCM Pre-Bias Start-Up

Typical Characteristics (continued)

T_A = 25°C (unless otherwise noted)

I_{LOAD} = 8A
V_{OUT} = 1.2 V
V_{IN} = 12 V
f_{SW} = 1 MHz

Figure 24. Auto-skip Mode Shutdown Operation



I_{LOAD} = 8 A
V_{OUT} = 1.2 V
V_{IN} = 12 V
f_{SW} = 1 MHz

Figure 25. Auto-skip Mode Shutdown Operation

I_{LOAD} = 0 A
V_{OUT} = 1.2 V
V_{IN} = 12 V
f_{SW} = 1 MHz

Figure 26. FCCM Shutdown Operation

I_{LOAD} = 8 A
V_{OUT} = 1.2 V
V_{IN} = 12 V
f_{SW} = 1 MHz

Figure 27. FCCM Shutdown Operation

Typical Characteristics (continued)

T_A = 25°C (unless otherwise noted)

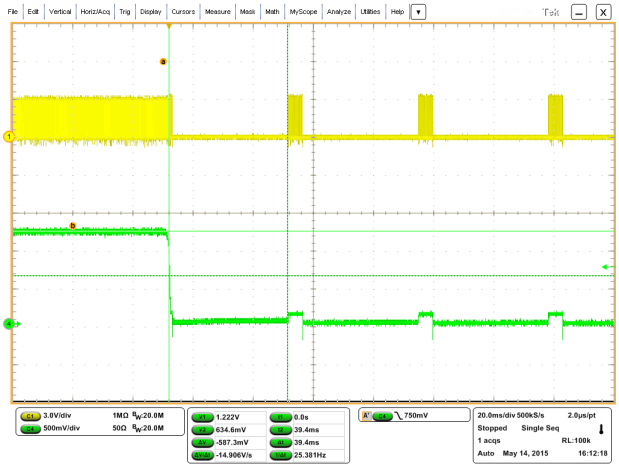


Figure 28. Overcurrent Protection Hiccup

Figure 29. Overcurrent Protection

6.7 Thermal Performance

f_{SW} = 500 kHz, V_{IN} = 12 V, V_{OUT} = 5 V, I_{OUT} = 12 A, C_{OUT} = 10 × 22 µF (1206, 6.3 V, X5R), R_{BOOT} = 0 Ω, SNB = 3 Ω + 470 pF
Inductor: L_{OUT} = 1 µH, PCMC135T-1R0MF, 12.6 mm × 13.8 mm × 5 mm, 2.1 mΩ (typ)

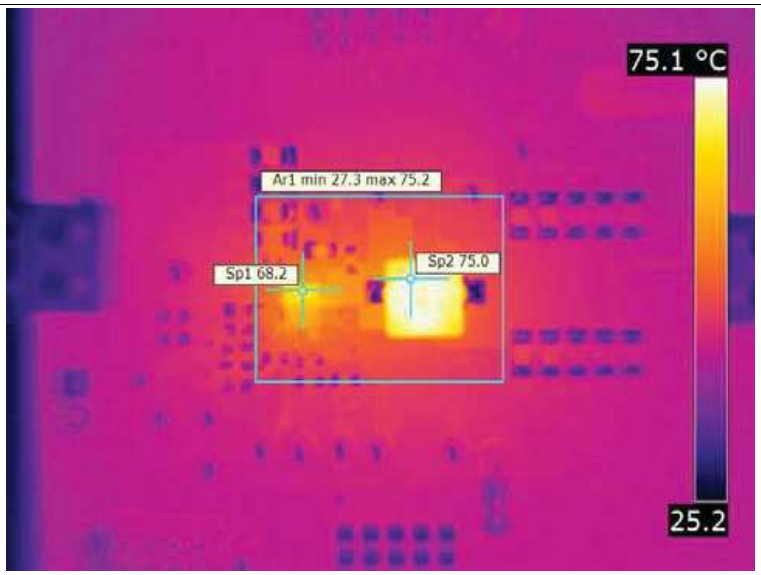


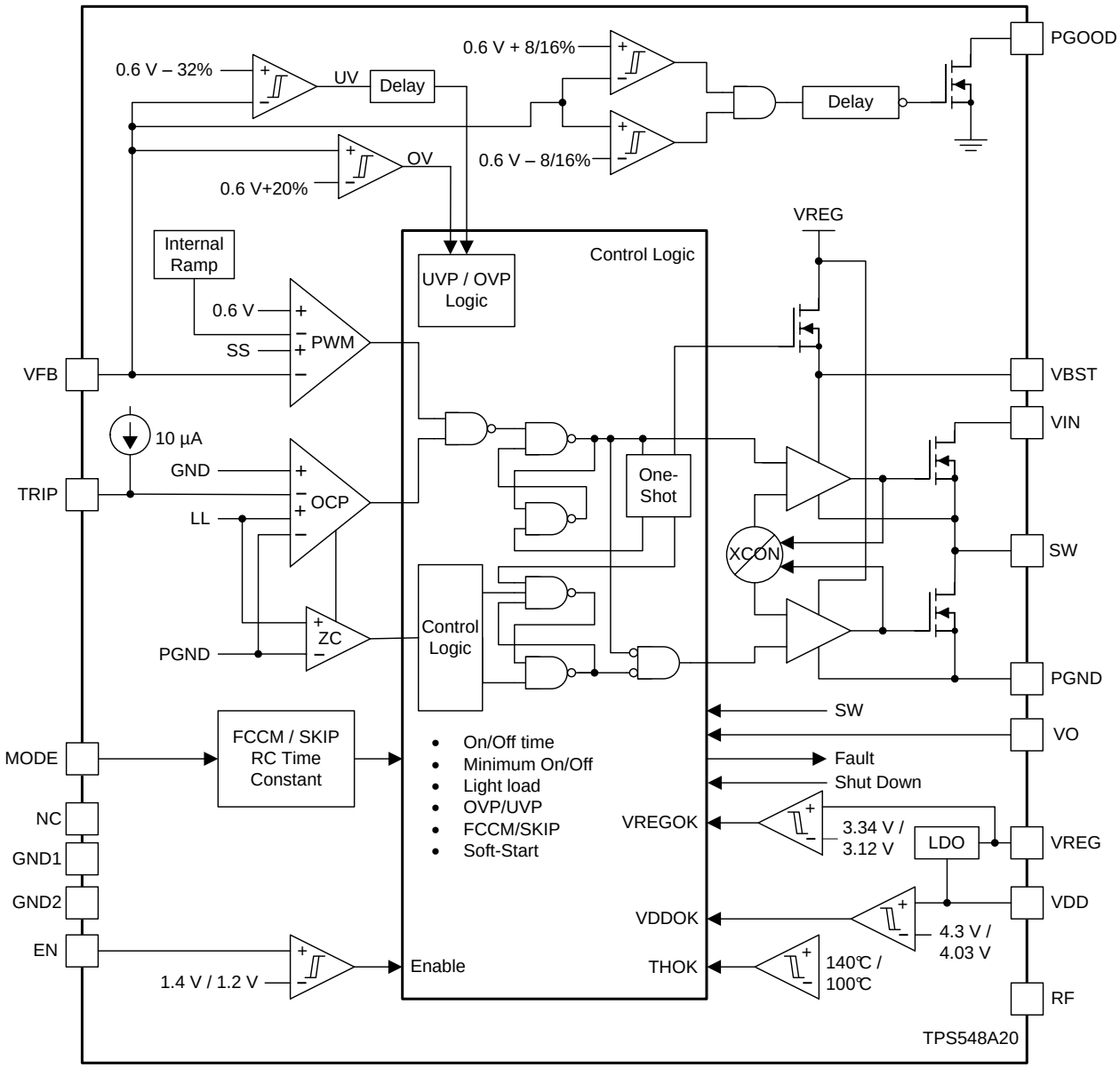
Figure 30. SP1: 68.2℃ (TPS548A20), SP2: 75℃ (Inductor)

7 Detailed Description

7.1 Overview

The TPS548A20 is a high-efficiency, single-channel, synchronous-buck converter. The device suits low-output voltage point-of-load applications with 15-A or lower output current in computing and similar digital consumer applications. The TPS548A20 features proprietary D-CAP3 mode control combined with adaptive on-time architecture. This combination builds modern low-duty-ratio and ultra-fast load-step-response DC-DC converters in an ideal fashion. The output voltage ranges from 0.6 V to 5.5 V. The conversion input voltage ranges from 1.5 V to 20 V (with snubber) and the VDD input voltage ranges from 4.5 V to 25 V. D-CAP3 mode operation uses emulated current information to control the modulation. An advantage of this control scheme is that it does not require a phase-compensation network outside which makes the device easy-to-use and also allows low-external component count. Adaptive on-time control tracks the preset switching frequency over a wide range of input and output voltage while increasing switching frequency as needed during load-step transient.

7.2 Functional Block Diagrams



7.3 Feature Description

7.3.1 Powergood

The TPS548A20 has powergood output that indicates high when switcher output is within the target. The power-good function is activated after the soft-start operation is complete. If the output voltage becomes within ±8% of the target value, internal comparators detect the power-good state and the power-good signal becomes high after a 1-ms internal delay. If the output voltage goes outside of ±16% of the target value, the power-good signal becomes low after a 2-µs internal delay. The power-good output is an open-drain output and must be pulled-up externally.

7.3.2 D-CAP3 Control and Mode Selection

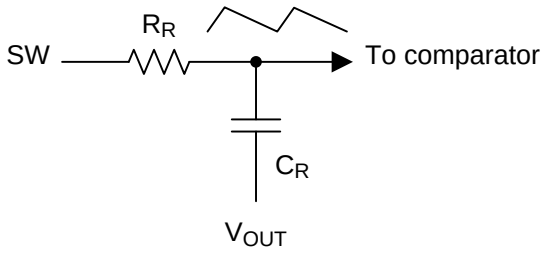


Figure 31. Internal RAMP Generation Circuit

The TPS548A20 uses D-CAP3 mode control to achieve fast load transient while maintaining the ease-of-use feature. An internal RAMP is generated and fed to the VFB pin to reduce jitter and maintain stability. The amplitude of the ramp is determined by the R-C time-constant as shown in Figure 31. At different switching frequencies, (f_{SW}) the R-C time-constant varies to maintain relatively constant RAMP amplitude.

7.3.3 D-CAP3 Mode

From small-signal loop analysis, a buck converter using the D-CAP3 mode control architecture can be simplified as shown in Figure 32.

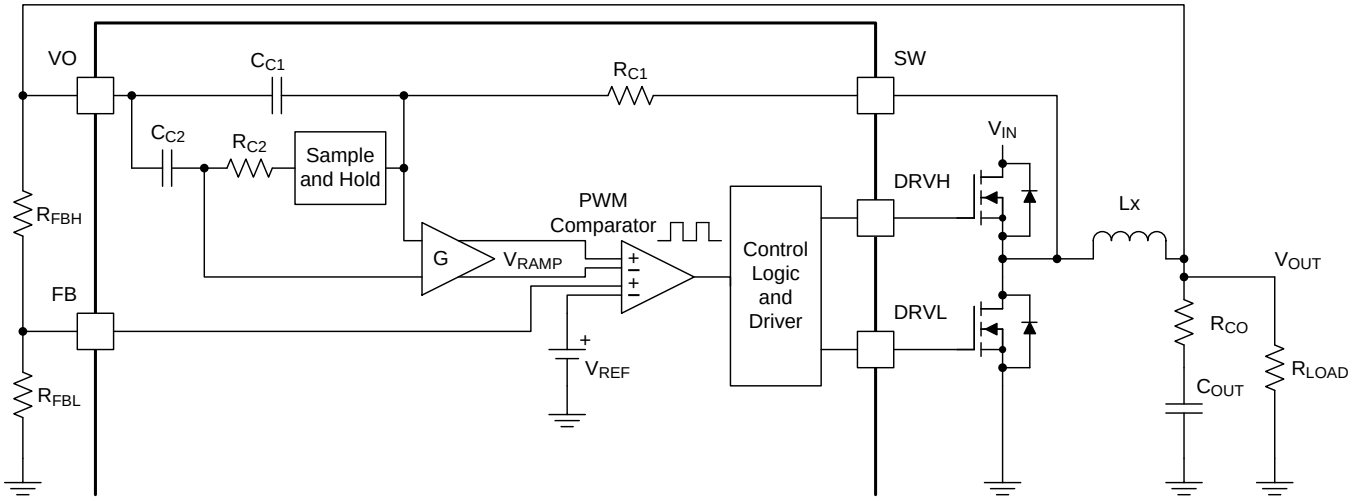


Figure 32. D-CAP3 Mode

Feature Description (continued)

The D-CAP3 control architecture includes an internal ripple generation network enabling the use of very low-ESR output capacitors such as multi-layered ceramic capacitors (MLCC). No external current sensing network or voltage compensators are required with D-CAP3 control architecture. The role of the internal ripple generation network is to emulate the ripple component of the inductor current information and then combine it with the voltage feedback signal to regulate the loop operation. For any control topologies supporting no external compensation design, there is a minimum and/or maximum range of the output filter it can support. The output filter used with the TPS548A20 device is a lowpass L-C circuit. This L-C filter has double pole that is described in Equation 1.

$$f_P = \frac{1}{2 \times \pi \times \sqrt{L_{OUT} \times C_{OUT}}} \quad (1)$$

At low frequencies, the overall loop gain is set by the output set-point resistor divider network and the internal gain of the device. The low frequency L-C double pole has a 180 degree in phase. At the output filter frequency, the gain rolls off at a –40dB per decade rate and the phase drops rapidly. The internal ripple generation network introduces a high-frequency zero that reduces the gain roll off from –40dB to –20dB per decade and increases the phase to 90 degree one decade above the zero frequency.

The inductor and capacitor selected for the output filter must be such that the double pole of Equation 1 is located close enough to the high-frequency zero so that the phase boost provided by the high-frequency zero provides adequate phase margin for the stability requirement.

Table 1. Locating the Zero

SWITCHING FREQUENCIES (f_{SW}) (kHz)	ZERO (f_Z) LOCATION (kHz)
250 and 300	6
400 and 500	7
600 and 750	9
850 and 1000	12

After identifying the application requirements, the output inductance should be designed so that the inductor peak-to-peak ripple current is approximately between 25% and 35% of the $I_{CC(max)}$ (peak current in the application). Use Table 1 to help locate the internal zero based on the selected switching frequency. In general, where reasonable (or smaller) output capacitance is desired, Equation 2 can be used to determine the necessary output capacitance for stable operation.

$$f_P = \frac{1}{2 \times \pi \times \sqrt{L_{OUT} \times C_{OUT}}} = f_Z \quad (2)$$

If MLCC is used, consider the derating characteristics to determine the final output capacitance for the design. For example, when using an MLCC with specifications of 10-µF, X5R and 6.3 V, the deratings by DC bias and AC bias are 80% and 50% respectively. The effective derating is the product of these two factors, which in this case is 40% and 4-µF. Consult with capacitor manufacturers for specific characteristics of the capacitors to be used in the system/applications.

Table 2 shows the recommended output filter range for an application design with the following specifications:

- Input voltage, V_{IN} = 12 V
- Switching frequency, f_{SW} = 600 kHz
- Output current, I_{OUT} = 8 A

The minimum output capacitance is verified by the small signal measurement conducted on the EVM using the following two criteria:

- Loop crossover frequency is less than one-half the switching frequency (300 kHz)
- Phase margin at the loop crossover is greater than 50 degrees

For the maximum output capacitance recommendation, simplify the procedure to adopt an unrealistically high output capacitance for this type of converter design, then verify the small signal response on the EVM using the following one criteria:

- Phase margin at the loop crossover is greater than 50 degrees

As indicated by the phase margin, the actual maximum output capacitance ($C_{OUT(max)}$) can continue to go higher. However, small signal measurement (bode plot) should be done to confirm the design.

Select a MODE pin configuration as shown in Table 3 to double the R-C time constant option for the maximum output capacitance design and application. Select a MODE pin configuration to use single R-C time constant option for the normal (or smaller) output capacitance design and application.

The MODE pin also selects Auto-skip-mode or FCCM-mode operation.

Table 2. Recommended Component Values

V_{OUT} (V)	R_{LOWER} (kΩ)	R_{UPPER} (kΩ)	L_{OUT} (µH)	$C_{OUT(min)}$ (µF) (1)	CROSS-OVER (kHz)	PHASE MARGIN (°)	$C_{OUT(max)}$ (µF) (1)	INTERNAL RC SETTING (µs)	INDUCTOR $\Delta I/I_{CC(max)}$	$I_{CC(max)}$ (A)
0.6	10	0	0.36 PIMB065T-R36MS	3 × 100	247	70		40	33%	8
					48	62	30 x 100	80		
1.2		10	0.68 PIMB065T-R68MS	9 × 22	207	53		40	33%	
					25	84	30 x 100	80		
2.5		31.6	1.2 PIMB065T-1R2MS	4 × 22	185	57		40	34%	
					11	63	30 x 100	80		
3.3		45.3	1.5 PIMB065T-1R5MS	3 × 22	185	57		40	33%	
					9	59	30 x 100	80		
5.5		82.5	2.2 PIMB065T-2R2MS	2 × 22	185	51		40	28%	
					7	58	30 x 100	80		

(1) All $C_{OUT(min)}$ and $C_{OUT(max)}$ capacitor specifications are 1206, X5R, 10 V.

For higher output voltage at or above 2.0 V, additional phase boost might be required in order to secure sufficient phase margin due to phase delay/loss for higher output voltage (large on-time (t_{ON})) setting in a fixed on time topology based operation.

A feedforward capacitor placing in parallel with R_{UPPER} is found to be very effective to boost the phase margin at loop crossover.

Table 3. Mode Selection and Internal RAMP RC Time Constant

MODE SELECTION	ACTION	R_{MODE} (kΩ)	R-C TIME CONSTANT (µs)	SWITCHING FREQUENCIES f_{SW} (kHz)
Auto-skip Mode	Pull down to GND	0	60	275 and 325
			50	425 and 525
			40	625 and 750
			30	850 and 1000
		150	120	275 and 325
			100	425 and 525
			80	625 and 750
			60	850 and 1000
FCCM (1)	Connect to PGOOD	20	60	275 and 325
			50	425 and 525
			40	625 and 750
			30	850 and 1000
		150	120	275 and 325
			100	425 and 525
			80	625 and 750
			60	850 and 1000

(1) Device goes into Forced CCM (FCCM) after PGOOD becomes high.

Table 3. Mode Selection and Internal RAMP RC Time Constant (continued)

MODE SELECTION	ACTION	R_{MODE} (kΩ)	R-C TIME CONSTANT (µs)	SWITCHING FREQUENCIES f_{SW} (kHz)
FCCM	Connect to VREG	0	120	275 and 325
			100	425 and 525
			80	625 and 750
			60	850 and 1000

7.3.4 Sample and Hold Circuitry

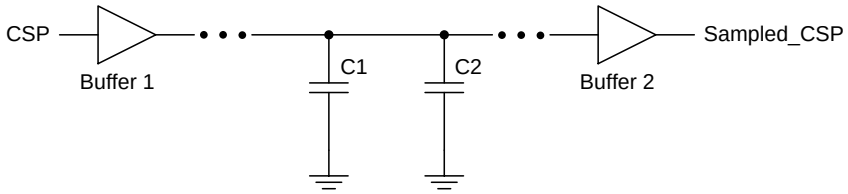


Figure 33. Sample and Hold Circuitry

The sample and hold circuitry is the difference between D-CAP3 and D-CAP2. The sample and hold circuitry, which is an advance control scheme to boost output voltage accuracy higher on the TPS548A20 , is one of features of the TPS548A20 . The sample and hold circuitry generates a new DC voltage of CSN instead of the voltage which is produced by R_{C2} and C_{C2} which allows for tight output-voltage accuracy and makes the TPS548A20 more competitive.

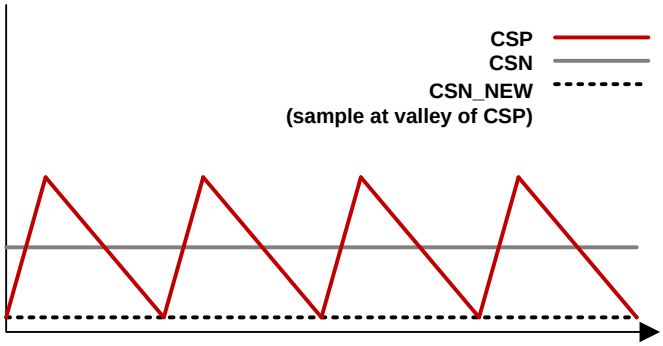


Figure 34. Continuous Conduction Mode (CCM) With Sample and Hold Circuitry

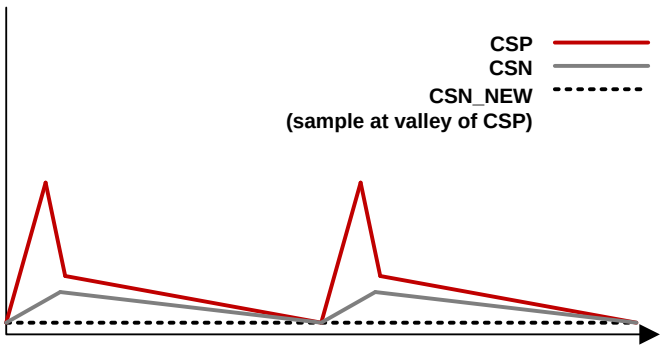


Figure 35. Discontinuous Conduction Mode (DCM) With Sample and Hold Circuitry

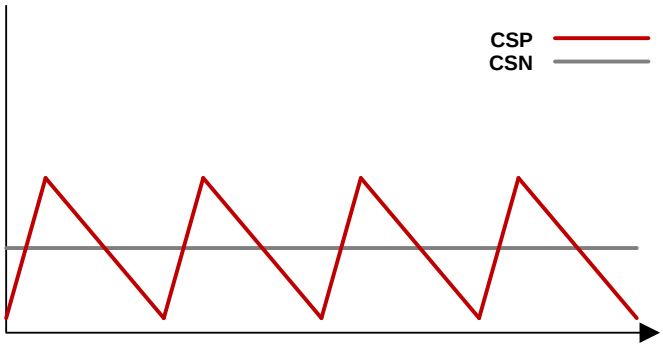


Figure 36. Continuous Conduction Mode (CCM) Without Sample and Hold Circuitry

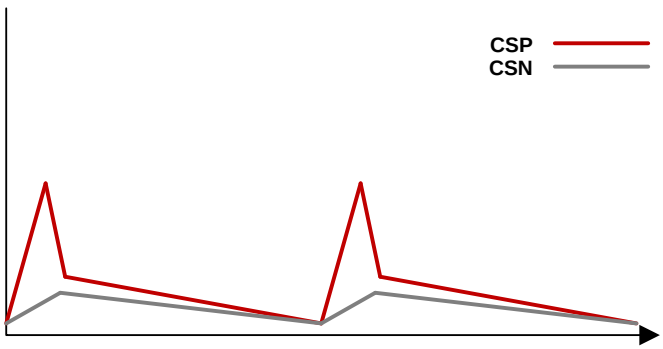


Figure 37. Discontinuous Conduction Mode (DCM) Without Sample and Hold Circuitry

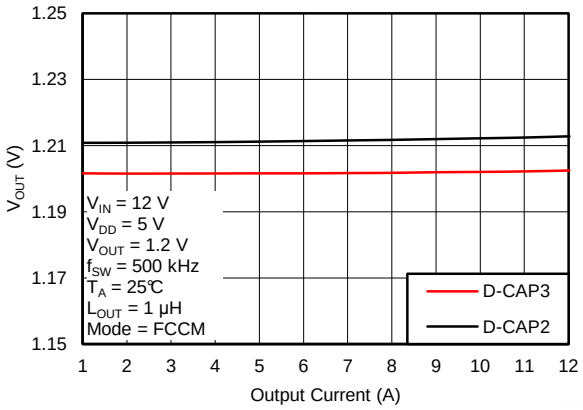


Figure 38. Output Voltage vs Output Current

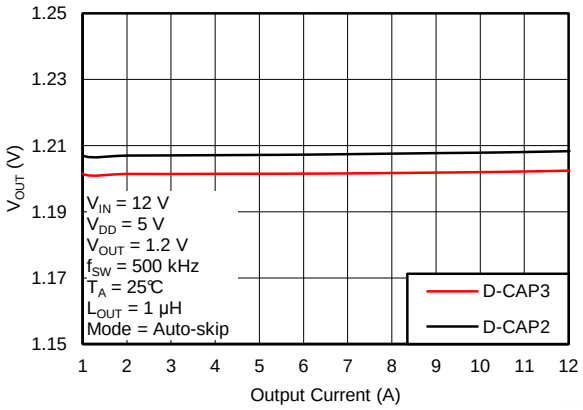


Figure 39. Output Voltage vs Output Current

7.3.5 Adaptive Zero-Crossing

The TPS548A20 uses an adaptive zero-crossing circuit to perform optimization of the zero inductor-current detection during Auto-skip-mode operation. This function allows ideal low-side MOSFET turn-off timing. The function also compensates the inherent offset voltage of the Z-C comparator and delay time of the Z-C detection circuit. Adaptive zero-crossing prevents SW-node swing-up caused by too-late detection and minimizes diode conduction period caused by too-early detection. As a result, the device delivers better light-load efficiency.

7.3.6 Forced Continuous-Conduction Mode

When the MODE pin is tied to the PGOOD pin through a resistor, the controller operates in continuous conduction mode (CCM) during light-load conditions. During CCM, the switching frequency maintained to an most constant level over the entire load range which is suitable for applications requiring tight control of the switching frequency at the cost of lower efficiency.

7.3.7 Current Sense and Overcurrent Protection

The TPS548A20 has cycle-by-cycle overcurrent limiting control. The inductor current is monitored during the OFF state and the controller maintains the OFF state during the period that the inductor current is larger than the overcurrent trip level. In order to provide good accuracy and a cost-effective solution, the TPS548A20 supports temperature compensated MOSFET $R_{DS(on)}$ sensing. Connect the TRIP pin to GND through the trip-voltage setting resistor, R_{TRIP}(**20kΩ<R_{TRIP}<65kΩ**). The TRIP terminal sources I_{TRIP} current, which is 10 µA typically at room temperature, and the trip level is set to the OCL trip voltage V_{TRIP} as shown in Equation 3.

$$V_{TRIP} = R_{TRIP} \times I_{TRIP}$$

where

- V_{TRIP} is in mV
- R_{TRIP} is in kΩ
- I_{TRIP} is in µA

(3)

Equation 4 calculates the typical DC OCP level (typical low-side on-resistance [RDS(on)] of 4.3 mΩ should be used); in order to design for worst case minimum OCP, maximum low-side on-resistance value of 5.7 mΩ should be used. The inductor current is monitored by the voltage between the GND pin and SW pin so that the SW pin is properly connected to the drain terminal of the low-side MOSFET. I_{TRIP} has a 3000-ppm/°C temperature slope to compensate the temperature dependency of $R_{DS(on)}$. The GND pin acts as the positive current-sensing node. Connect the GND pin to the proper current sensing device, (for example, the source terminal of the low-side MOSFET.)

Because the comparison occurs during the OFF state, V_{TRIP} sets the valley level of the inductor current. Thus, the load current at the overcurrent threshold, I_{OCP}, is calculated as shown in Equation 4.

$$I_{OCP} = \frac{V_{TRIP}}{\left(8 \times R_{DS(on)}\right)} + \frac{I_{IND(ripple)}}{2} = \frac{V_{TRIP}}{\left(8 \times R_{DS(on)L}\right)} + \frac{1}{2 \times L \times f_{SW}} \times \frac{\left(V_{IN} - V_{OUT}\right) \times V_{OUT}}{V_{IN}}$$

where

- $R_{DS(on)}$ is the on-resistance of the low-side MOSFET
- R_{TRIP} is in kΩ (4)

In an overcurrent condition, the current to the load exceeds the current to the output capacitor thus the output voltage tends to decrease. Eventually, the output voltage crosses the undervoltage-protection threshold and shuts down.

7.3.8 Overvoltage and Undervoltage Protection

The TPS548A20 monitors a resistor-divided feedback voltage to detect overvoltage and undervoltage. When the feedback voltage becomes lower than 68% of the target voltage, the UVP comparator output goes high and an internal UVP delay counter begins counting. After 1 ms, the TPS548A20 latches OFF both high-side and low-side MOSFETs drivers. The UVP function enables after soft-start is complete.

When the feedback voltage becomes higher than 120% of the target voltage, the OVP comparator output goes high and the circuit latches OFF the high-side MOSFET driver and turns on the low-side MOSFET until reaching a negative current limit. Upon reaching the negative current limit, the low-side FET is turned off and the high-side FET is turned on again for a minimum on-time. The TPS548A20 operates in this cycle until the output voltage is pulled down under the UVP threshold voltage for 1 ms. After the 1-ms UVP delay time, the high-side FET is latched off and low-side FET is latched on. The fault is cleared with a reset of VDD or by re-toggling EN pin.

7.3.9 Out-of-Bounds Operation (OOB)

The TPS548A20 has an out-of-bounds (OOB) overvoltage protection that protects the output load at a much lower overvoltage threshold of 8% above the target voltage. OOB protection does not trigger an overvoltage fault, so the device is not latched off after an OOB event. OOB protection operates as an early no-fault overvoltage-protection mechanism. During the OOB operation, the controller operates in forced PWM mode only by turning on the low-side FET. Turning on the low-side FET beyond the zero inductor current quickly discharges the output capacitor thus causing the output voltage to fall quickly towards the setpoint. During the operation, the cycle-by-cycle negative current limit is also activated to ensure the safe operation of the internal FETs.

7.3.10 UVLO Protection

The TPS548A20 monitors the voltage on the VDD pin. If the VDD pin voltage is lower than the UVLO off-threshold voltage, the switch mode power supply shuts off. If the VDD voltage increases beyond the UVLO on-threshold voltage, the controller turns back on. UVLO is a non-latch protection.

7.3.11 Thermal Shutdown

The TPS548A20 monitors internal temperature. If the temperature exceeds the threshold value (typically 140°C), TPS548A20 shuts off. When the temperature falls approximately 40°C below the threshold value, the device turns on. Thermal shutdown is a non-latch protection.

7.4 Device Functional Modes

7.4.1 Auto-Skip Eco-Mode Light-Load Operation

While the MODE pin is pulled to GND directly or through a 150-kΩ resistor, the TPS548A20 device automatically reduces the switching frequency at light-load conditions to maintain high efficiency. This section describes the operation in detail.

As the output current decreases from heavy-load condition, the inductor current also decreases until the rippled valley of the inductor current touches zero level. Zero level is the boundary between the continuous-conduction and discontinuous-conduction modes. The synchronous MOSFET turns off when this zero inductor current is detected. As the load current decreases further, the converter runs into discontinuous-conduction mode (DCM). The on-time is maintained to a level approximately the same as during continuous-conduction mode operation so that discharging the output capacitor with a smaller load current to the level of the reference voltage requires more time. The transition point to the light-load operation $I_{OUT(LL)}$ (for example: the threshold between continuous-conduction mode and discontinuous-conduction mode) is calculated as shown in Equation 5.

$$I_{OUT(LL)} = \frac{1}{2 \times L \times f_{SW}} \times \frac{(V_{IN} - V_{OUT}) \times V_{OUT}}{V_{IN}} \quad (5)$$

where

- f SW is the PWM switching frequency

TI recommends only using ceramic capacitors for Auto-skip mode.

7.4.2 Forced Continuous-Conduction Mode

When the MODE pin is tied to the PGOOD pin through a resistor, the controller operates in continuous conduction mode (CCM) during light-load conditions. During CCM, the switching frequency maintained to an almost constant level over the entire load range which is suitable for applications requiring tight control of the switching frequency at the cost of lower efficiency.

8 Application and Implementation

NOTE

Information in the following applications sections is not part of the TI component specification, and TI does not warrant its accuracy or completeness. TI's customers are responsible for determining suitability of components for their purposes. Customers should validate and test their design implementation to confirm system functionality.

8.1 Application Information

The TPS548A20 device is a high-efficiency, single-channel, synchronous-buck converter. The device suits low-output voltage point-of-load applications with 15-A or lower output current in computing and similar digital consumer applications.

8.2 Typical Application

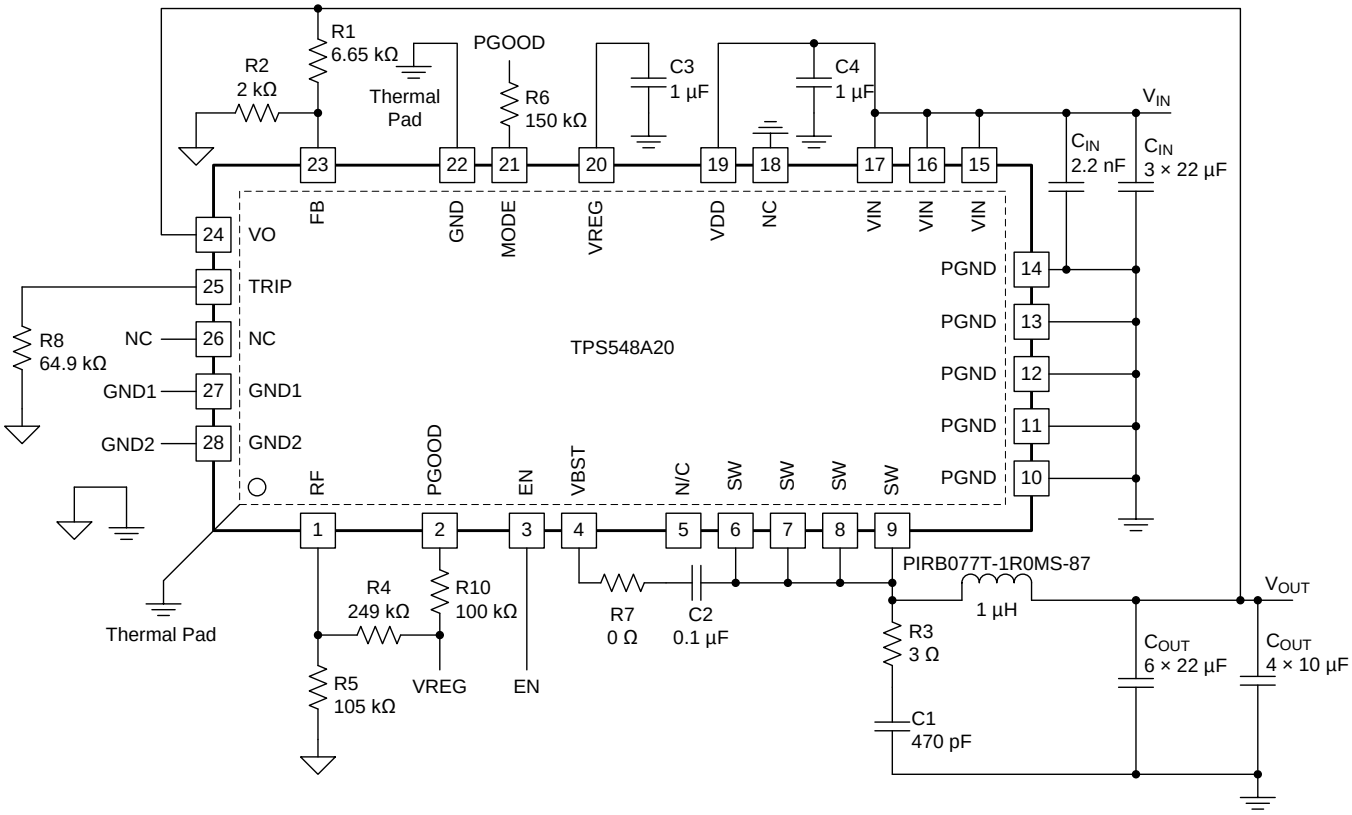


Figure 40. Typical Application Circuit Diagram

Typical Application (continued)

8.2.1 Design Requirements

This design uses the parameters listed in Table 4.

Table 4. Design Example Specifications

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
INPUT CHARACTERISTIC						
V_{IN}	Voltage range		5	12	18	V
I_{MAX}	Maximum input current	V_{IN} = 5 V, I_{OUT} = 8 A		2.5		A
	No load input current	V_{IN} = 12 V, I_{OUT} = 0 A with auto skip mode		1		mA
OUTPUT CHARACTERISTICS						
V_{OUT}	Output voltage			1.2		V
	Output voltage regulation	Line regulation, 5 V ≤ V_{IN} ≤ –14 V with FCCM		0.2%		
		Load regulation, V_{IN} = 12 V, 0 A ≤ I_{OUT} ≤ 8 A with FCCM		0.5%		
V_{RIPPLE}	Output voltage ripple	V_{IN} = 12 V, I_{OUT} = 8 A with FCCM		10		mV_{PP}
I_{LOAD}	Output load current		0		12	A
I_{OVER}	Output over current			11		
t_{SS}	Soft-start time			1		ms
SYSTEMS CHARACTERISTICS						
f_{SW}	Switching frequency			1		MHz
η	Peak efficiency	V_{IN} = 12 V, V_{OUT} = 1.2 V, I_{OUT} = 4 A		91.2%		
η	Full load efficiency	V_{IN} = 12 V, V_{OUT} = 1.2 V, I_{OUT} = 8 A		90.3%		
T_A	Operating temperature			25		°C

8.2.2 Detailed Design Procedure

The external components selection is a simple process using D-CAP3 mode. Select the external components using the following steps.

8.2.2.1 Choose the Switching Frequency

The switching frequency is configured by the resistor divider on the RF pin. Select one of eight switching frequencies from 250 kHz to 1 MHz. Refer to for the relationship between the switching frequency and resistor-divider configuration.

8.2.2.2 Choose the Operation Mode

Select the operation mode using Table 3.

8.2.2.3 Choose the Inductor

Determine the inductance value to set the ripple current at approximately ¼ to ½ of the maximum output current. Larger ripple current increases output ripple voltage, improves signal-to-noise ratio, and helps to stabilize operation.

$$L = \frac{1}{I_{IND(ripple)} \times f_{SW}} \times \frac{\left(V_{IN(max)} - V_{OUT}\right) \times V_{OUT}}{V_{IN(max)}} = \frac{3}{I_{OUT(max)} \times f_{SW}} \times \frac{\left(V_{IN(max)} - V_{OUT}\right) \times V_{OUT}}{V_{IN(max)}}$$

$$= \frac{3}{6 \times 500\,kHz} \times \frac{(12\,V - 1.2\,V) \times 1.2\,V}{12\,V} = 1.08\,\mu H \quad (6)$$

The inductor requires a low DCR to achieve good efficiency. The inductor also requires enough room above peak inductor current before saturation. The peak inductor current is estimated using Equation 7.

$$I_{IND(peak)} = \frac{V_{TRIP}}{8 \times R_{DS(on)}} + \frac{1}{L \times f_{SW}} \times \frac{\left(V_{IN(max)} - V_{OUT}\right) \times V_{OUT}}{V_{IN(max)}} = \frac{10\,\mu A \times R_{TRIP}}{8 \times 4.3\,m\Omega} + \frac{1}{1\,\mu H \times 500\,kHz} \times \frac{(12\,V - 1.2\,V) \times 1.2\,V}{12\,V} \quad (7)$$

8.2.2.4 Choose the Output Capacitor

The output capacitor selection is determined by output ripple and transient requirement. When operating in CCM, the output ripple has two components as shown in Equation 8. Equation 9 and Equation 10 define these components.

$$V_{RIPPLE} = V_{RIPPLE(C)} + V_{RIPPLE(ESR)} \quad (8)$$

$$V_{RIPPLE(C)} = \frac{I_{L(ripple)}}{8 \times C_{OUT} \times f_{SW}} \quad (9)$$

$$V_{RIPPLE(ESR)} = I_{L(ripple)} \times ESR \quad (10)$$

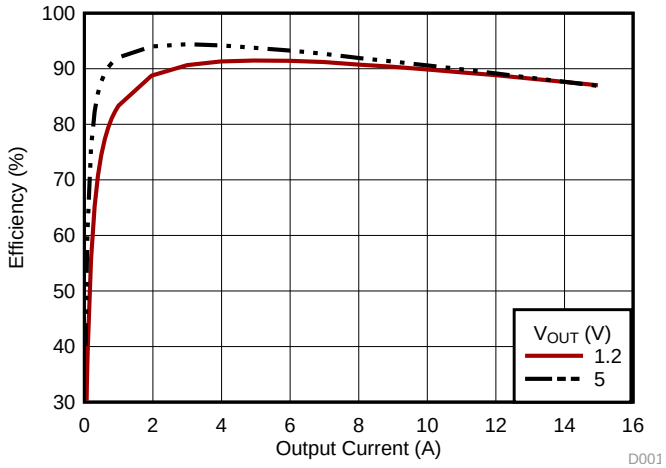
8.2.2.5 Determine the Value of R1 and R2

The output voltage is programmed by the voltage-divider resistors, R1 and R2, shown in Equation 11. Connect R1 between the VFB pin and the output, and connect R2 between the VFB pin and GND. The recommended R2 value is from 1 kΩ to 20 kΩ. Determine R1 using Equation 11.

$$R1 = \frac{V_{OUT} - 0.6}{0.6} \times R2 = \frac{1.2\,V - 0.6}{0.6} \times 10\,k\Omega = 10\,k\Omega \quad (11)$$

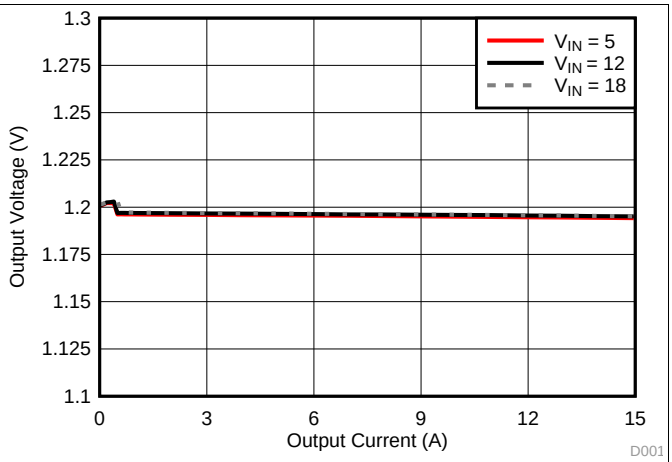
8.2.3 Application Curves

T_A = 25°C (unless otherwise noted)



f_{SW} = 500 kHz FCCM
V_{IN} = 12 V

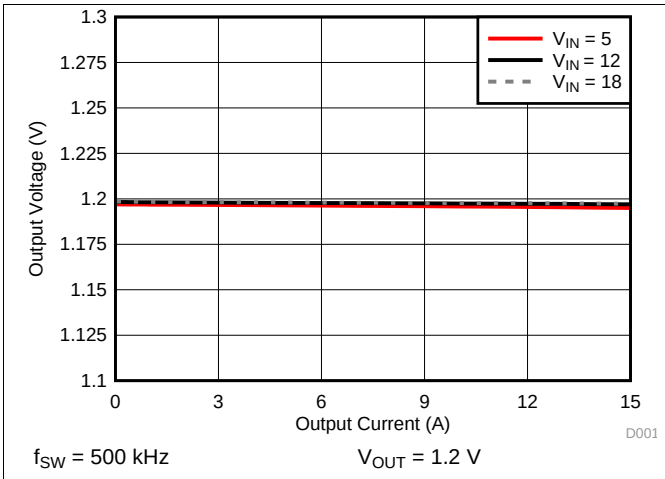
Figure 41. Efficiency vs. Output Current



f_{SW} = 500 kHz V_{OUT} = 1.2 V

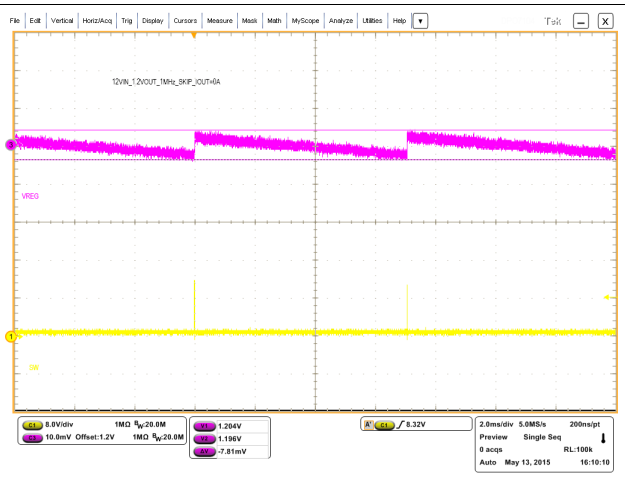
Figure 42. DC Load Regulation

T_A = 25°C (unless otherwise noted)



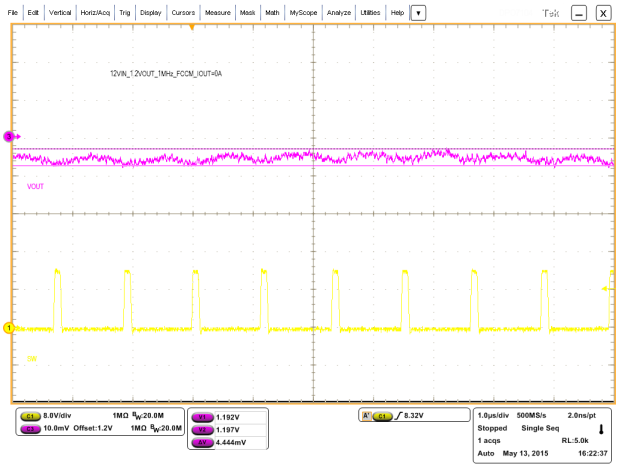
f_{SW} = 500 kHz V_{OUT} = 1.2 V

Figure 43. DC Load Regulation



I_{OUT} = 0 A

Figure 44. Auto-skip Mode Steady-State Operation

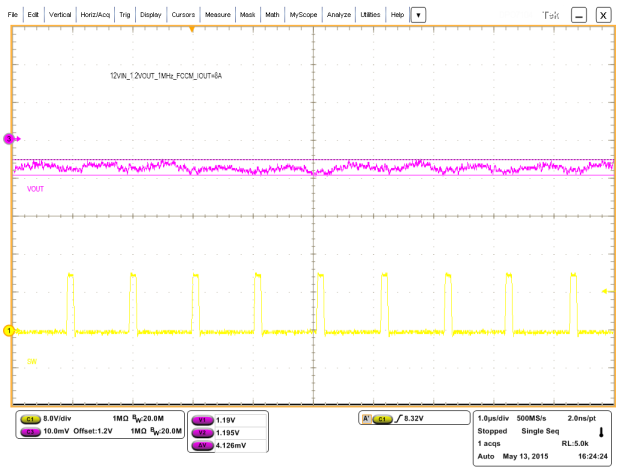


I_{LOAD} = 0 A

Figure 45. FCCM Steady-State Operation

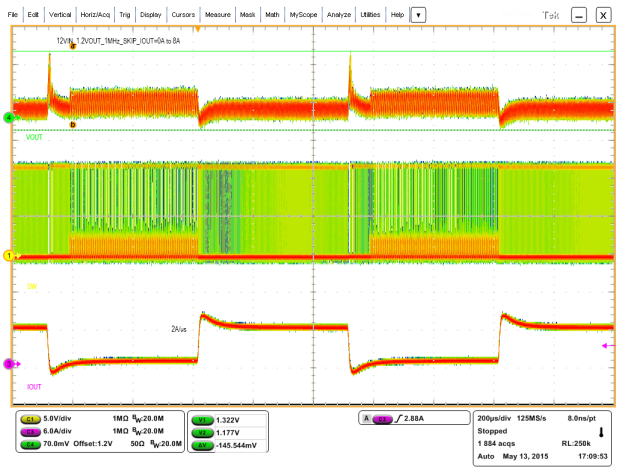
I_{LOAD} = 8 A

Figure 46. Auto-skip Mode Steady-State Operation



I_{LOAD} = 8 A

Figure 47. Steady-State Operation



I_{LOAD} from 0 A to 8 A Div = 2 A/µs

Figure 48. Auto-skip Mode Load Transient

T_A = 25°C (unless otherwise noted)

I_{LOAD} from 0 A to 8 A Div = 2 A/µs

Figure 49. Load Transient

9 Power Supply Recommendations

This device is designed to operate from an input voltage supply between 1.5-V and 18-V (4.5-V and 25-V biased) Input. use only a well regulated supply. These devices are not designed for split-rail operation. The VIN and VDD terminals must be the same potential for accurate high-side short circuit protection. Proper bypassing of input supplies and internal regulators is also critical for noise performance, as is PCB layout and grounding scheme. See the recommendations in the *Layout* section.

10 Layout

10.1 Layout Guidelines

Before beginning a design using the TPS548A20 , consider the following:

- Place the power components (including input and output capacitors, the inductor, and the TPS548A20) on the solder side of the PCB. In order to shield and isolate the small signal traces from noisy power lines, insert and connect at least one inner plane to ground.
- All sensitive analog traces and components such as VFB, PGOOD, TRIP, MODE, and ADDR must be placed away from high-voltage switching nodes such as SW and VBST to avoid coupling. Use internal layers as ground planes and shield the feedback trace from power traces and components.
- Pin 22 (GND pin) must be connected directly to the thermal pad. Connect the thermal pad to the PGND pins and then to the GND plane.
- Place the VIN decoupling capacitors as close to the VIN and PGND pins as possible to minimize the input AC-current loop.
- Place the feedback resistor near the IC to minimize the VFB trace distance.
- Place the frequency-setting resistor (ADDR), OCP-setting resistor (R_{TRIP}) and mode-setting resistor (R_{MODE}) close to the device. Use the common GND via to connect the resistors to the GND plane if applicable.
- Place the VDD and VREG decoupling capacitors as close to the device as possible. Provide GND vias for each decoupling capacitor and ensure the loop is as small as possible.
- The PCB trace is defined as switch node, which connects the SW pins and high-voltage side of the inductor. The switch node should be as short and wide as possible.
- Use separated vias or trace to connect SW node to the snubber, bootstrap capacitor, and ripple-injection resistor. Do not combine these connections.
- Place one more small capacitor (2.2 nF, 0402 size) between the VIN and PGND pins. This capacitor must be placed as close to the IC as possible.
- TI recommends placing a snubber between the SW shape and GND shape for effective ringing reduction. The value of snubber design starts at 3 Ω + 470 pF.
- Consider R-C-C_C network (Ripple injection network) component placement and place the AC coupling capacitor, C_C, close to the device, and R and C close to the power stage.
- See Figure 50 for the layout recommendation.

10.2 Layout Example

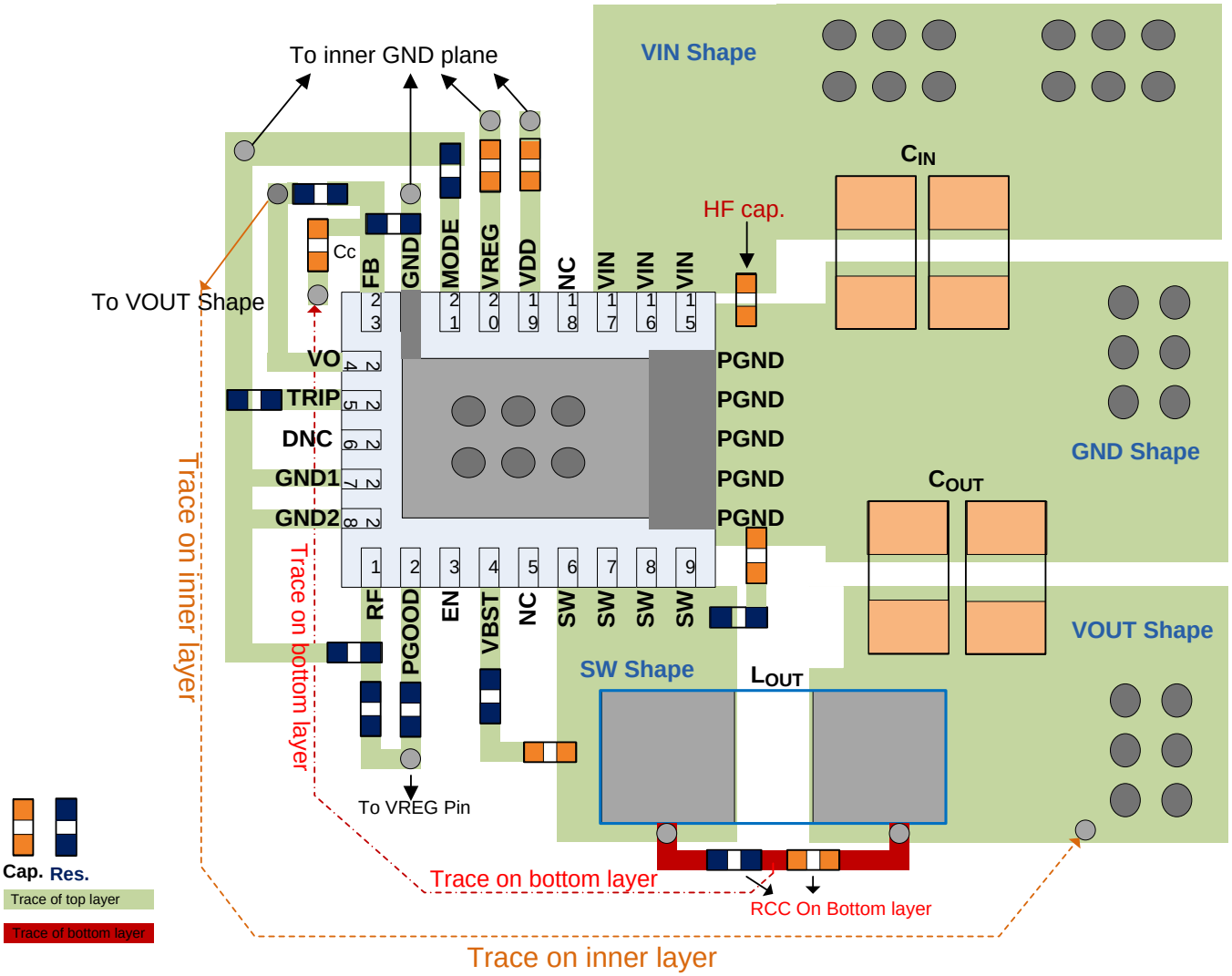


Figure 50. Layout Recommendation

11 Device and Documentation Support

11.1 Documentation Support

For related documentation, see the following:

- *Optimizing Transient Response of Internally Compensated dc-dc Converters With Feedforward Capacitor*, Application Report SLVA289

11.2 Trademarks

SWIFT, D-CAP3, Eco-Mode, WEBENCH are trademarks of Texas Instruments.
All other trademarks are the property of their respective owners.

11.3 Electrostatic Discharge Caution

These devices have limited built-in ESD protection. The leads should be shorted together or the device placed in conductive foam during storage or handling to prevent electrostatic damage to the MOS gates.

11.4 Glossary

SLYZ022 — *TI Glossary*.

This glossary lists and explains terms, acronyms, and definitions.

12 Mechanical, Packaging, and Orderable Information

The following pages include mechanical, packaging, and orderable information. This information is the most current data available for the designated devices. This data is subject to change without notice and revision of this document. For browser-based versions of this data sheet, refer to the left-hand navigation.

PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead finish/ Ball material (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
TPS548A20RVER	ACTIVE	VQFN-CLIP	RVE	28	2500	RoHS-Exempt & Green	NIPDAU | SN	Level-2-260C-1 YEAR	-40 to 125	T548A20	Samples
TPS548A20RVET	ACTIVE	VQFN-CLIP	RVE	28	250	RoHS-Exempt & Green	NIPDAU | SN	Level-2-260C-1 YEAR	-40 to 125	T548A20	Samples

(1) The marketing status values are defined as follows:
ACTIVE: Product device recommended for new designs.
LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
PREVIEW: Device has been announced but is not in production. Samples may or may not be available.
OBSOLETE: TI has discontinued the production of the device.

(2) **RoHS:** TI defines "RoHS" to mean semiconductor products that are compliant with the current EU RoHS requirements for all 10 RoHS substances, including the requirement that RoHS substance do not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, "RoHS" products are suitable for use in specified lead-free processes. TI may reference these types of products as "Pb-Free".
RoHS Exempt: TI defines "RoHS Exempt" to mean products that contain lead but are compliant with EU RoHS pursuant to a specific EU RoHS exemption.
Green: TI defines "Green" to mean the content of Chlorine (Cl) and Bromine (Br) based flame retardants meet JS709B low halogen requirements of <=1000ppm threshold. Antimony trioxide based flame retardants must also meet the <=1000ppm threshold requirement.

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

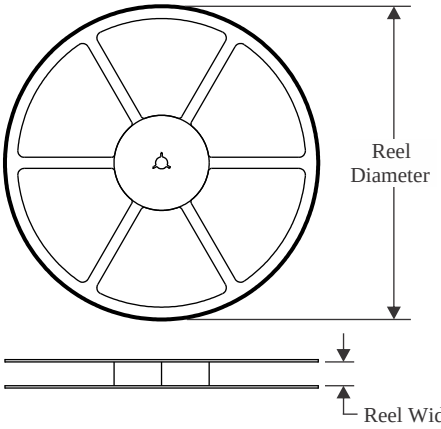
(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

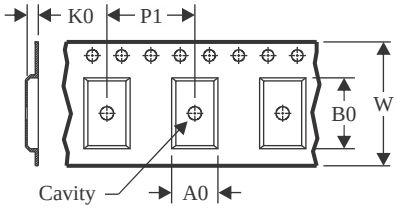
(6) Lead finish/Ball material - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

TAPE AND REEL INFORMATION

REEL DIMENSIONS

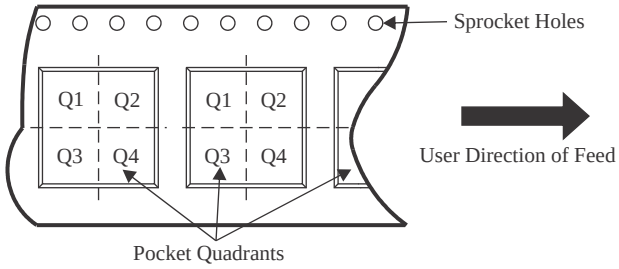


TAPE DIMENSIONS



A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

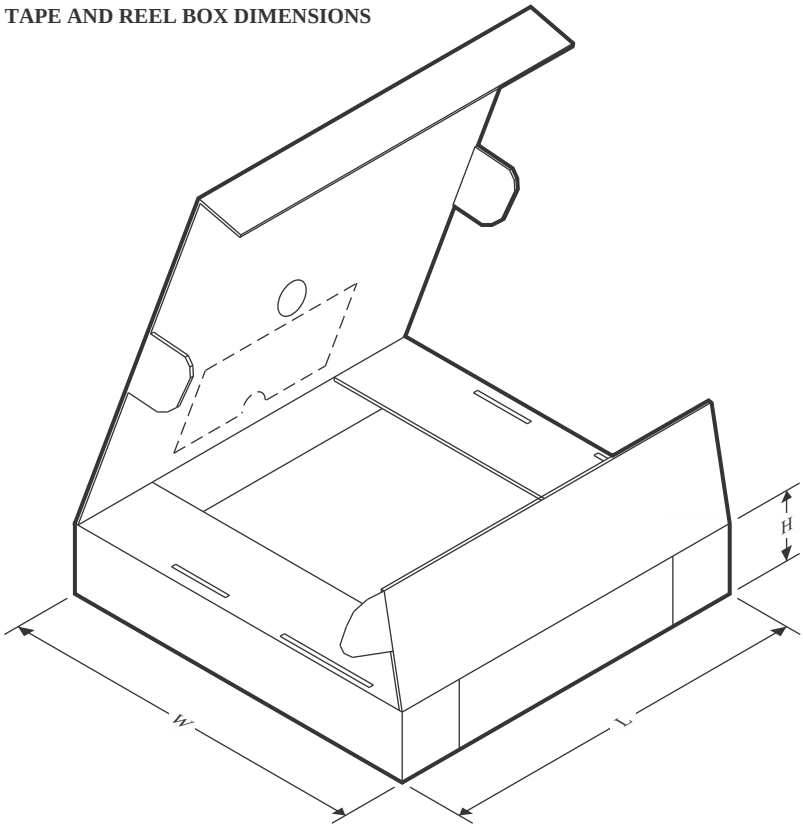
QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
TPS548A20RVER	VQFN-CLIP	RVE	28	2500	330.0	12.4	3.71	4.71	1.1	8.0	12.0	Q1
TPS548A20RVET	VQFN-CLIP	RVE	28	250	180.0	12.4	3.71	4.71	1.1	8.0	12.0	Q1

TAPE AND REEL BOX DIMENSIONS



*All dimensions are nominal

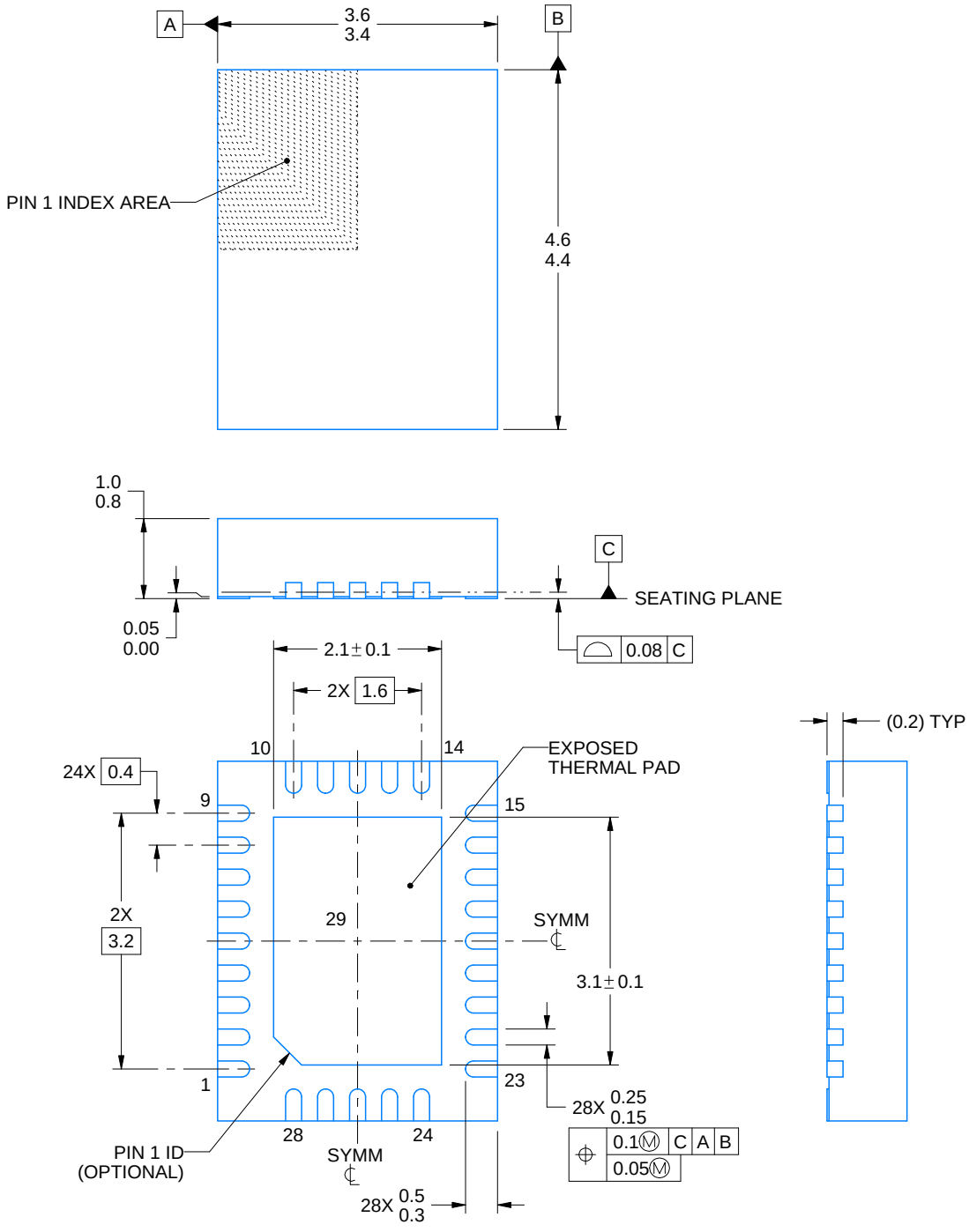
Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
TPS548A20RVER	VQFN-CLIP	RVE	28	2500	346.0	346.0	33.0
TPS548A20RVET	VQFN-CLIP	RVE	28	250	210.0	185.0	35.0

PACKAGE OUTLINE

RVE0028A

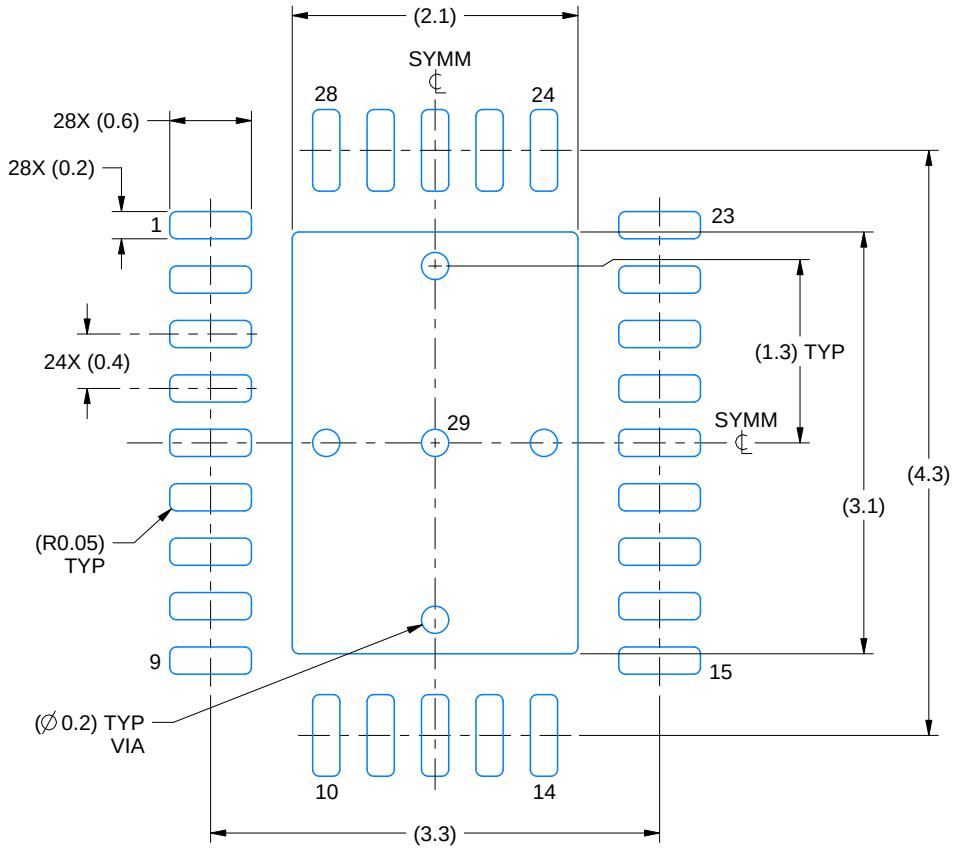
VQFN - 1 mm max height

PLASTIC QUAD FLATPACK - NO LEAD

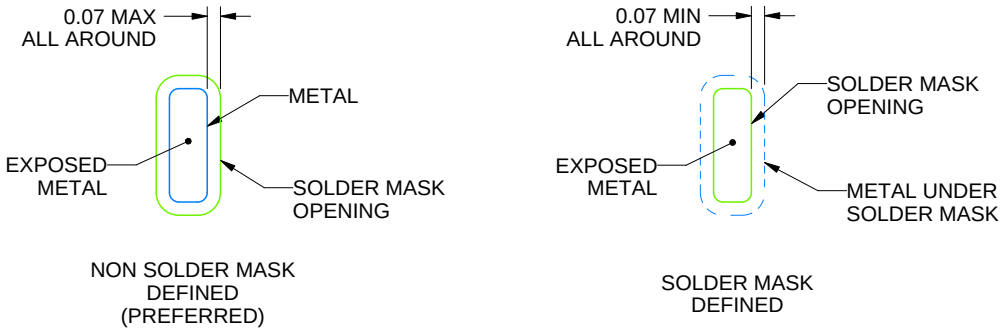


NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. The package thermal pad must be soldered to the printed circuit board for thermal and mechanical performance.



LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE:18X



SOLDER MASK DETAILS

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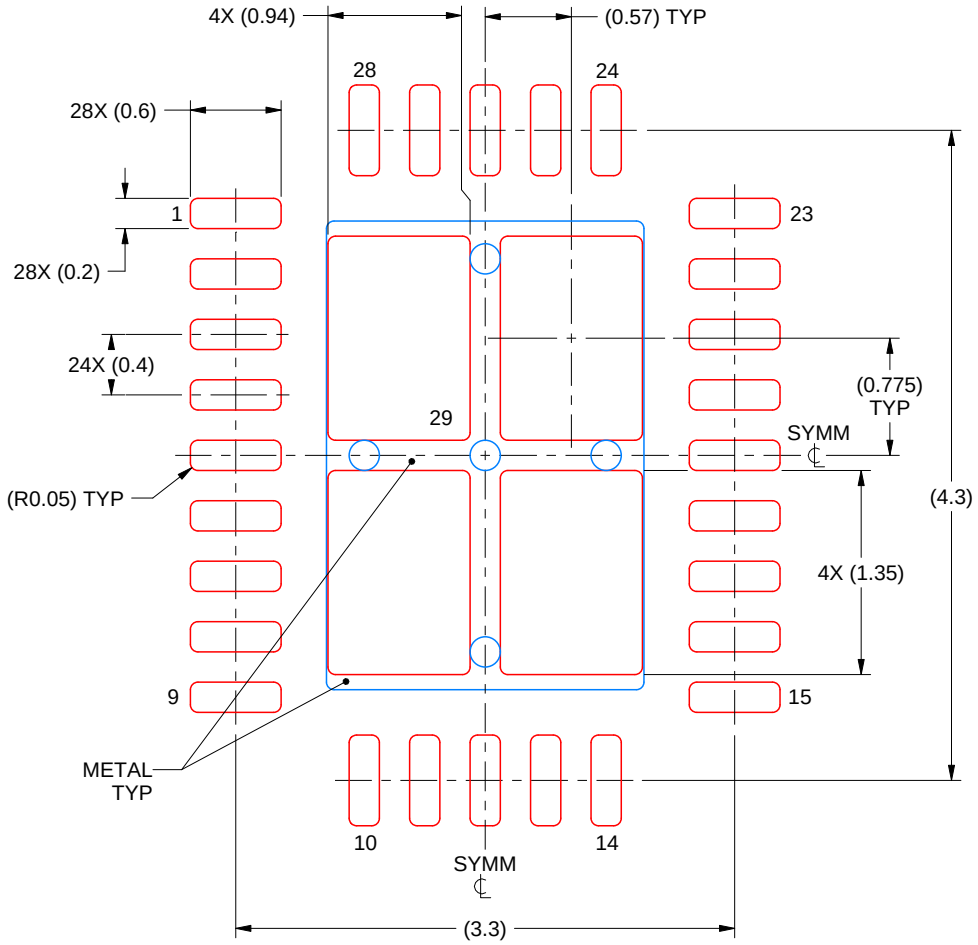
NOTES: (continued)

4. This package is designed to be soldered to a thermal pad on the board. For more information, see Texas Instruments literature number SLUA271 (www.ti.com/lit/slua271).
5. Vias are optional depending on application, refer to device data sheet. If any vias are implemented, refer to their locations shown on this view. It is recommended that vias under paste be filled, plugged or tented.



SOLDER PASTE EXAMPLE
BASED ON 0.125 mm THICK STENCIL

EXPOSED PAD 29
78% PRINTED SOLDER COVERAGE BY AREA UNDER PACKAGE
SCALE:20X

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NOTES: (continued)

6. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.

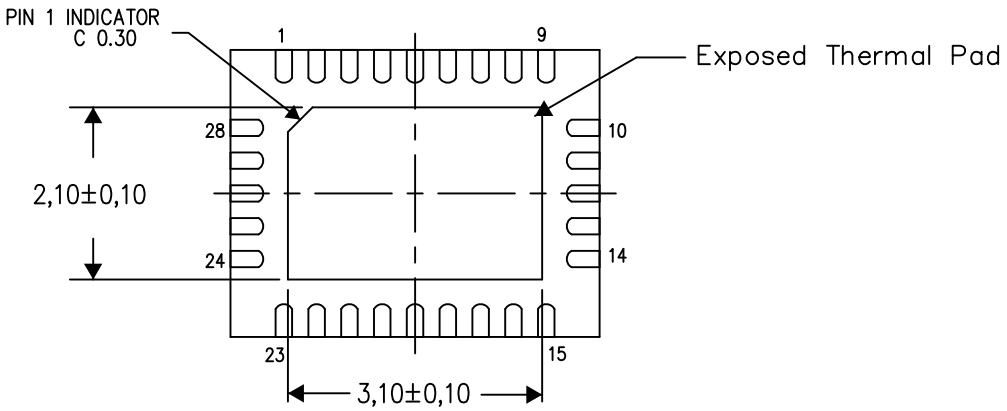
RVE (R–PVQFN–N28) PLASTIC QUAD FLATPACK NO–LEAD

THERMAL INFORMATION

This package incorporates an exposed thermal pad that is designed to be attached directly to an external heatsink. The thermal pad must be soldered directly to the printed circuit board (PCB). After soldering, the PCB can be used as a heatsink. In addition, through the use of thermal vias, the thermal pad can be attached directly to the appropriate copper plane shown in the electrical schematic for the device, or alternatively, can be attached to a special heatsink structure designed into the PCB. This design optimizes the heat transfer from the integrated circuit (IC).

For information on the Quad Flatpack No–Lead (QFN) package and its advantages, refer to Application Report, QFN/SON PCB Attachment, Texas Instruments Literature No. SLUA271. This document is available at www.ti.com.

The exposed thermal pad dimensions for this package are shown in the following illustration.



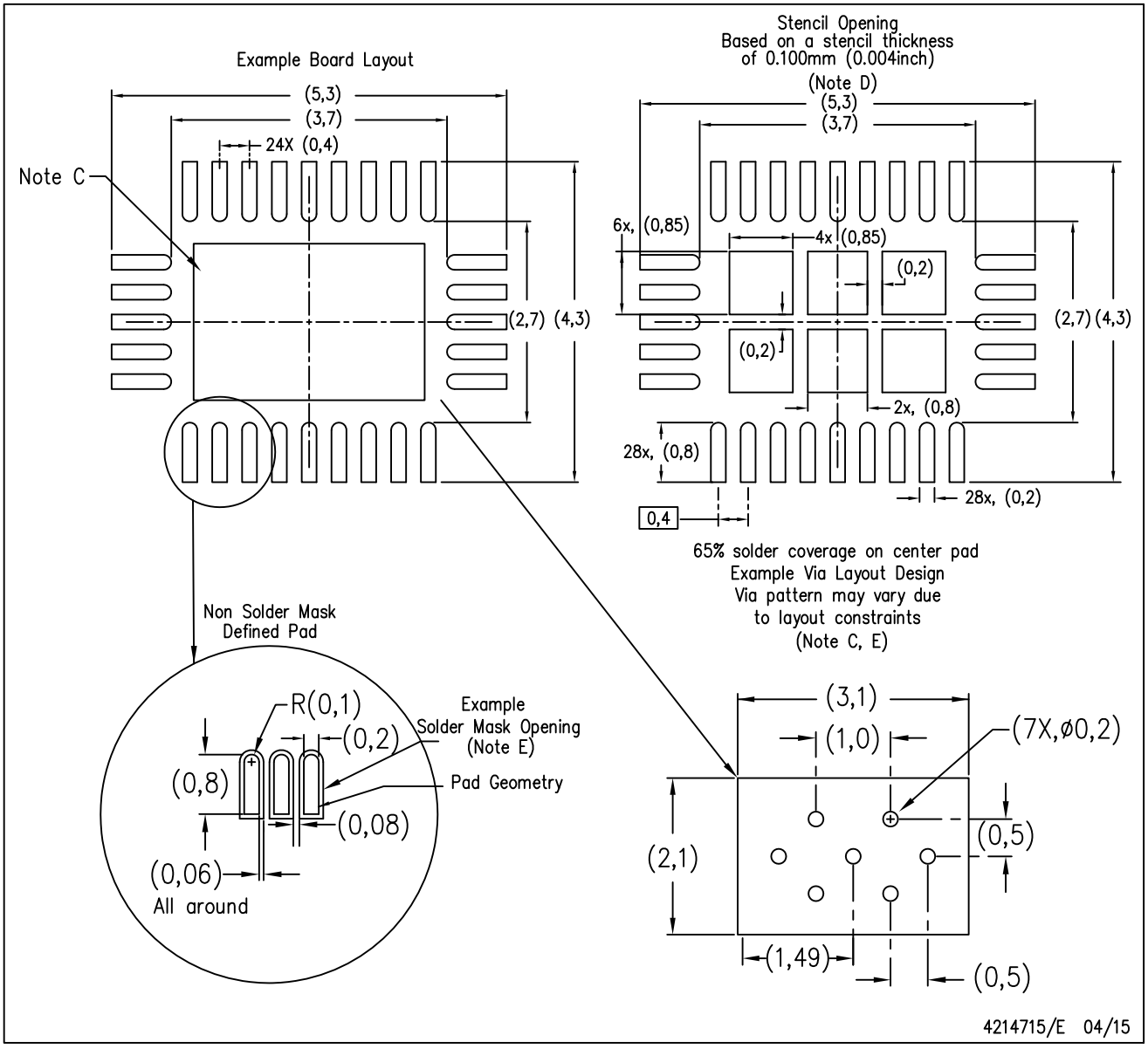
Bottom View

Exposed Thermal Pad Dimensions

4211776/E 04/15

NOTE: All linear dimensions are in millimeters

RVE (R–PWQFN–N28) PLASTIC QUAD FLATPACK NO–LEAD



NOTES:
A. All linear dimensions are in millimeters.
B. This drawing is subject to change without notice.
C. This package is designed to be soldered to a thermal pad on the board. Refer to Application Note, Quad Flat–Pack Packages, Texas Instruments Literature No. SLUA271, and also the Product Data Sheets for specific thermal information, via requirements, and recommended board layout. These documents are available at www.ti.com <http://www.ti.com>.
D. Laser cutting apertures with trapezoidal walls and also rounding corners will offer better paste release. Electroformed stencils offer adequate release at thicker values/lower Area Ratios. Customers should contact their board assembly site for stencil design recommendations. Refer to IPC 7525 for stencil design considerations.
E. Customers should contact their board fabrication site for minimum solder mask web tolerances between signal pads.

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