TPS56428 4.5-V to 18-V Input, 4-A Sync. Step-Down Converter with Advanced Eco-mode™

1 Features

- D-CAP2™ Mode at 650kHz Switching for Fast Transient Response, Ceramic Capacitor Support
- V_{IN} Input Voltage Range: 4.5 V to 18 V
- Output Voltage Range: 0.6 V to 7.0 V
- Advanced Eco-mode for High Light Load Efficiency
- Integrated FETs Optimized for Lower Duty Cycle – 68 mΩ (High Side) and 37 mΩ (Low Side)
- Shutdown Current Less Than 10 µA
- 1% Initial Reference Voltage Accuracy
- Soft Start with Pre-Bias Output Support
- Cycle By Cycle Over Current Limit
- Power Good Output
- Fixed Soft Start : 1.0ms

2 Applications

- Digital TV, High Definition Video Equipment
- Networking Home Terminal
- Digital Set Top Box (STB)
- Network Controllers

3 Description

The TPS56428 is a D-CAP2 mode synchronous buck converter which is optimized for various power bus regulation needs with a cost effective, low component count, low standby current solution.

The D-CAP2 mode control provides a fast transient response with no external compensation components. This adaptive on-time control supports seamless transition between PWM mode at higher load conditions and advanced Eco-mode operation at light loads. Advanced Eco-mode™ maintains higher efficiency during lighter load conditions than traditional skip mode.

The TPS56428 also has a proprietary circuit to adopt to both low equivalent series resistance (ESR) output capacitors, such as POSCAP or SP-CAP, and ultra-low ESR ceramic capacitors. The device operates from 4.5-V to 18 V VIN input and its output voltage can be programmed between 0.6V and 7.0V. The device also features a fixed 1-ms soft start and a power-good output.

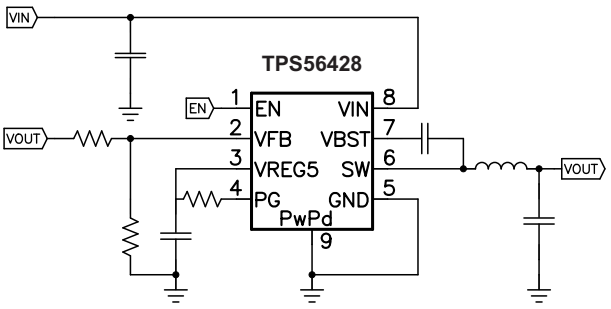
The TPS56428 is available in 8-pin SOIC-8 and 14-pin QFN packages designed to operate over the ambient temperature range of –40°C to 85°C.

Device Information(1)

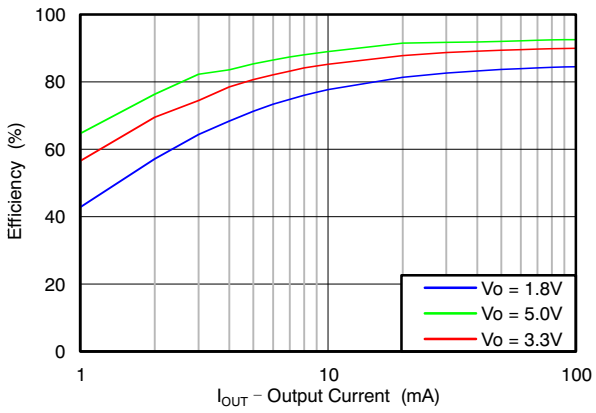
PART NUMBER	PACKAGE	BODY SIZE (NOM)
TPS56428	HSOP (8)	4.89 mm × 3.9 mm
	VQFN (14)	3.5 mm × 3.5 mm

(1) For all available packages, see the orderable addendum at the end of the data sheet.

Simplified Schematic



Light Load Efficiency with Advanced Eco-mode



An IMPORTANT NOTICE at the end of this data sheet addresses availability, warranty, changes, use in safety-critical applications, intellectual property matters and other important disclaimers. PRODUCTION DATA.

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4 Revision History

Changes from Revision A (April 2013) to Revision B **Page**

- Added *Device Information* and *ESD Rating* tables, *Feature Description* section, *Device Functional Modes*, *Application and Implementation* section, *Power Supply Recommendations* section, *Layout* section, *Device and Documentation Support* section, and *Mechanical, Packaging, and Orderable Information* section ... 1
- Added RHL package outline and pinout descriptions ... 3
- Added RHL package Thermal Information ... 5
- Changed Figure 14 Y-axis label from "V_{OUT} - Output Voltage (V)" to "f_{SW} - Switching Frequency (kHz)" ... 13
- Added PCB layout example for RHL package. ... 17

Changes from Original (April 2013) to Revision A **Page**

- Changed the device From: Preview To: Production ... 1

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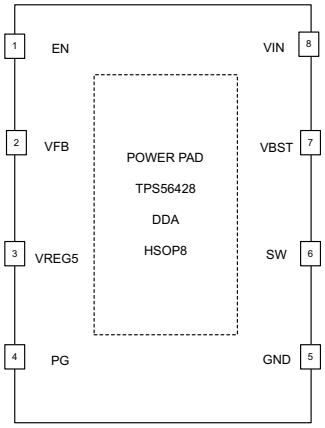
5 Device Comparison Table

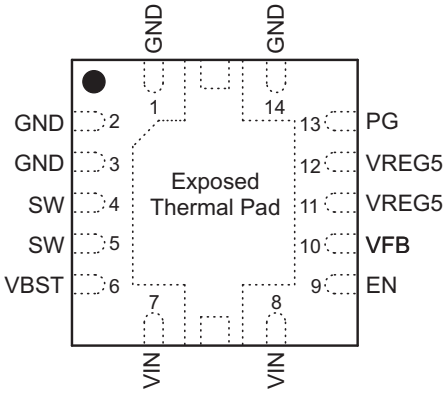
T_A	PART NUMBER	PINS	
		HSOP (DDA)	VQFN (RHL)
–40°C to 85°C	TPS56428	8	14

6 Pin Configuration and Functions

8-Pin HSOP with Thermal Pad
DDA PACKAGE
(Top View)



14-Pin VQFN with Thermal Pad
RHL Package
(Top View)



Pin Functions

PIN			DESCRIPTION
	NUMBER		
NAME	DDA	RHL	
EN	1	9	Enable input control. Active high. Active high and must be pulled up to enable the device.
VFB	2	10	Converter feedback input. Connect to output voltage with feedback resistor divider.
VREG5	3	11, 12	5.5 V power supply output. A capacitor (typical 0.47 µF) should be connected to GND. VREG5 is not active when EN is low.
PG	4	13	Open drain power good output.
GND	5	1, 2, 3, 14	Ground pin. Power ground return for switching circuit. Connect sensitive SS and VFB returns to GND at a single point. Connect all four GND pins together on a PCB trace as short as possible.
SW	6	4, 5	Switch node connection between high-side NFET and low-side NFET. Connect two SW pins together on a PCB trace.
VBST	7	6	Supply input for the high-side FET gate drive circuit. Connect 0.1µF capacitor between VBST and SW pins. An internal diode is connected between VREG5 and VBST.
VIN	8	7, 8	Input voltage supply pin. Connect two VIN pins together on a PCB trace as short as possible.
Exposed Thermal Pad	Back side	Back side	Thermal pad of the package. Must be soldered to achieve appropriate dissipation. Must be connected to GND.

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7 Specifications

7.1 Absolute Maximum Ratings

over operating free-air temperature range (unless otherwise noted)(1)

		VALUE		UNIT
		MIN	MAX	
Input voltage range	VIN, EN	–0.3	20	V
	VBST	–0.3	26	V
	VBST (10 ns transient)	–0.3	28	V
	VBST (vs SW)	–0.3	6.5	V
	VFB, PG	–0.3	6.5	V
	SW	–2	20	V
	SW (10 ns transient)	–3	22	V
Output voltage range	VREG5	–0.3	6.5	V
	GND	–0.3	0.3	V
Voltage from GND to thermal pad, V_{diff}		–0.2	0.2	V
Operating junction temperature, T_J		–40	150	°C
Storage temperature, T_{stg}		–55	150	°C

(1) Stresses beyond those listed under *absolute maximum ratings* may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under *recommended operating conditions* is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

7.2 ESD Ratings

			VALUE	UNIT
$V_{(ESD)}$	Electrostatic discharge	Human-body model (HBM), per ANSI/ESDA/JEDEC JS-001(1)	±2000	V
		Charged-device model (CDM), per JEDEC specification JESD22-C101(2)	±500	

(1) JEDEC document JEP155 states that 500-V HBM allows safe manufacturing with a standard ESD control process.
(2) JEDEC document JEP157 states that 250-V CDM allows safe manufacturing with a standard ESD control process.

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7.3 Recommended Operating Conditions

over operating free-air temperature range (unless otherwise noted)

			MIN	MAX	UNIT
V_{IN}	Supply input voltage range		4.5	18	V
V_I	Input voltage range	VBST	–0.1	24	V
		VBST (10 ns transient)	-0.1	27	
		VBST(vs SW)	–0.1	6.0	
		PG	–0.1	5.7	
		EN	–0.1	18	
		VFB	–0.1	5.5	
		SW	–1.8	18	
		SW (10 ns transient)	–3	21	
		GND	–0.1	0.1	
V_O	Output voltage range	VREG5	–0.1	5.7	V
I_O	Output Current range	I_{VREG5}	0	5	mA
T_A	Operating free-air temperature		–40	85	°C
T_J	Operating junction temperature		–40	150	°C

7.4 Thermal Information

THERMAL METRIC[1]		TPS56428		UNIT
		DDA	RHL	
		8 PINS	14 PINS	
$R_{\theta JA}$	Junction-to-ambient thermal resistance	44.4	45.2	°C/W
$R_{\theta JC(top)}$	Junction-to-case (top) thermal resistance	51.6	50.7	°C/W
$R_{\theta JB}$	Junction-to-board thermal resistance	27.8	21.4	°C/W
ψ_{JT}	Junction-to-top characterization parameter	8.7	0.9	°C/W
ψ_{JB}	Junction-to-board characterization parameter	27.7	21.6	°C/W
$R_{\theta JC(bot)}$	Junction-to-case (bottom) thermal resistance	5.3	3.5	°C/W

(1) For more information about traditional and new thermal metrics, see the *IC Package Thermal Metrics* application report, SPRA953.

7.5 Electrical Characteristics

over operating free-air temperature range, V_{IN} = 12 V (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
SUPPLY CURRENT						
I_{VIN}	Operating - non-switching supply current	V_{IN} current, T_A = 25°C, EN = 5 V, V_{FB} = 0.7 V		170	350	µA
I_{VINSDN}	Shutdown supply current	V_{IN} current, T_A = 25°C, EN = 0 V		3.8	10	µA
LOGIC THRESHOLD						
V_{ENH}	EN high-level input voltage	EN	1.6			V
V_{ENL}	EN low-level input voltage	EN			0.6	V
R_{EN}	EN pin resistance to GND	V_{EN} = 12 V	180	350	700	kΩ
V_{FB} VOLTAGE AND DISCHARGE RESISTANCE						
V_{FBTH}	V_{FB} threshold voltage	T_A = 25°C, V_O = 1.05 V, I_O = 10 mA, advanced Eco-mode™ operation		606		mV
		T_A = 25°C, V_O = 1.05 V, continuous mode operation	593	600	607	
		T_A = –40°C to 85°C , V_O = 1.05V, continuous mode operation[1]	588	600	612	
I_{VFB}	V_{FB} input current	V_{FB} = 0.7 V, T_A = 25°C		0	±0.15	µA

(1) Not production tested.

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Electrical Characteristics (continued)

over operating free-air temperature range, V_{IN} = 12 V (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
SW DISCHARGE						
I_{Dischg}	SW discharge current	EN=0V SW=1V, T_A = 25°C	1.0	1.5		mA
V_{REG5} OUTPUT						
V_{VREG5}	V_{REG5} output voltage	T_A = 25°C, 6.0 V < V_{IN} < 18 V, 0 < I_{VREG5} < 5 mA	5.2	5.5	5.7	V
I_{VREG5}	Output current	V_{IN} = 6 V, V_{REG5} = 4.0 V, T_A = 25°C	20			mA
MOSFET						
$R_{DS(on)h}$	High side switch resistance	25°C, V_{BST} - SW = 5.5 V		68		mΩ
$R_{DS(on)l}$	Low side switch resistance	25°C		37		mΩ
CURRENT LIMIT						
I_{ocl}	Current limit	L out = 1.5 µH (1)	4.8	5.6	7.0	A
THERMAL SHUTDOWN						
T_{SDN}	Thermal shutdown threshold	Shutdown temperature (1)		165		°C
		Hysteresis (1)		35		
ON-TIME TIMER CONTROL						
t_{ON}	On time	V_{IN} = 12 V, V_O = 1.05 V		150		ns
$t_{OFF(MIN)}$	Minimum off time	T_A = 25°C, V_{FB} = 0.5 V		260	310	ns
SOFT START						
t_{ss}	Soft-start time	Internal soft-start time	0.7	1.0	1.3	ms
POWER GOOD						
V_{THPG}	PG threshold	VFB rising(good)	85%	90%	95%	
		VFB falling(Fault)		85%		
I_{PG}	IPG PG sink current	PG=0.5V	2	4		mA
OUTPUT UNDERVOLTAGE AND OVERVOLTAGE PROTECTION						
V_{OVP}	Output OVP threshold	OVP Detect (L>H)		125%		
V_{UVP}	Output UVP threshold	UVP detect (H>L)		65%		
t_{UVPDEL}	Output UVP delay	To Hiccup state		7		µs
t_{UVPEN}	Output UVP Enable delay	Relative to soft start time		x1.7		
UVLO						
UVLO	UVLO threshold	Wake up V_{REG5} voltage	3.45	3.75	4.05	V
		Hysteresis V_{REG5} voltage	0.13	0.32	0.48	

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7.6 Typical Characteristics

VIN = 12 V, TA = 25°C (unless otherwise noted)

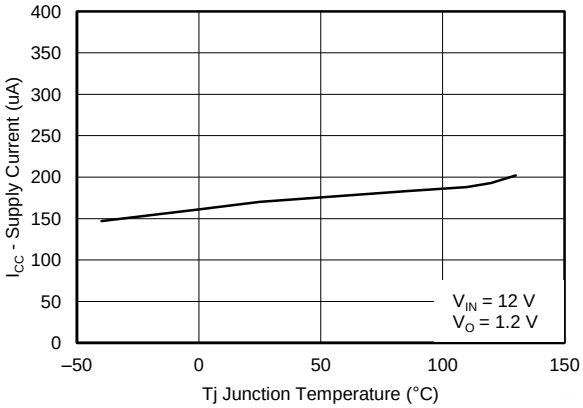

Figure 1. Supply Current vs Junction Temperature

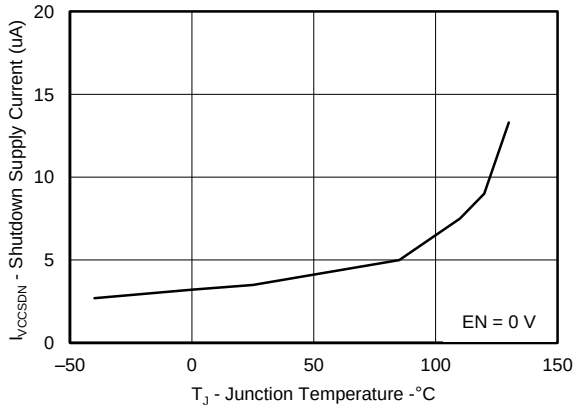

Figure 2. VIN Shutdown Current vs Junction Temperature

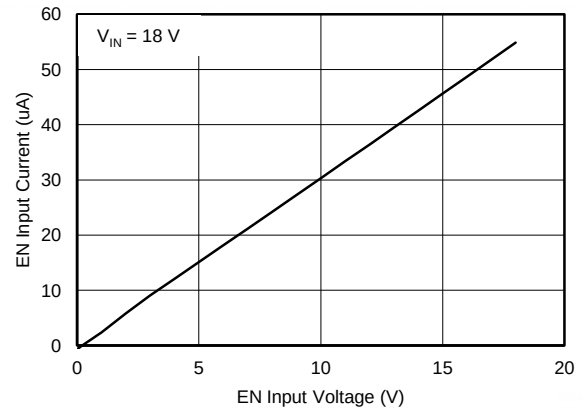

Figure 3. EN Current vs EN Voltage

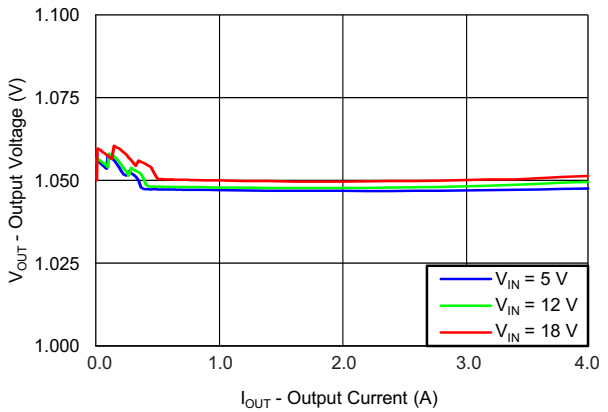

Figure 4. Output Voltage vs Output Current

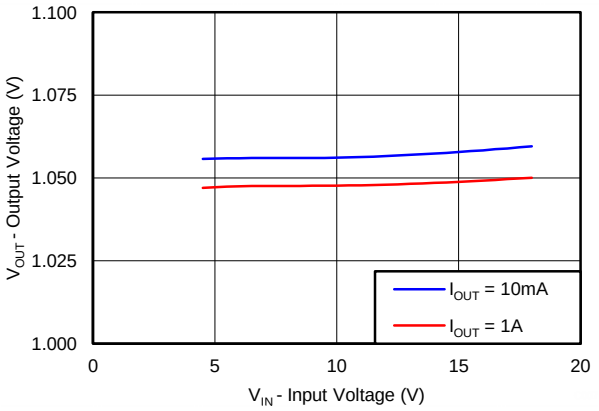

Figure 5. Output Voltage vs Input Voltage

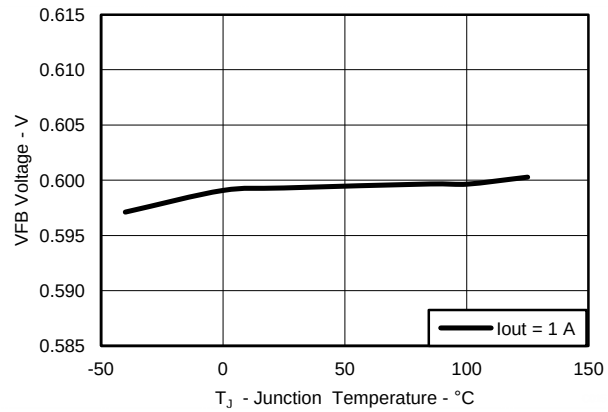

Figure 6. VFB Voltage vs Junction Temperature

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8 Detailed Description

8.1 Overview

The TPS56428 is a 4-A synchronous step-down (buck) converter with two integrated N-channel MOSFETs. It operates using D-CAP2™ mode control. The fast transient response of D-CAP2™ control reduces the output capacitance required to meet a specific level of performance. Proprietary internal circuitry allows the use of low ESR output capacitors including ceramic and special polymer types. PG output can be used for sequence operation.

8.2 Functional Block Diagram

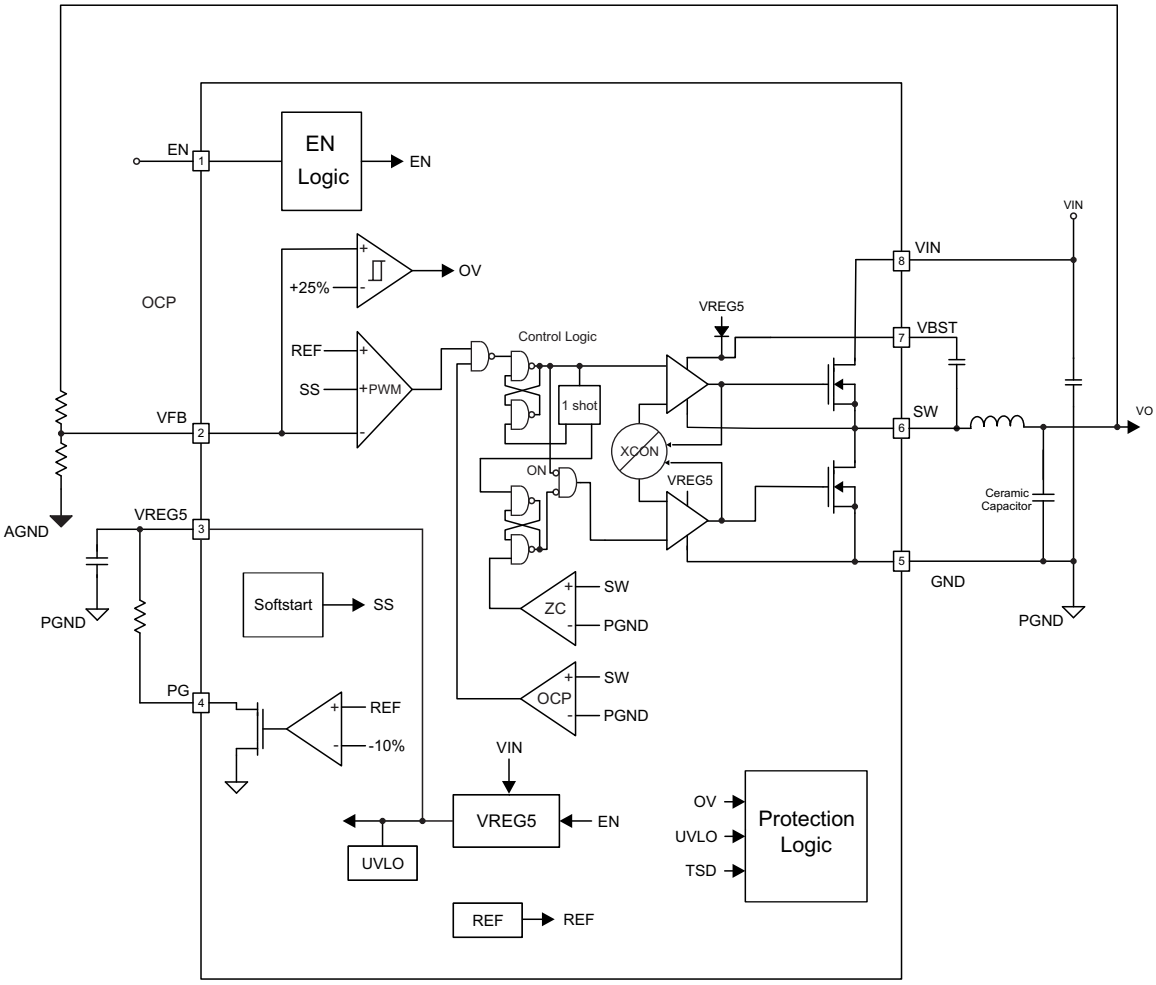

Figure 7. Functional Block Diagram

8.3 Feature Description

8.3.1 PWM Operation

The main control loop of the TPS56428 is an adaptive on-time pulse width modulation (PWM) controller that supports a proprietary D-CAP2™ mode control. D-CAP2™ mode control combines constant on-time control with an internal compensation circuit for pseudo-fixed frequency and low external component count configuration with both low ESR and ceramic output capacitors. It is stable even with virtually no ripple at the output.

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Feature Description (continued)

At the beginning of each cycle, the high-side MOSFET is turned on. This MOSFET is turned off after internal one shot timer expires. This one shot is set by the converter input voltage, VIN, and the output voltage, VO, to maintain a pseudo-fixed frequency over the input voltage range, hence it is called adaptive on-time control. The one-shot timer is reset and the high-side MOSFET is turned on again when the feedback voltage falls below the reference voltage. An internal ramp is added to reference voltage to simulate output ripple, eliminating the need for ESR induced output ripple from D-CAP2™ mode control.

8.3.2 PWM Frequency and Adaptive On-Time Control

TPS56428 uses an adaptive on-time control scheme and does not have a dedicated on board oscillator. The TPS56428 runs with a pseudo-constant frequency of 650 kHz by using the input voltage and output voltage to set the on-time one-shot timer. The on-time is inversely proportional to the input voltage and proportional to the output voltage, therefore, when the duty ratio is VOUT/VIN, the frequency is constant.

8.3.3 Advanced Auto-Skip Eco-mode™ Control

The TPS56428 is designed with advanced auto-skip Eco-mode™ to increase higher light load efficiency. As the output current decreases from heavy load condition, the inductor current is also reduced. If the output current is reduced enough, the inductor current ripple valley reaches the zero level, which is the boundary between continuous conduction and discontinuous conduction modes. The rectifying low-side MOSFET is turned off when its zero inductor current is detected. As the load current further decreases the converter run into discontinuous conduction mode. The on-time is kept approximately the same as is in continuous conduction mode. The off-time increases as it takes more time to discharge the output capacitor to the level of the reference voltage with smaller load current. The transition point to the light load operation $I_{OUT(LL)}$ current can be calculated in Equation 1.

$$I_{OUT(LL)} = \frac{1}{2 \times L \times f_{SW}} \times \frac{(V_{IN} - V_{OUT}) \times V_{OUT}}{V_{IN}} \quad (1)$$

8.3.4 Soft Start and Pre-Biased Soft Start

The TPS56428 has an internal 1.0ms soft-start. When the EN pin becomes high, internal soft-start function begins ramping up the reference voltage to the PWM comparator.

The TPS56428 contains a unique circuit to prevent current from being pulled from the output during startup if the output is pre-biased. When the soft-start commands a voltage higher than the pre-bias level (internal soft start becomes greater than feedback voltage V_{FB}), the controller slowly activates synchronous rectification by starting the first low side FET gate driver pulses with a narrow on-time. It then increments that on-time on a cycle-by-cycle basis until it coincides with the time dictated by (1-D), where D is the duty cycle of the converter. This scheme prevents the initial sinking of the pre-bias output, and ensure that the out voltage (VO) starts and ramps up smoothly into regulation and the control loop is given time to transition from pre-biased start-up to normal mode operation.

8.4 Device Functional Modes

8.4.1 Power Good

The power-good function is activated after soft start has finished. The power good function becomes active after 1.7 times soft-start time. When the output voltage becomes within –10% of the target value, internal comparators detect power good state and the power good signal becomes high. The power good output, PG is an open drain output. If the feedback voltage goes under 15% of the target value, the power good signal becomes low.

8.4.2 Output Discharge Control

TPS56428 discharges the output via SW pin when EN is low, or the controller is turned off by the protection functions(UVP, UVLO and thermal shutdown). The internal regular low-side MOSFET is not turned on during the output discharge operation to avoid the possibility of causing negative voltage at the output

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Device Functional Modes (continued)

8.4.3 Current Protection

The output over-current protection (OCP) is implemented using a cycle-by-cycle valley detect control circuit. The switch current is monitored by measuring the low-side FET switch voltage between the SW pin and GND. This voltage is proportional to the switch current. To improve accuracy, the voltage sensing is temperature compensated.

During the on time of the high-side FET switch, the switch current increases at a linear rate determined by Vin, Vout, the on-time and the output inductor value. During the on time of the low-side FET switch, this current decreases linearly. The average value of the switch current is the load current Iout. The TPS56428 constantly monitors the low-side FET switch voltage, which is proportional to the switch current, during the low-side on-time. If the measured voltage is above the voltage proportional to the current limit, an internal counter is incremented per each SW cycle and the converter maintains the low-side switch on until the measured voltage is below the voltage corresponding to the current limit at which time the switching cycle is terminated and a new switching cycle begins. In subsequent switching cycles, the on-time is set to a fixed value and the current is monitored in the same manner. If the over current condition exists for 7 consecutive switching cycles, the internal OCL threshold is set to a lower level, reducing the available output current. When a switching cycle occurs where the switch current is not above the lower OCL threshold, the counter is reset and the OCL limit is returned to the higher value.

There are some important considerations for this type of over-current protection. The load current one half of the peak-to-peak inductor current is higher than the over-current threshold also when the current is being limited, the output voltage tends to fall as the demanded load current may be higher than the current available from the converter. This may cause the output voltage to fall. . When the VFB voltage becomes lower than 65% of the target voltage, the UVP comparator detects it. After 5µs detecting the UVP voltage, device will shut down and re-start after hiccup time.

When the over current condition is removed, the output voltage returns to the regulated value.

8.4.4 UVLO Protection

Undervoltage lock out protection (UVLO) monitors the voltage of the VREG5 pin. When the VREG5 voltage is lower than UVLO threshold voltage, the TPS56428 is shut off. This protection is non-latching.

8.4.5 Thermal Shutdown

TPS56428 monitors the temperature of itself. If the temperature exceeds the threshold value (typically 165°C), the device is shut off. This is non-latch protection.

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9 Application and Implementation

NOTE

Information in the following applications sections is not part of the TI component specification, and TI does not warrant its accuracy or completeness. TI's customers are responsible for determining suitability of components for their purposes. Customers should validate and test their design implementation to confirm system functionality.

9.1 Application Information

The TPS56428 is typically used as a step down converter, which convert a voltage from 4.5V–18V to a lower voltage. WEBENCH software is available to aid in the design and analysis of circuits.

9.2 Typical Application

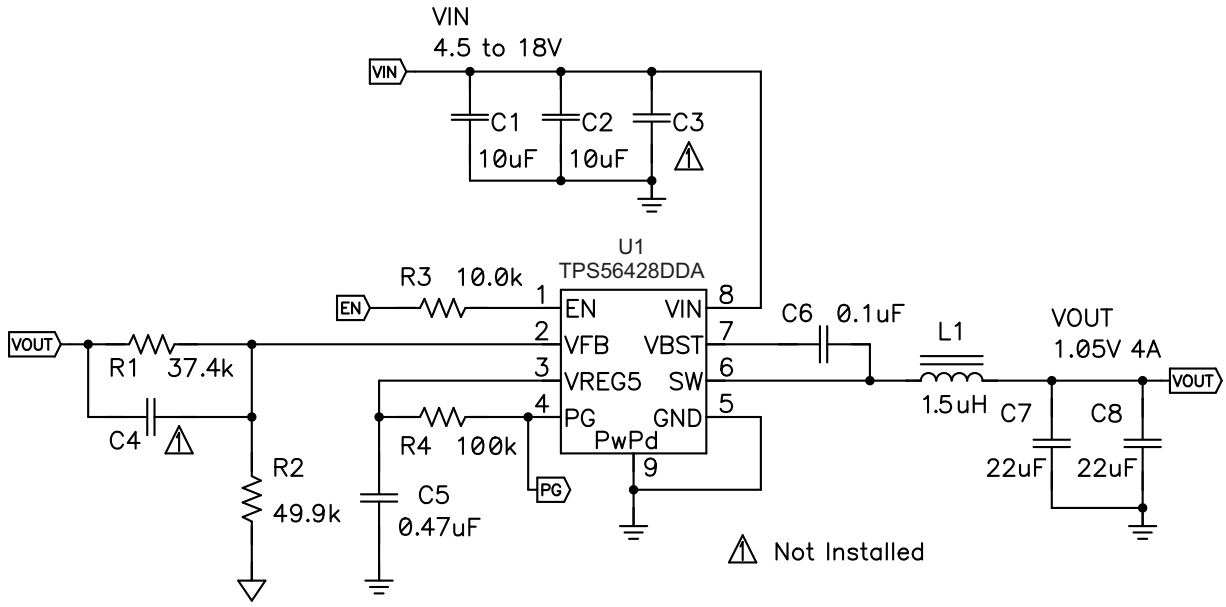

Figure 8. Schematic Diagram for This Design Example.

9.2.1 Design Requirements

To begin the design process, you must know a few application parameters:

- Input voltage range
- Output voltage
- Output current
- Output voltage ripple
- Input voltage ripple

9.2.2 Detailed Design Procedure

9.2.2.1 Output Voltage Resistors Selection

The output voltage is set with a resistor divider from the output node to the VFB pin. It is recommended to use 1% tolerance or better divider resistors. Start by using Equation 2 to calculate V_{OUT}.

To improve efficiency at very light loads consider using larger value resistors, too high of resistance will be more susceptible to noise and voltage errors from the VFB input current will be more noticeable.

$$V_{OUT} = 0.60 \times \left(1 + \frac{R1}{R2}\right) \quad (2)$$

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Typical Application (continued)

9.2.2.2 Output Filter Selection

The output filter used with the TPS56428 is an LC circuit. This LC filter has double pole at:

$$F_P = \frac{1}{2\pi \sqrt{L_{OUT} \times C_{OUT}}} \quad (3)$$

At low frequencies, the overall loop gain is set by the output set-point resistor divider network and the internal gain of the TPS56428. The low frequency phase is 180 degrees. At the output filter pole frequency, the gain rolls off at a –40 dB per decade rate and the phase drops rapidly. D-CAP2™ introduces a high frequency zero that reduces the gain roll off to –20 dB per decade and increases the phase to 90 degrees one decade above the zero frequency. The inductor and capacitor selected for the output filter must be selected so that the double pole of is located below the high frequency zero but close enough that the phase boost provided be the high frequency zero provides adequate phase margin for a stable circuit. To meet this requirement use the values recommended in Table 1.

Table 1. Recommended Component Values

Output Voltage (V)	R1 (kΩ)	R2 (kΩ)	C4 (pF)(1)			L1 (µH)			C7 + C8 (µF)
			MIN	TYP	MAX	MIN	TYP	MAX	
1	33.2	49.9	5	33	100	1.0	1.5	4.7	20 - 68
1.05	37.4	49.9	5	33	100	1.0	1.5	4.7	20 - 68
1.2	49.9	49.9	5	22	47	1.0	1.5	4.7	20 - 68
1.5	75.0	49.9	5	15	33	1.0	1.5	4.7	20 - 68
1.8	100	49.9	5	10	22	1.0	1.5	4.7	20 - 68
2.5	158	49.9	5	10	22	1.5	2.2	4.7	20 - 68
3.3	226	49.9	2	5	15	1.5	2.2	4.7	20 - 68
5	365	49.9	2	5	10	2.2	3.3	4.7	20 - 68
6.5	487	49.9	2	2	10	2.2	3.3	4.7	20 - 68

(1) Optional

For higher output voltages at or above 1.8 V, additional phase boost can be achieved by adding a feed forward capacitor (C4) in parallel with R1

The inductor peak-to-peak ripple current, peak current and RMS current are calculated using Equation 4, Equation 5 and Equation 6. The inductor saturation current rating must be greater than the calculated peak current and the RMS or heating current rating must be greater than the calculated RMS current. Use 650 kHz for f_{SW}.

Use 650 kHz for f_{SW}. Make sure the chosen inductor is rated for the peak current of Equation 5 and the RMS current of Equation 6.

$$I_{P-P} = \frac{V_{OUT}}{V_{IN(MAX)}} \times \frac{V_{IN(MAX)} - V_{OUT}}{L_O \times f_{SW}} \quad (4)$$

$$I_{PEAK} = I_O + \frac{I_{P-P}}{2} \quad (5)$$

$$I_{LO(RMS)} = \sqrt{I_O^2 + \frac{1}{12} I_{P-P}^2} \quad (6)$$

For this design example, the calculated peak current is 4.51 A and the calculated RMS current is 4.01 A. The inductor used is a TDK SPM6530-1R5M100 with a peak current rating of 11.5 A and an RMS current rating of 11 A.

The capacitor value and ESR determines the amount of output voltage ripple. The TPS56428 is intended for use with ceramic or other low ESR capacitors. Recommended values range from 20µF to 68µF. Use Equation 7 to determine the required RMS current rating for the output capacitor.

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$$I_{CO(RMS)} = \frac{V_{Ox} \times (V_{IN} - V_{OUT})}{\sqrt{12} \times V_{IN} \times L_O \times f_{SW}} \quad (7)$$

For this design two TDK C3216X5R0J226M 22µF output capacitors are used. The typical ESR is 2 mΩ each. The calculated RMS current is 0.284A and each output capacitor is rated for 4A.

9.2.2.3 Input Capacitor Selection

The TPS56428 requires an input decoupling capacitor and a bulk capacitor is needed depending on the application. A ceramic capacitor over 10µF is recommended for the decoupling capacitor. An additional 0.1 µF capacitor from pin 8 to ground is optional to provide additional frequency filtering. The capacitor voltage rating needs to be greater than the maximum input voltage.

9.2.2.4 Bootstrap Capacitor Selection

A 0.1µF ceramic capacitor must be connected between the VBST to SW pin for proper operation. It is recommended to use a ceramic capacitor.

9.2.2.5 VREG5 Capacitor Selection

A 0.47-µF ceramic capacitor must be connected between the VREG5 to GND pin for proper operation. It is recommended to use a ceramic capacitor

9.2.3 Application Curves

VIN = 12 V, TA = 25°C (unless otherwise noted)

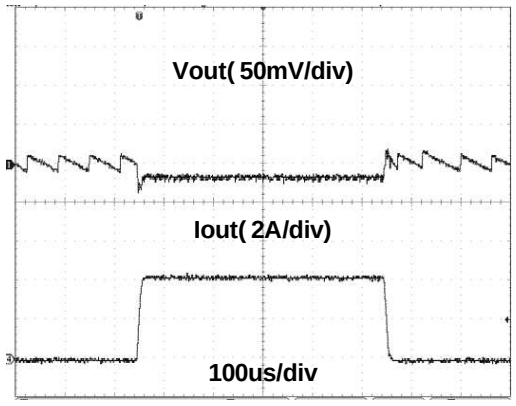

Figure 9. 1.05 V Load Transient Response

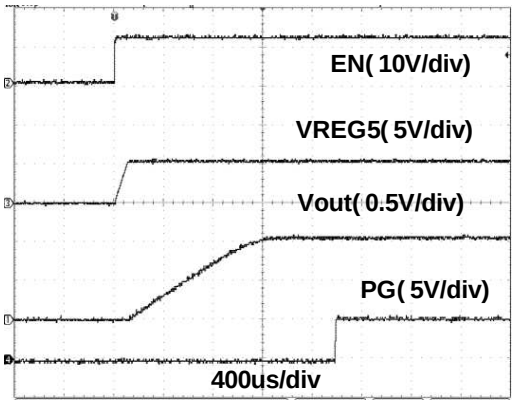

Figure 10. Slow Start

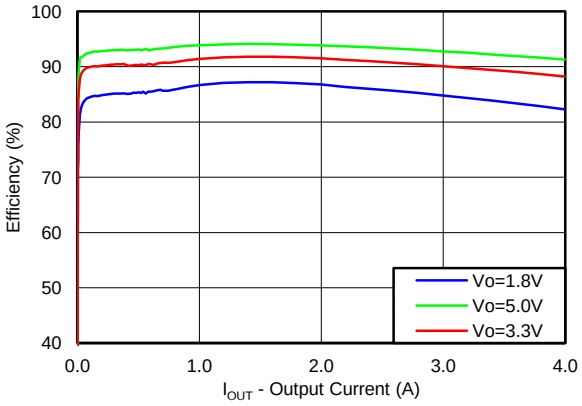

Figure 11. Efficiency vs Output Current

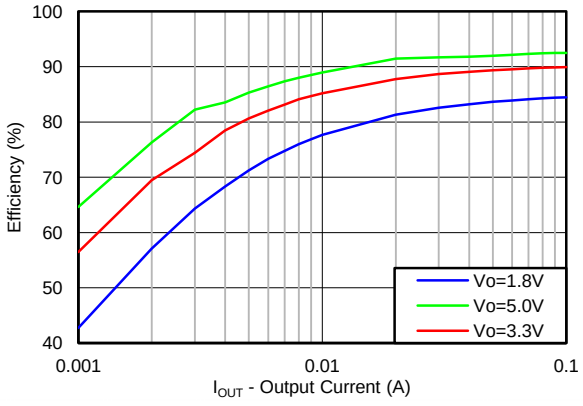

Figure 12. Efficiency vs Output Current

VIN = 12 V, TA = 25°C (unless otherwise noted)

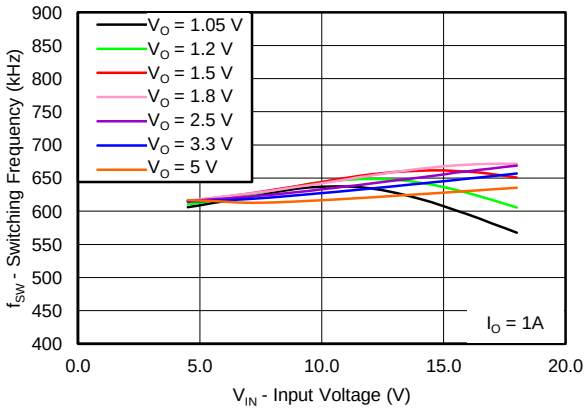

Figure 13. Switching Frequency vs Input Voltage

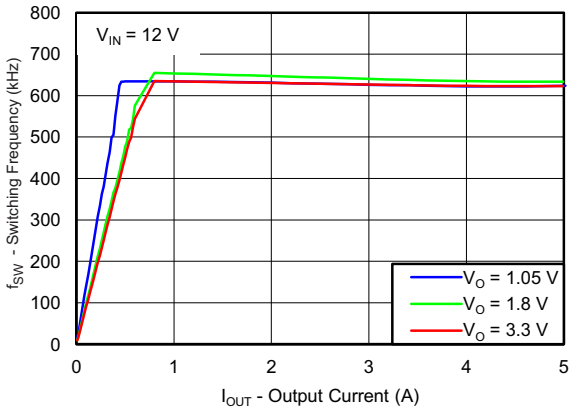

Figure 14. Output Voltage vs Output Current

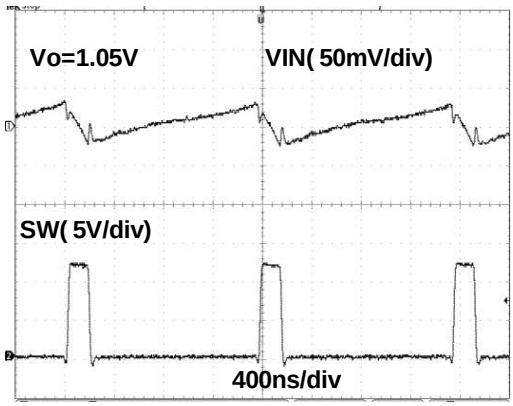

Figure 15. VIN Ripple

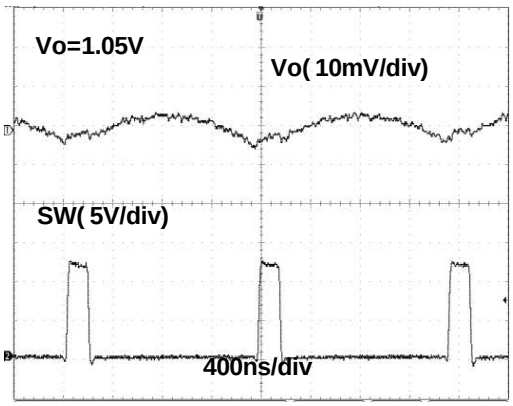

Figure 16. VOUT Ripple

10 Power Supply Recommendations

The TPS56428 designed to operate from input supply voltage in the range of 4.5 V to 18 V. Buck converters require the input voltage to be higher than the output voltage for proper operation. The maximum recommended operating duty cycle is 65%. Using that criteria, the minimum recommended input voltage is $V_{OUT} \div 0.65$.

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11 Layout

11.1 Layout Guidelines

1. The TPS56428 can supply relatively large current up to 4 A; so heat dissipation may be a concern. The top side area adjacent to the TPS56428 must be filled with ground as much as possible to dissipate heat.
2. The bottom side area directly below the IC must be a dedicated ground area; and, be directly connected to the thermal pad using vias as shown. The ground area must be as large as practical. Additional internal layers can be dedicated as ground planes and connected to vias as well.
3. Keep the input switching current loop as small as possible.
4. Keep the SW node as physically small and short as possible to minimize parasitic capacitance and inductance and to minimize radiated emissions. Kelvin connections must be brought from the output to the feedback pin of the device.
5. Keep analog and non-switching components away from switching components.
6. Make a single point connection from the signal ground to power ground.
7. Do not allow switching current to flow under the device.
8. Keep the pattern lines for VIN and PGND broad.
9. Exposed pad of device must be connected to PGND with solder.
10. VREG5 capacitor must be placed near the device, and connected PGND.
11. Output capacitor must be connected to a broad pattern of the PGND.
12. Voltage feedback loop must be as short as possible, and preferably with ground shield.
13. Lower resistor of the voltage divider which is connected to the VFB pin must be tied to SGND.
14. Providing sufficient via is preferable for VIN, SW and PGND connection.
15. PCB pattern for VIN, SW, and PGND must be as broad as possible.
16. VIN Capacitor must be placed as near as possible to the device.

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11.2 Layout Example

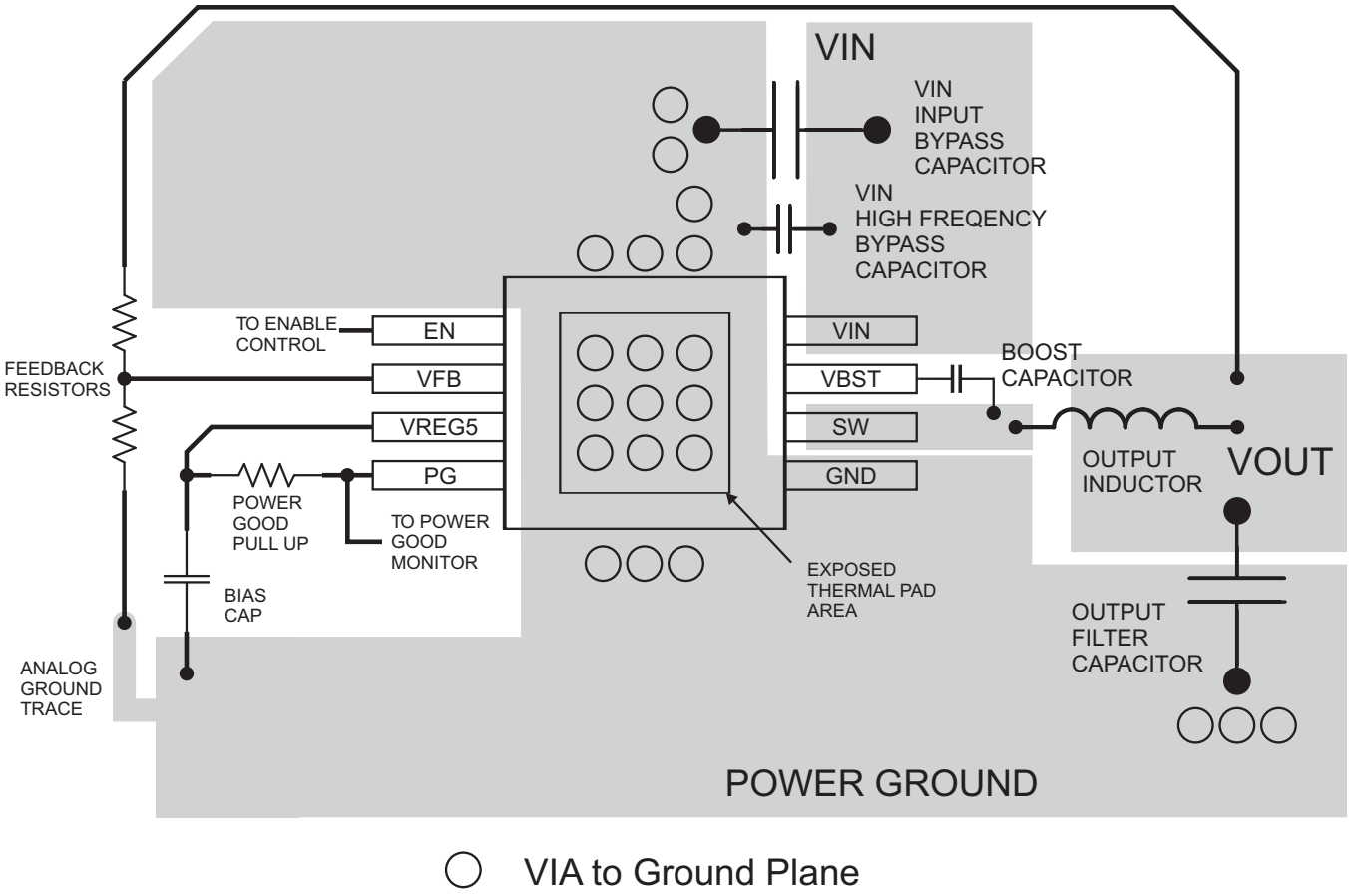

Figure 17. TPS56428 Layout – HSOP (DDA) Package

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Layout Example (continued)

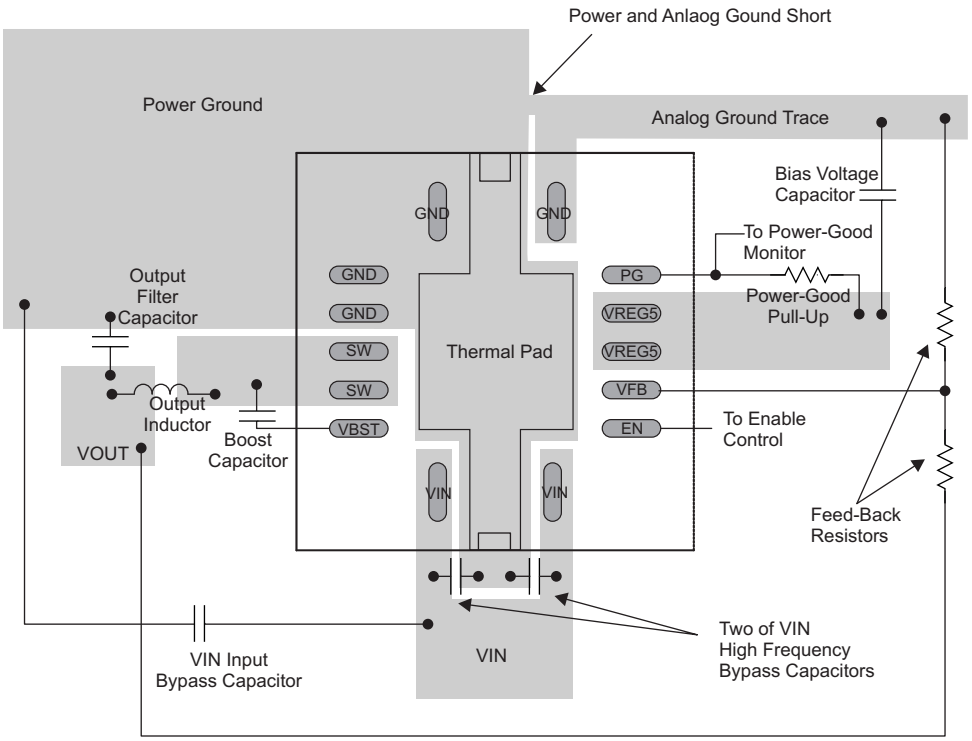

Figure 18. TPS56428 Layout – VQFN (RHL) Package

11.3 Thermal Information

This 8-pin DDA package incorporates an exposed thermal pad that is designed to be soldered directly to an external heatsink. The thermal pad must be soldered directly to the printed board (PCB). After soldering, the PCB can be used as a heatsink. In addition, through the use of thermal vias, the thermal pad can be attached directly to the appropriate copper plane shown in the electrical schematic for the device, or alternatively, can be attached to a special heatsink structure designed into the PCB. This design optimizes the heat transfer from the integrated circuit (IC).

For additional information on the exposed thermal pad and how to use the advantage of its heat dissipating abilities, refer to Technical Brief, PowerPAD™ Thermally Enhanced Package, Texas Instruments Literature No. SLMA002 and Application Brief, PowerPAD™ Made Easy, Texas Instruments Literature No. SLMA004.

The exposed thermal pad dimensions for this package are shown in Figure 19.

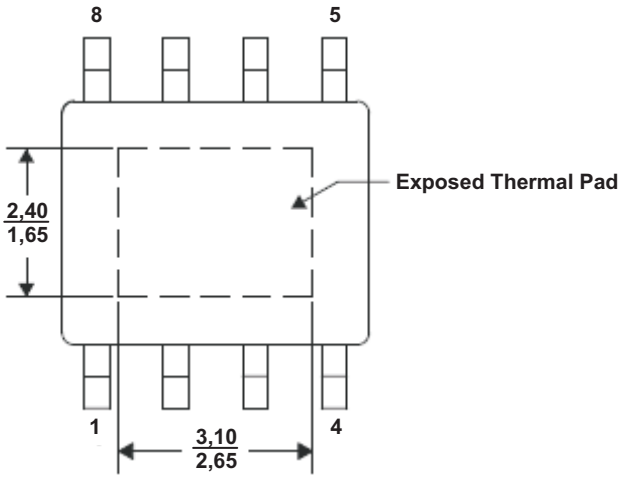

Figure 19. Thermal Pad Dimensions – HSOP (DDA) Package

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12 Device and Documentation Support

12.1 Documentation Support

12.1.1 Related Documentation

Technical Brief, PowerPAD™ Thermally Enhanced Package, SLMA002

Application Brief, PowerPAD™ Made Easy, SLMA004

12.2 Community Resources

The following links connect to TI community resources. Linked contents are provided "AS IS" by the respective contributors. They do not constitute TI specifications and do not necessarily reflect TI's views; see TI's Terms of Use.

TI E2E™ Online Community ***TI's Engineer-to-Engineer (E2E) Community.*** Created to foster collaboration among engineers. At e2e.ti.com, you can ask questions, share knowledge, explore ideas and help solve problems with fellow engineers.

Design Support ***TI's Design Support*** Quickly find helpful E2E forums along with design support tools and contact information for technical support.

12.3 Trademarks

D-CAP2, E2E are trademarks of Texas Instruments.
All other trademarks are the property of their respective owners.

12.4 Electrostatic Discharge Caution

These devices have limited built-in ESD protection. The leads should be shorted together or the device placed in conductive foam during storage or handling to prevent electrostatic damage to the MOS gates.

12.5 Glossary

SLYZ022 — *TI Glossary*.

This glossary lists and explains terms, acronyms, and definitions.

13 Mechanical, Packaging, and Orderable Information

The following pages include mechanical, packaging, and orderable information. This information is the most current data available for the designated devices. This data is subject to change without notice and revision of this document. For browser-based versions of this data sheet, refer to the left-hand navigation.

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PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead finish/ Ball material (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
TPS56428DDA	ACTIVE	SO PowerPAD	DDA	8	75	RoHS & Green	NIPDAU | SN	Level-2-260C-1 YEAR	-40 to 85	56428	Samples
TPS56428DDAR	ACTIVE	SO PowerPAD	DDA	8	2500	RoHS & Green	NIPDAU | SN	Level-2-260C-1 YEAR	-40 to 85	56428	Samples
TPS56428RHLR	ACTIVE	VQFN	RHL	14	3000	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-40 to 85	56428	Samples
TPS56428RHLT	ACTIVE	VQFN	RHL	14	250	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-40 to 85	56428	Samples

(1) The marketing status values are defined as follows:
ACTIVE: Product device recommended for new designs.
LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
PREVIEW: Device has been announced but is not in production. Samples may or may not be available.
OBSOLETE: TI has discontinued the production of the device.

(2) **RoHS:** TI defines "RoHS" to mean semiconductor products that are compliant with the current EU RoHS requirements for all 10 RoHS substances, including the requirement that RoHS substance do not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, "RoHS" products are suitable for use in specified lead-free processes. TI may reference these types of products as "Pb-Free".
RoHS Exempt: TI defines "RoHS Exempt" to mean products that contain lead but are compliant with EU RoHS pursuant to a specific EU RoHS exemption.
Green: TI defines "Green" to mean the content of Chlorine (Cl) and Bromine (Br) based flame retardants meet JS709B low halogen requirements of <=1000ppm threshold. Antimony trioxide based flame retardants must also meet the <=1000ppm threshold requirement.

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

(6) Lead finish/Ball material - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

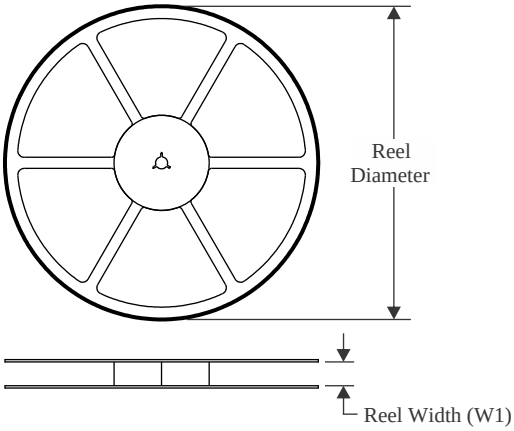
Important Information and Disclaimer: The information provided on this page represents TI's knowledge and belief as of the date that it is provided. TI bases its knowledge and belief on information provided by third parties, and makes no representation or warranty as to the accuracy of such information. Efforts are underway to better integrate information from third parties. TI has taken and

continues to take reasonable steps to provide representative and accurate information but may not have conducted destructive testing or chemical analysis on incoming materials and chemicals.
TI and TI suppliers consider certain information to be proprietary, and thus CAS numbers and other limited information may not be available for release.

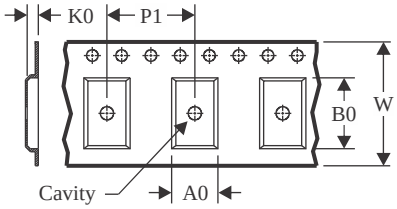
In no event shall TI's liability arising out of such information exceed the total purchase price of the TI part(s) at issue in this document sold by TI to Customer on an annual basis.

TAPE AND REEL INFORMATION

REEL DIMENSIONS

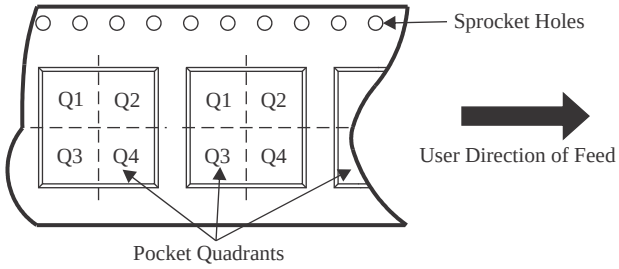


TAPE DIMENSIONS



A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

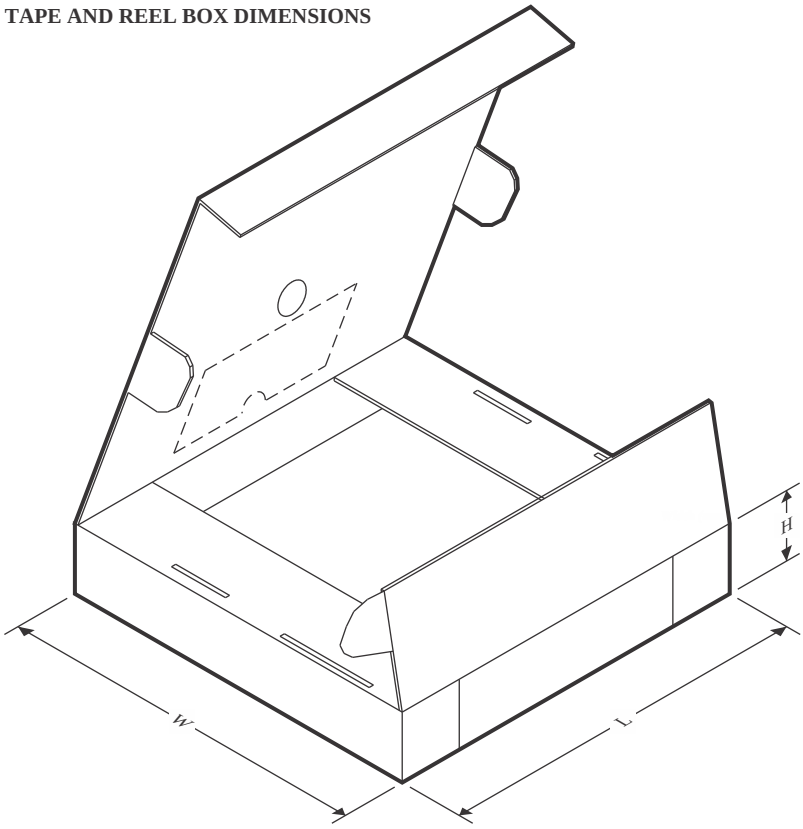
QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
TPS56428RHLR	VQFN	RHL	14	3000	330.0	12.4	3.75	3.75	1.15	8.0	12.0	Q2
TPS56428RHLT	VQFN	RHL	14	250	180.0	12.4	3.75	3.75	1.15	8.0	12.0	Q2

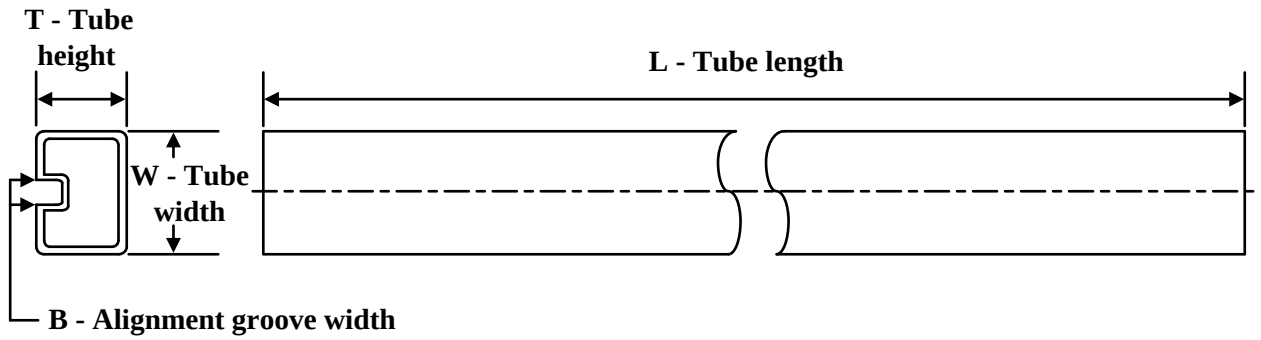
TAPE AND REEL BOX DIMENSIONS



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
TPS56428RHLR	VQFN	RHL	14	3000	335.0	335.0	25.0
TPS56428RHLT	VQFN	RHL	14	250	182.0	182.0	20.0

TUBE



*All dimensions are nominal

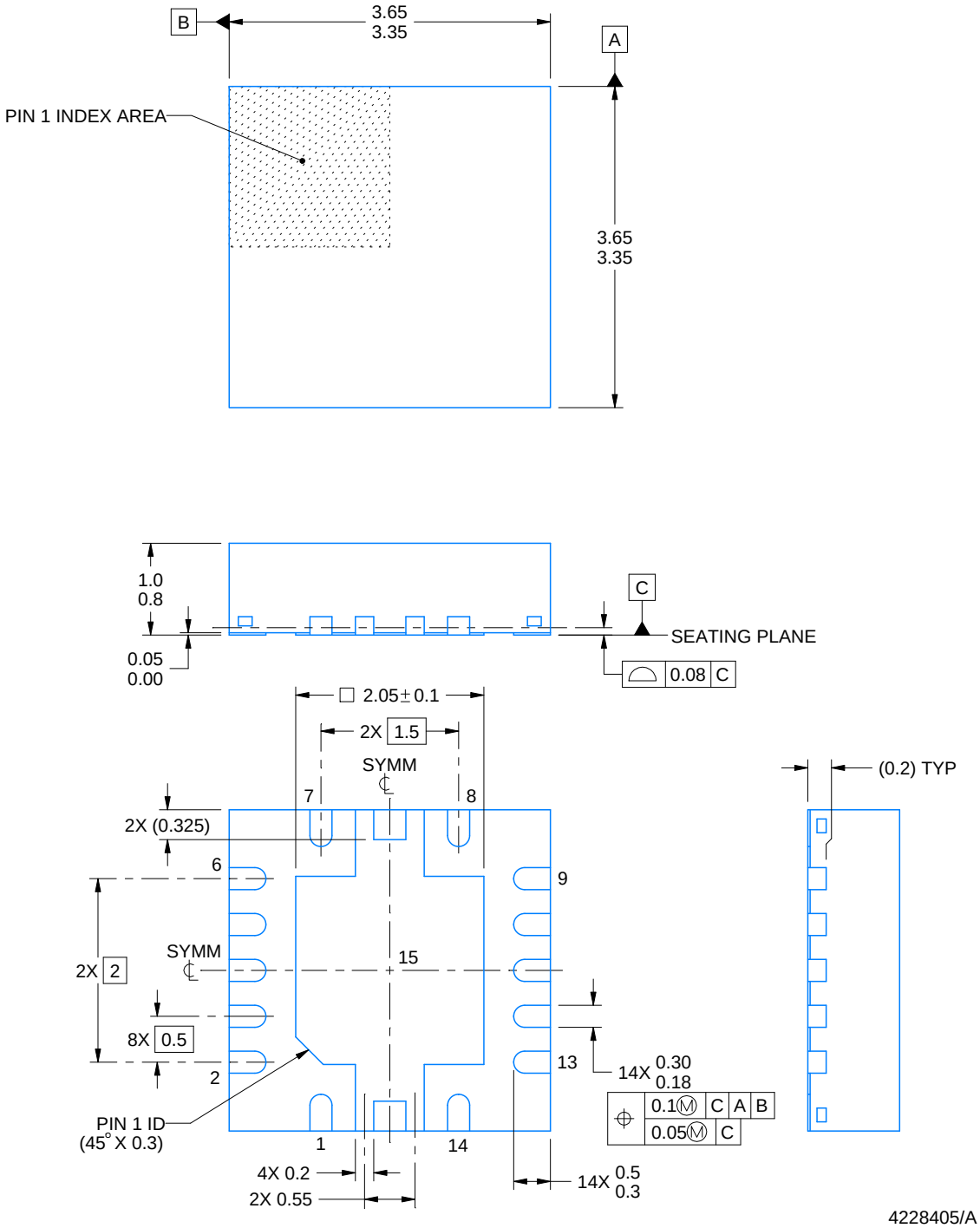
Device	Package Name	Package Type	Pins	SPQ	L (mm)	W (mm)	T (µm)	B (mm)
TPS56428DDA	DDA	HSOIC	8	75	517	7.87	635	4.25

PACKAGE OUTLINE

RHL0014A

VQFN - 1 mm max height

PLASTIC QUAD FLATPACK - NO LEAD



NOTES:

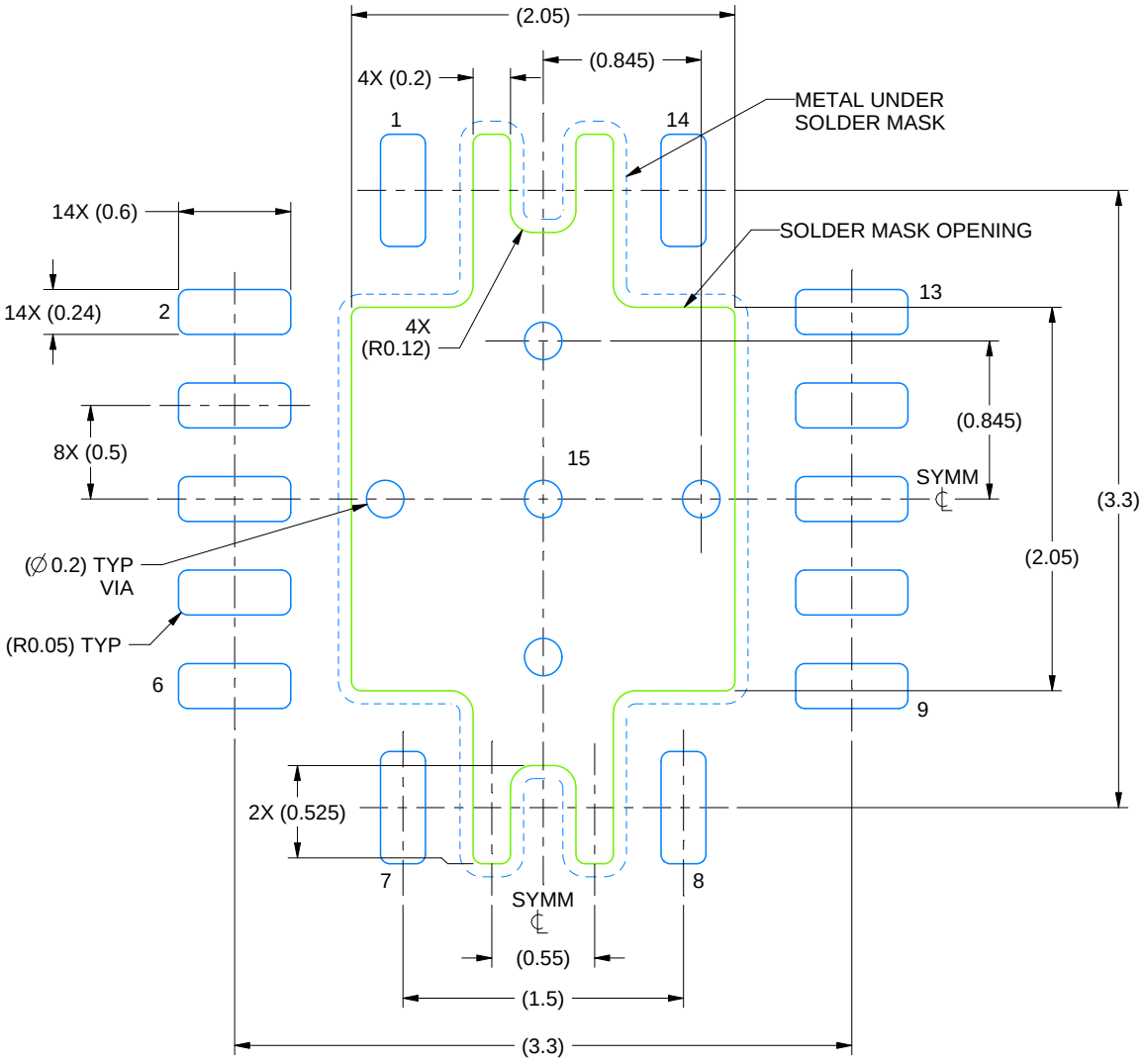
1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. The package thermal pad must be soldered to the printed circuit board for thermal and mechanical performance.

EXAMPLE BOARD LAYOUT

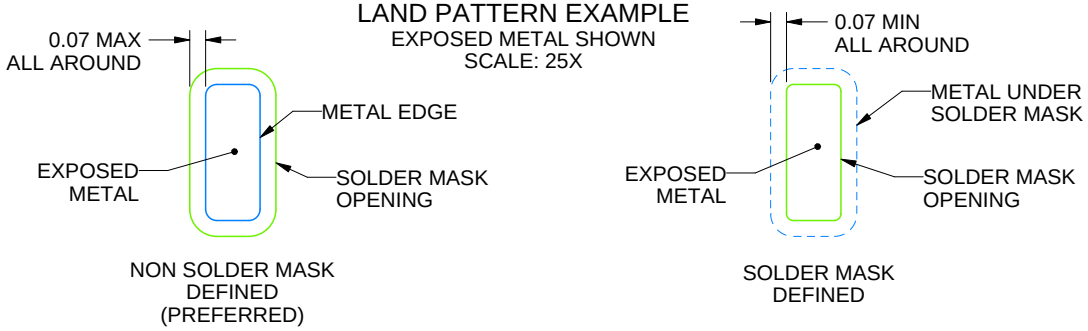
RHL0014A

VQFN - 1 mm max height

PLASTIC QUAD FLATPACK - NO LEAD



LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE: 25X

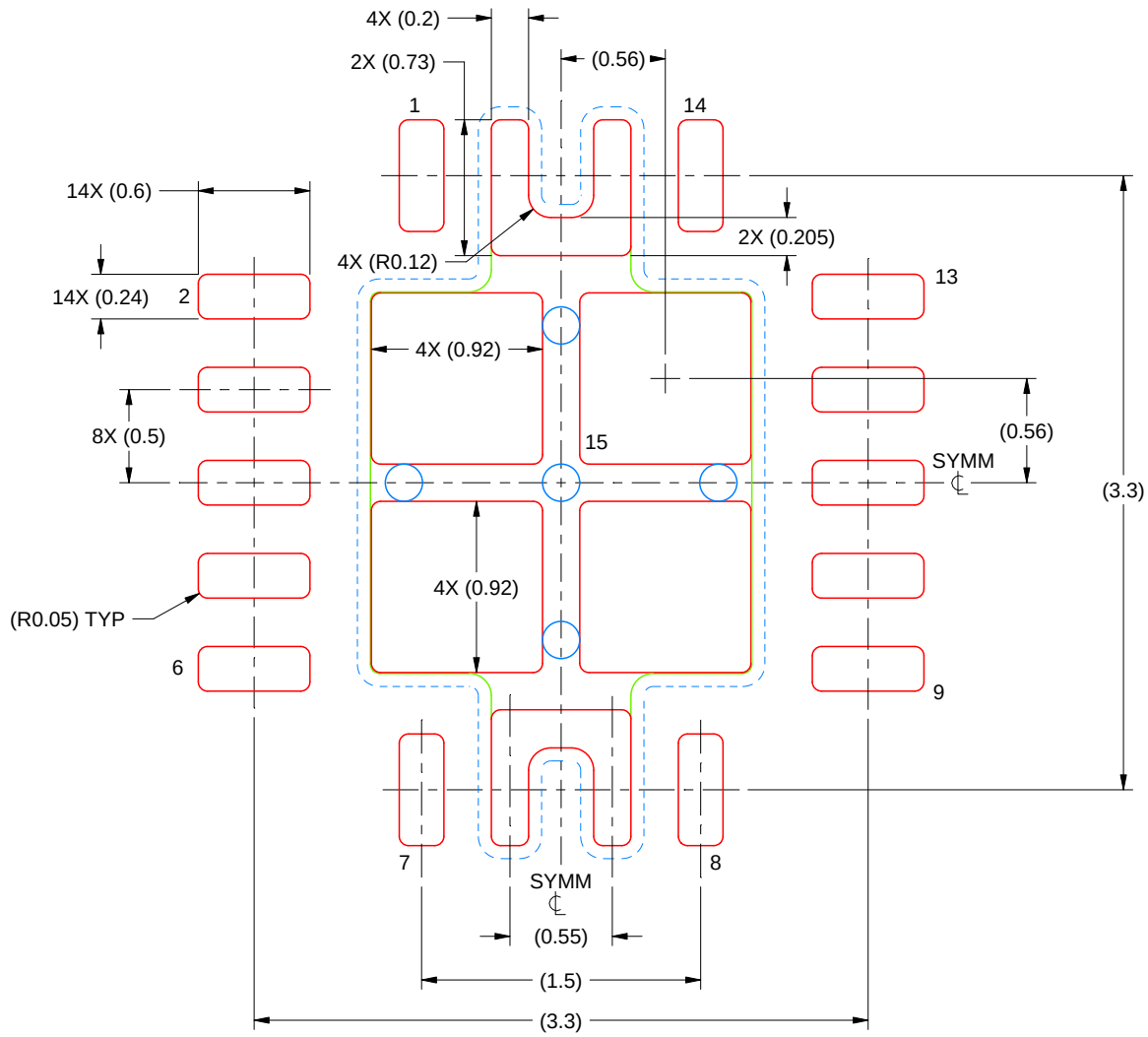


SOLDER MASK DETAILS

4228405/A 01/2022

NOTES: (continued)

4. This package is designed to be soldered to a thermal pad on the board. For more information, see Texas Instruments literature number SLUA271 (www.ti.com/lit/slua271).
5. Solder mask tolerances between and around signal pads can vary based on board fabrication site.
6. Vias are optional depending on application, refer to device data sheet. If any vias are implemented, refer to their locations shown on this view. It is recommended that vias under paste be filled, plugged or tented.



SOLDER PASTE EXAMPLE
BASED ON 0.125 mm THICK STENCIL

EXPOSED PAD
79% PRINTED COVERAGE BY AREA
SCALE: 25X

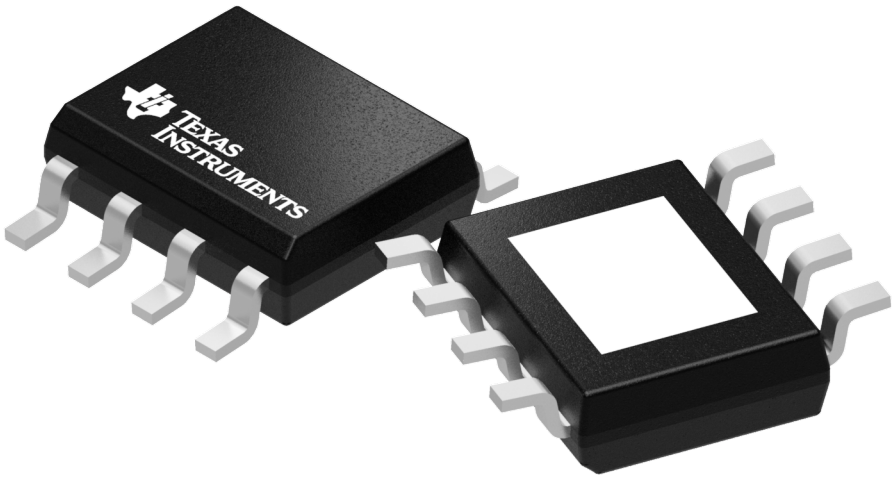
4228405/A 01/2022

NOTES: (continued)

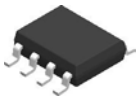
7. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.

DDA 8 PowerPAD™ SOIC - 1.7 mm max height

PLASTIC SMALL OUTLINE



Images above are just a representation of the package family, actual package may vary.
Refer to the product data sheet for package details.

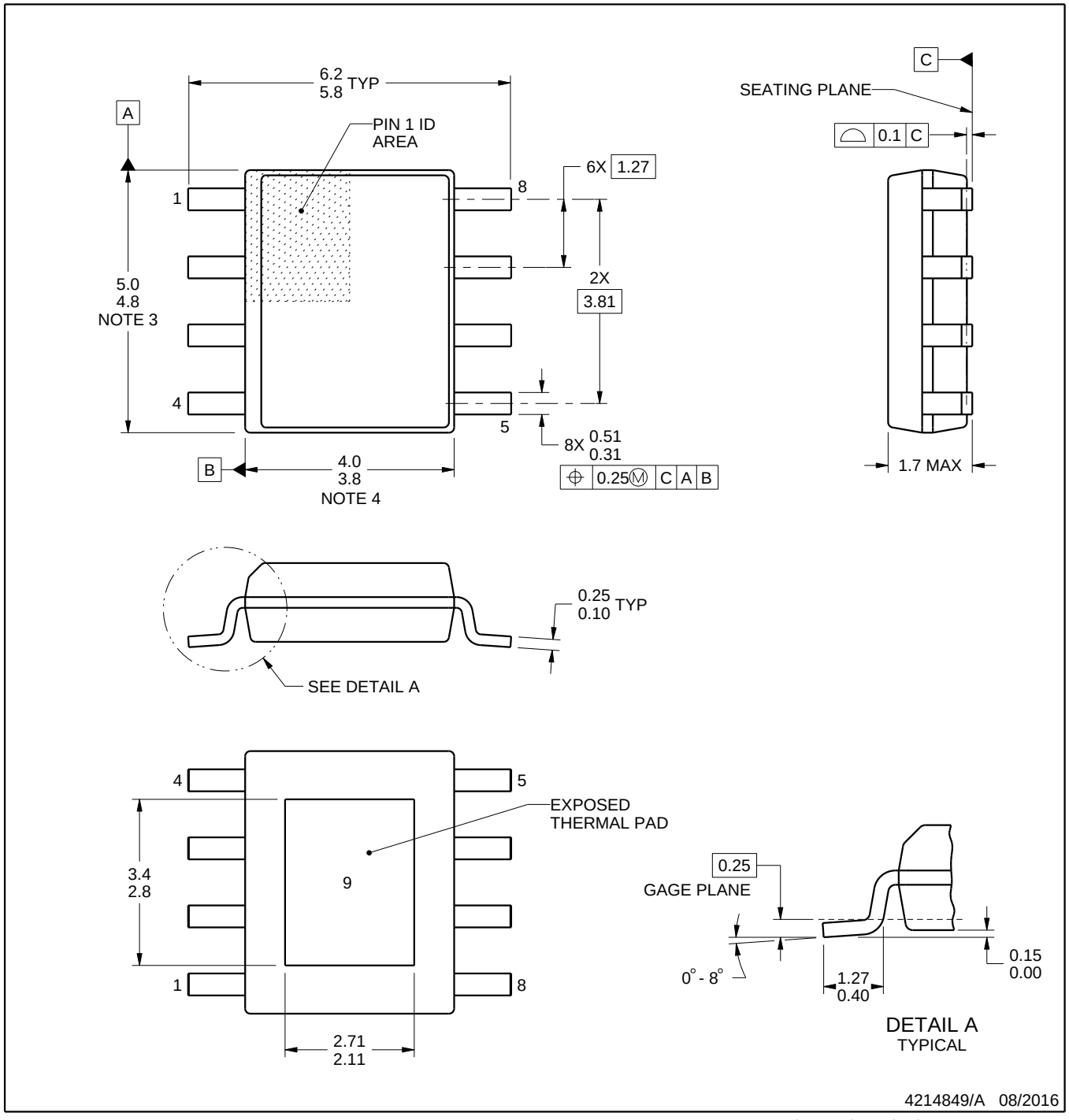


PACKAGE OUTLINE

DDA0008B

PowerPAD™ SOIC - 1.7 mm max height

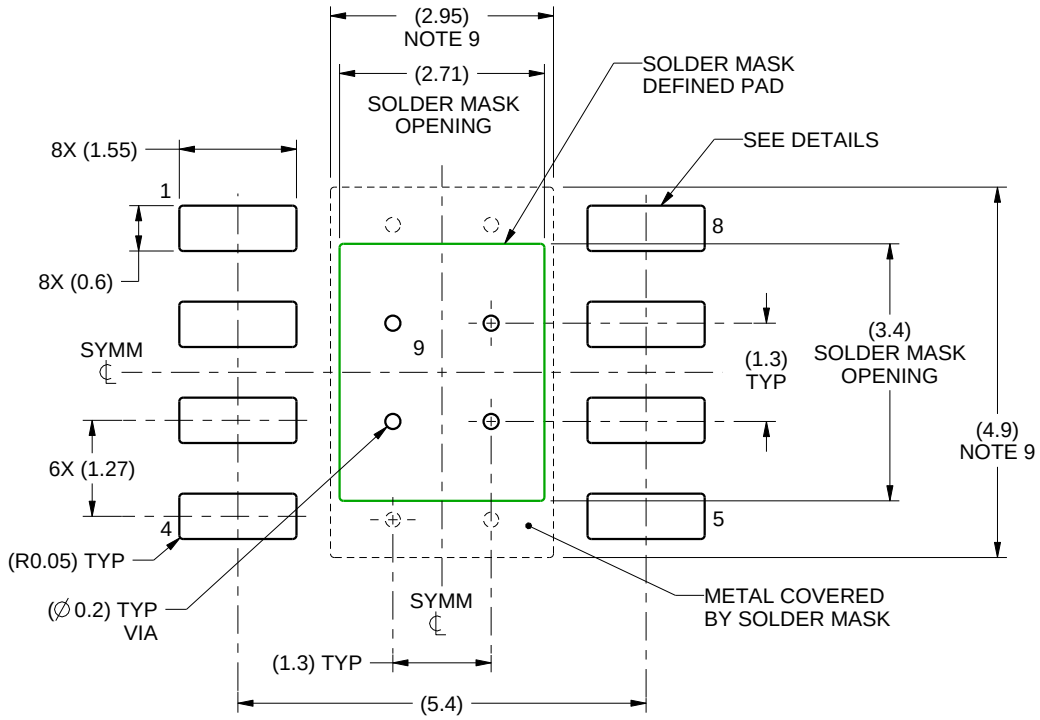
PLASTIC SMALL OUTLINE



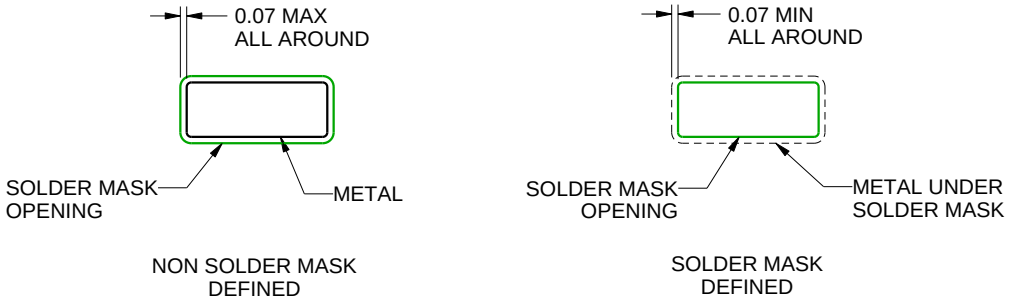
PowerPAD is a trademark of Texas Instruments.

NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.15 mm per side.
4. This dimension does not include interlead flash. Interlead flash shall not exceed 0.25 mm per side.
5. Reference JEDEC registration MS-012.



LAND PATTERN EXAMPLE
SCALE:10X



SOLDER MASK DETAILS
PADS 1-8

4214849/A 08/2016

NOTES: (continued)

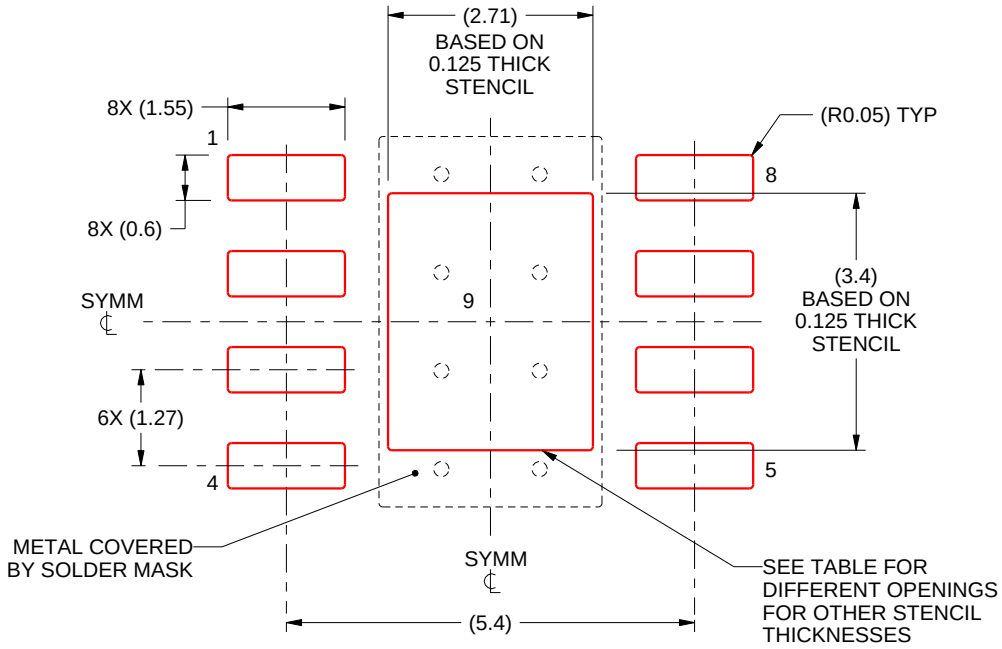
6. Publication IPC-7351 may have alternate designs.
7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.
8. This package is designed to be soldered to a thermal pad on the board. For more information, see Texas Instruments literature numbers SLMA002 (www.ti.com/lit/slma002) and SLMA004 (www.ti.com/lit/slma004).
9. Size of metal pad may vary due to creepage requirement.
10. Vias are optional depending on application, refer to device data sheet. If any vias are implemented, refer to their locations shown on this view. It is recommended that vias under paste be filled, plugged or tented.

EXAMPLE STENCIL DESIGN

DDA0008B

PowerPAD™ SOIC - 1.7 mm max height

PLASTIC SMALL OUTLINE



SOLDER PASTE EXAMPLE
EXPOSED PAD
100% PRINTED SOLDER COVERAGE BY AREA
SCALE:10X

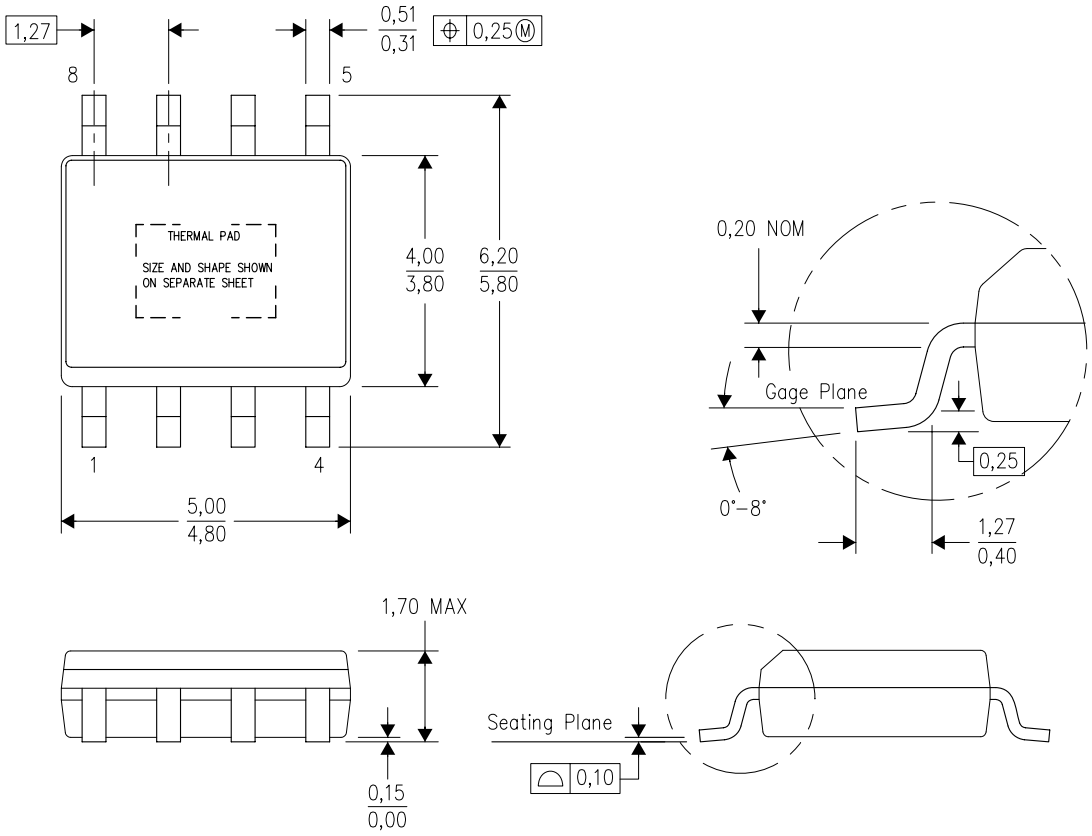
STENCIL THICKNESS	SOLDER STENCIL OPENING
0.1	3.03 X 3.80
0.125	2.71 X 3.40 (SHOWN)
0.150	2.47 X 3.10
0.175	2.29 X 2.87

4214849/A 08/2016

NOTES: (continued)

11. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
12. Board assembly site may have different recommendations for stencil design.

DDA (R–PDSO–G8) PowerPAD™ PLASTIC SMALL–OUTLINE



NOTES:
A. All linear dimensions are in millimeters. Dimensioning and tolerancing per ASME Y14.5–1994.
B. This drawing is subject to change without notice.
C. Body dimensions do not include mold flash or protrusion not to exceed 0,15.
D. This package is designed to be soldered to a thermal pad on the board. Refer to Technical Brief, PowerPad Thermally Enhanced Package, Texas Instruments Literature No. SLMA002 for information regarding recommended board layout. This document is available at www.ti.com <http://www.ti.com>.
E. See the additional figure in the Product Data Sheet for details regarding the exposed thermal pad features and dimensions.
F. This package complies to JEDEC MS–012 variation BA

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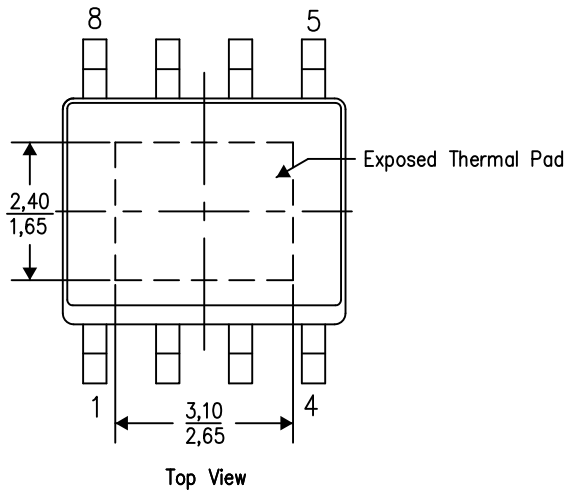
DDA (R–PDSO–G8) PowerPAD™ PLASTIC SMALL OUTLINE

THERMAL INFORMATION

This PowerPAD™ package incorporates an exposed thermal pad that is designed to be attached to a printed circuit board (PCB). The thermal pad must be soldered directly to the PCB. After soldering, the PCB can be used as a heatsink. In addition, through the use of thermal vias, the thermal pad can be attached directly to the appropriate copper plane shown in the electrical schematic for the device, or alternatively, can be attached to a special heatsink structure designed into the PCB. This design optimizes the heat transfer from the integrated circuit (IC).

For additional information on the PowerPAD package and how to take advantage of its heat dissipating abilities, refer to Technical Brief, PowerPAD Thermally Enhanced Package, Texas Instruments Literature No. SLMA002 and Application Brief, PowerPAD Made Easy, Texas Instruments Literature No. SLMA004. Both documents are available at www.ti.com.

The exposed thermal pad dimensions for this package are shown in the following illustration.



Exposed Thermal Pad Dimensions

4206322–6/L 05/12

NOTE: A. All linear dimensions are in millimeters

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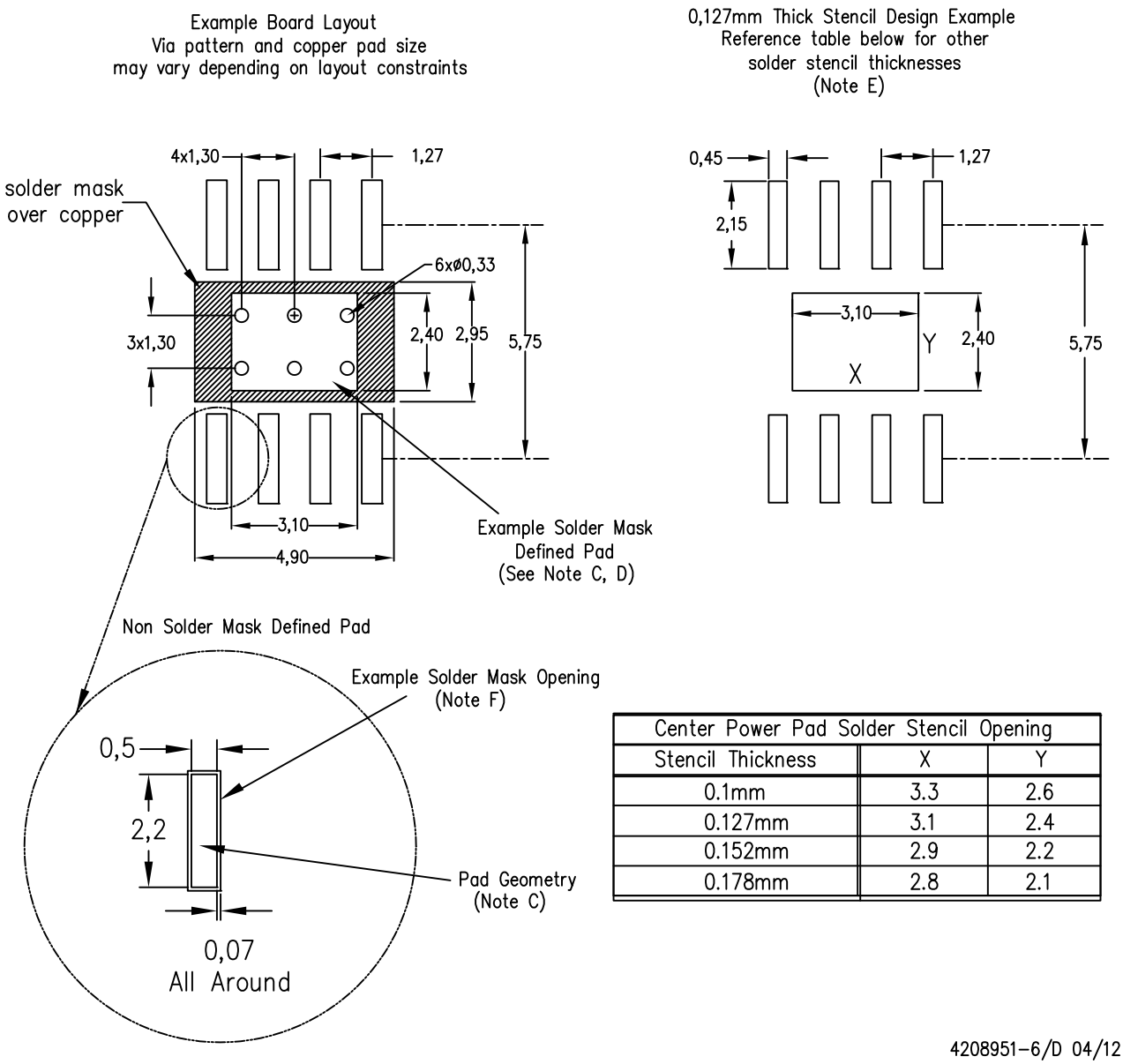

Center Power Pad Solder Stencil Opening		
Stencil Thickness	X	Y
0.1mm	3.3	2.6
0.127mm	3.1	2.4
0.152mm	2.9	2.2
0.178mm	2.8	2.1

NOTES:
A. All linear dimensions are in millimeters.
B. This drawing is subject to change without notice.
C. Publication IPC–7351 is recommended for alternate designs.
D. This package is designed to be soldered to a thermal pad on the board. Refer to Technical Brief, PowerPad Thermally Enhanced Package, Texas Instruments Literature No. SLMA002, SLMA004, and also the Product Data Sheets for specific thermal information, via requirements, and recommended board layout. These documents are available at www.ti.com <http://www.ti.com>. Publication IPC–7351 is recommended for alternate designs.
E. Laser cutting apertures with trapezoidal walls and also rounding corners will offer better paste release. Customers should contact their board assembly site for stencil design recommendations. Example stencil design based on a 50% volumetric metal load solder paste. Refer to IPC–7525 for other stencil recommendations.
F. Customers should contact their board fabrication site for solder mask tolerances between and around signal pads.

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