TEXAS INSTRUMENTS

TPS60130, TPS60131, TPS60132, TPS60133

SLVS258B – NOVEMBER 1999 – REVISED DECEMBER 2016

TPS6013x Regulated 5-V, 300-mA High-Efficiency Charge Pump DC-DC Converters

1 Features

- Up to 90% Efficiency From 2.7-V to 5.4-V Input Voltage Range Because of Special Switching Topology
- Up to 300-mA Output Current (TPS60130 and TPS60131)
- No Inductors Required, Low EMI
- Regulated 5-V ±4% Output
- Only Four External Components Required
- 60-µA Quiescent Supply Current
- 0.05-µA Shutdown Current
- Load Disconnected in Shutdown
- Thermally-Enhanced PowerPAD™ Package

2 Applications

- Battery-Powered Applications
- Three Battery Cells to 5-V Conversion or Point-of-Use 3.3-V to 5-V Conversion
- Lilon Battery to 5-V Conversion
- Portable Instruments
- Battery-Powered Microprocessor Systems
- Backup-Battery Boost Converters
- PDA's, Organizers, Laptops
- Handheld Instrumentation
- Medical Instruments (for example, Glucose Meters)
- PCMCIA and 5-V Smart Card Supply

3 Description

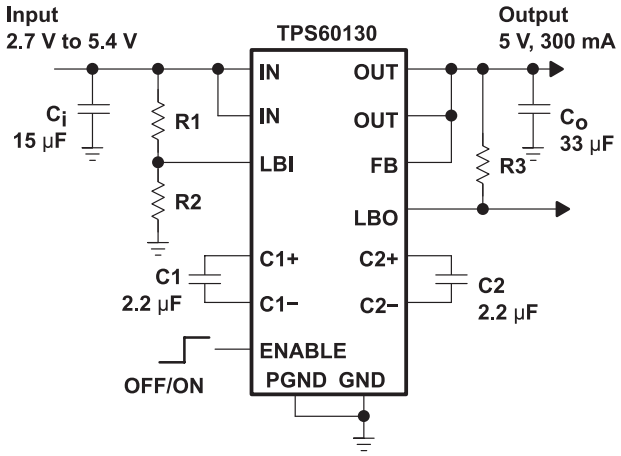
The TPS6013x step-up, regulated charge pump devices generate a 5-V ±4% output voltage from a 2.7-V to 5.4-V input voltage (three alkaline, NiCd, or NiMH batteries or one Lithium or Lilon battery). The output current is 300 mA for the TPS60130 and TPS60131, and 150 mA for the TPS60132 and TPS60133 devices, all from a 3-V input. Only four external capacitors are required to build a complete high efficiency dc/dc charge pump converter. To achieve the high efficiency over a wide input voltage range, the charge pump automatically selects between a 1.5× or doubler conversion mode. From a 3-V input, all ICs can start with full load current.

Device Information(1)

PART NUMBER	PACKAGE	BODY SIZE (NOM)
TPS6013x	HTSSOP (20)	6.50 mm × 4.40 mm

(1) For all available packages, see the orderable addendum at the end of the data sheet.

Typical Operating Circuit



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4 Revision History

NOTE: Page numbers for previous revisions may differ from page numbers in the current version.

Changes from Revision A (December 1999) to Revision B	Page
• Added *ESD Ratings* table, *Feature Description* section, *Device Functional Modes*, *Application and Implementation* section, *Power Supply Recommendations* section, *Layout* section, *Device and Documentation Support* section, and *Mechanical, Packaging, and Orderable Information* section	1
• Deleted Lead temperature (260°C maximum) from *Absolute Maximum Ratings* table	5

5 Device Options

Table 1. Available Options

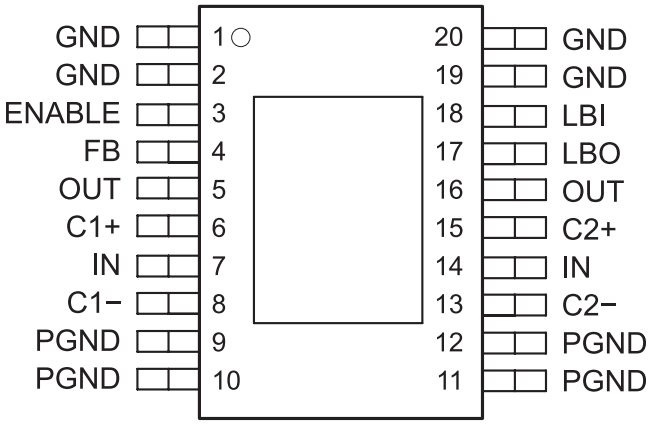
PART NUMBER	DEVICE FEATURES	
TPS60130	Low battery detector	3-cell to 5 V, 300 mA
TPS60131	Power good detector	
TPS60132	Low battery detector	3-cell to 5 V, 150 mA
TPS60133	Power good detector	

Table 2. Device Family Products

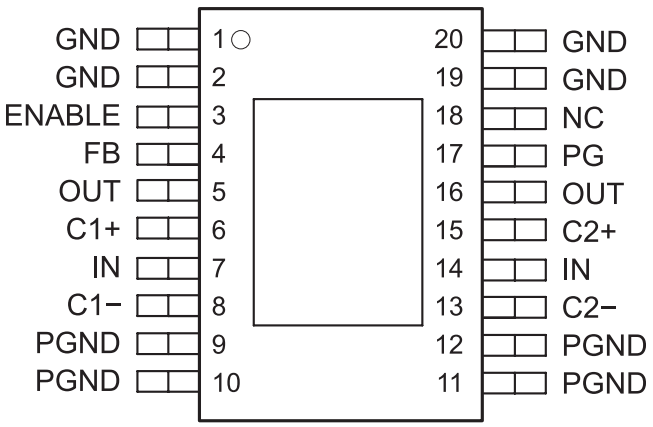
PART NUMBER	DESCRIPTION
TPS60100	Regulated 3.3-V, 200-mA low-noise charge pump dc-dc converter
TPS60101	Regulated 3.3-V, 100-mA low-noise charge pump dc-dc converter
TPS60110	Regulated 5-V, 300-mA low-noise charge pump dc-dc converter
TPS60111	Regulated 5-V, 150-mA low-noise charge pump dc-dc converter
TPS60120	Regulated 3.3-V, 200-mA high efficiency charge pump dc-dc converter with low battery comparator
TPS60121	Regulated 3.3-V, 200-mA high efficiency charge pump dc-dc converter with Power Good comparator
TPS60122	Regulated 3.3-V, 100-mA high efficiency charge pump dc-dc converter with low battery comparator
TPS60123	Regulated 3.3-V, 100-mA high efficiency charge pump dc-dc converter with Power Good comparator

6 Pin Configuration and Functions

TPS60130 and TPS60132 PWP Package
20-Pin HTSSOP
Top View



TPS60131 and TPS60133 PWP Package
20-Pin HTSSOP
Top View



Pin Functions

PIN		I/O	DESCRIPTION
NAME	NO.		
C1+	6	—	Positive pin of the flying capacitor C1
C1–	8	—	Negative pin of the flying capacitor C1
C2+	15	—	Positive pin of the flying capacitor C2
C2–	13	—	Negative pin of the flying capacitor C2
ENABLE	3	I	Enable input. Connect ENABLE to IN for normal operation. When ENABLE is a logic low, the device turns off and the supply current decreases to 0.05 µA. The output is disconnected from the input when the device is disabled.
FB	4	I	Feedback input. Connect FB to OUT as close to the load as possible to achieve best regulation. A resistive divider is on the chip to match internal reference voltage of 1.21 V.
GND	1, 2, 19, 20	—	Ground. Analog ground for internal reference and control circuitry. Connect to PGND pins through a short trace.
IN	7, 14	I	Supply input. Bypass IN to PGND with a capacitor that has half of the capacitance of the output capacitor. Connect both IN pins together through a short trace.
LBO/PG	17	O	Low battery detector output (TPS60130 and TPS60132) or Power Good output (TPS60131 and TPS60133). Open drain output of the low battery or Power Good comparator. It can sink 1 mA. TI recommends a 100-kΩ to 1-MΩ pullup resistor to OUT. Leave the pin unconnected if the low battery or Power Good detector is not used.
LBI/NC	18	I	Low battery detector input (TPS60130 and TPS60132 only). The voltage at this input is compared to the internal 1.21-V reference voltage. Connect this pin to ground if the low battery detection function is not used. On the TPS60131 and TPS60133, this pin is not connected.
OUT	5, 16	O	Regulated 5-V power output. Connect both OUT pins through a short trace and bypass OUT to GND with the output filter capacitor CO.
PGND	9, 10, 11, 12	—	Power ground. Charge-pump current flows through this pin. Connect all PGND pins together.

7 Specifications

7.1 Absolute Maximum Ratings

over operating free-air temperature range (unless otherwise noted)(1)

		MIN	MAX	UNIT
Input voltage, V_I (IN, OUT, ENABLE, FB, LBI, LBO/PG)		–0.3	5.5	V
Differential input voltage, V_{ID}	C1+, C2+ to GND	–0.3	V_O + 0.3	V
	C1−, C2− to GND	–0.3	V_I + 0.3	
Continuous total power dissipation		See *Dissipation Ratings*		
Continuous output current	TPS60130 and TPS60131		400	mA
	TPS60132 and TPS60133		200	
Maximum junction temperature			150	°C
Storage temperature, T_{stg}			150	°C

(1) Stresses beyond those listed under *Absolute Maximum Ratings* may cause permanent damage to the device. These are stress ratings only, which do not imply functional operation of the device at these or any other conditions beyond those indicated under *Recommended Operating Conditions*. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

7.2 ESD Ratings

			VALUE	UNIT
$V_{(ESD)}$	Electrostatic discharge	Human-body model (HBM), per ANSI/ESDA/JEDEC JS-001(1)	±2000	V
		Charged-device model (CDM), per JEDEC specification JESD22-C101(2)	±1000	
		Machine model (MM)	±200	

(1) JEDEC document JEP155 states that 500-V HBM allows safe manufacturing with a standard ESD control process.
(2) JEDEC document JEP157 states that 250-V CDM allows safe manufacturing with a standard ESD control process.

7.3 Recommended Operating Conditions

over operating free-air temperature range (unless otherwise noted)

			MIN	MAX	UNIT
V_I	Input voltage		2.7	5.4	V
I_O	Output current	TPS60130 and TPS60131		300	mA
		TPS60132 and TPS60133		150	
T_J	Operating junction temperature			125	°C

7.4 Thermal Information

THERMAL METRIC(1)		TPS6013x PWP (HTSSOP) 20 PINS	UNIT
$R_{\theta JA}$	Junction-to-ambient thermal resistance	178.75	°C/W
$R_{\theta JC(bot)}$	Junction-to-case (bottom) thermal resistance	3.5	°C/W

(1) For more information about traditional and new thermal metrics, see the *Semiconductor and IC Package Thermal Metrics* application report.

7.5 Electrical Characteristics

over operating free-air temperature range (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
V_I	Input voltage		2.7		5.4	V
$V_{(UVLO)}$	Input undervoltage lockout threshold	T_C = 25°C		1.6	1.8	V
$I_{O(MAX)}$	Maximum output current	TPS60130 and TPS60131	300			mA
		TPS60132 and TPS60133	150			
V_O		2.7 V < V_I < 3 V, 0 < I_O < $I_{O(MAX)}$/2, T_C = 0°C to 70°C	4.8		5.2	V
		3 V < V_I < 5 V, 0 < I_O < $I_{O(MAX)}$	4.8		5.2	
		5 V < V_I < 5.4 V, 0 < I_O < $I_{O(MAX)}$	4.8		5.25	
$I_{lkg(OUT)}$	Output leakage current	V_I = 3.6 V, $V_{(ENABLE)}$ = 0 V			1	µA
I_Q	Quiescent current (no-load input current)	V_I = 3.6 V		60	100	µA
$I_{Q(SDN)}$	Shutdown supply current	V_I = 3.6 V, V(ENABLE) = 0 V		0.05	1	µA
$f_{OSC(INT)}$	Internal switching frequency		210	320	450	kHz
V_{IL}	Enable input voltage low	V_I = 2.7 V			0.3 × V_I	V
V_{IH}	Enable input voltage high	V_I = 5.4 V	0.7 × V_I			V
$I_{lkg(ENABLE)}$	Enable input leakage current	$V_{(ENABLE)}$ = V_{GND} or V_I		0.01	0.1	µA
	Output load regulation	V_I = 3.8 V, 1 mA <I_O(maximum), T_C = 25°C		0.002%		mA
	Output line regulation	3 V < V_I < 5 V, I_O = 150 mA, T_C = 25°C		0.2%		V
	Short-circuit current limit	V_I = 3.6 V, V_O = 0 V, T_C = 25°C		115		mA
$V_{(LBITRIP)}$	LBI trip voltage (TPS60130 and TPS60132)	V_I = 2.7 V to 3.3 V, hysteresis 0.8% for rising LBI, T_C = 0°C to 70°C	1.15	1.21	1.27	V
$I_{I(LBI)}$	LBI input current (TPS60130 and TPS60132)	$V_{(LBI)}$ = 1.3 V			100	nA
$V_{O(LBO)}$	LBO output voltage low (TPS60130 and TPS60132)(1)	$V_{(LBI)}$ = 0 V, $I_{(LBO)(SINK)}$ = 1 mA			0.4	V
$I_{lkg(LBO)}$	LBO leakage current (TPS60130 and TPS60132)	$V_{(LBI)}$ = 1.3 V, $V_{(LBO)}$ = 5 V		0.01	0.1	µA
$V_{(PGTRIP)}$	Power Good trip voltage (TPS60131 and TPS60133)	T_C = 0°C to 70°C	0.86 × V_O	0.9 × V_O	0.94 × V_O	V
$V_{hys(PG)}$	Power Good trip voltage hysteresis (TPS60131 and TPS60133)	V_O ramping negative, T_C = 0°C to 70°C		0.8%		
$V_{O(PG)}$	Power Good output voltage low (TPS60131 and TPS60133)(1)	V_O = 0 V, $I_{(PG)(SINK)}$ = 1 mA			0.4	V
$I_{lkg(PG)}$	Power Good leakage current (TPS60131 andTPS60133)	V_O = 5 V, $V_{(PG)}$ = 5 V		0.01	0.1	µA

(1) During start-up the LBO and PG output signal is invalid for the first 500 µs.

7.6 Dissipation Ratings

over operating free-air temperature (unless otherwise noted)

PACKAGE	T_A ≤ 25°C POWER RATING	DERATING FACTOR ABOVE T_A = 25°C	T_A = 70°C POWER RATING	T_A = 85°C POWER RATING
FREE-AIR TEMPERATURE (see Figure 21)				
PWP	700 mW	5.6 mW/°C	448 mW	364 mW
CASE TEMPERATURE (see Figure 22)				
PWP	25 mW	285.7 mW/°C	22.9 mW	18.5 mW

7.7 Typical Characteristics

Table 3. Table of Graphs

			FIGURE
η	Efficiency	vs Output Current (TPS60130 and TPS60132)	Figure 1, Figure 2
		vs Input Voltage (TPS60130 and TPS60132)	Figure 3, Figure 4
I	Supply Current	vs Input Voltage	Figure 5
V_O	Output Voltage	vs Output Current (TPS60130 and TPS60132)	Figure 6, Figure 7
V_O	Output Voltage Ripple	vs Input Voltage (TPS60130 and TPS60132)	Figure 8, Figure 9
V_O	Output Voltage Ripple Amplitude	vs Time	Figure 10, Figure 11, and Figure 12
V_{PP}	Output Voltage Ripple Amplitude	vs Input Voltage	Figure 13
f(OSC)	Oscillator Frequency	vs Input Voltage	Figure 14
	Load Transient Response		Figure 15
	Line Transient Response		Figure 16
V_O	Output Voltage	vs Time (Start-Up Timing)	Figure 17

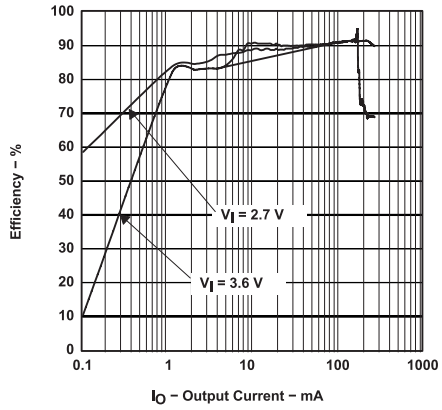


Figure 1. TPS60130 Efficiency vs Output Current

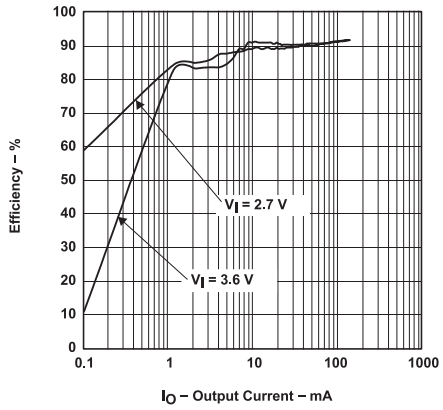


Figure 2. TPS60132 Efficiency vs Output Current

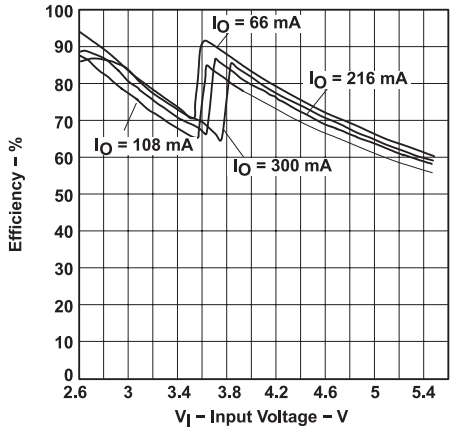


Figure 3. TPS60130 Efficiency vs Input Voltage

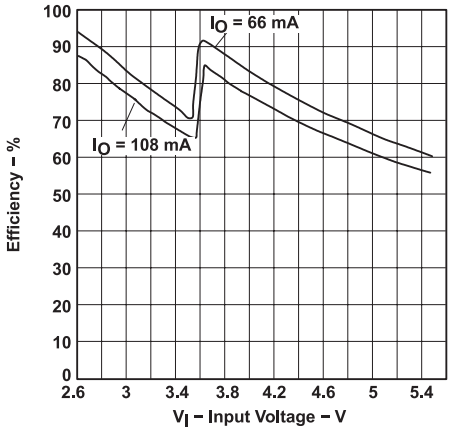


Figure 4. TPS60132 Efficiency vs Input Voltage

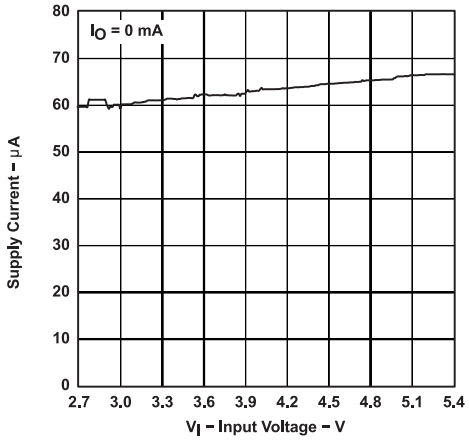


Figure 5. Supply Current vs Input Voltage

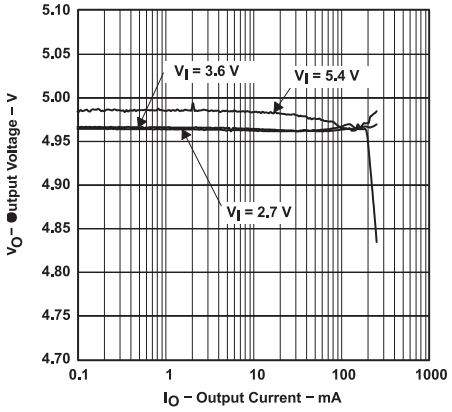


Figure 6. TPS60132 Output Voltage vs Output Current

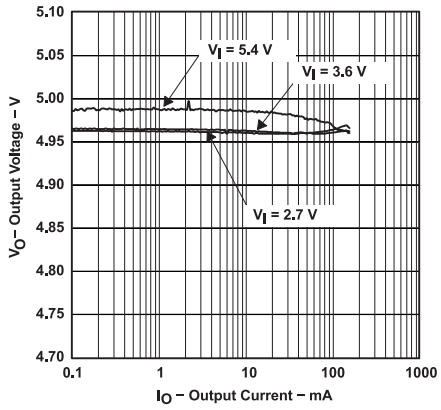


Figure 7. TPS60132 Output Voltage vs Output Current

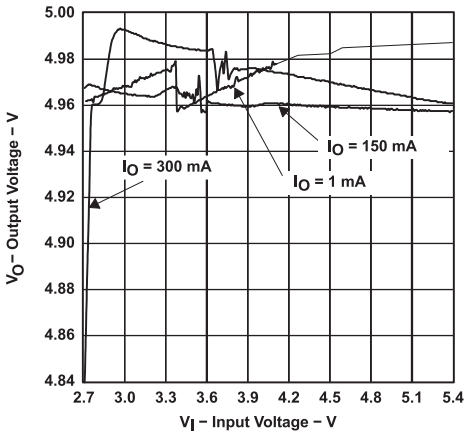


Figure 8. TPS60130 Output Voltage vs Input Voltage

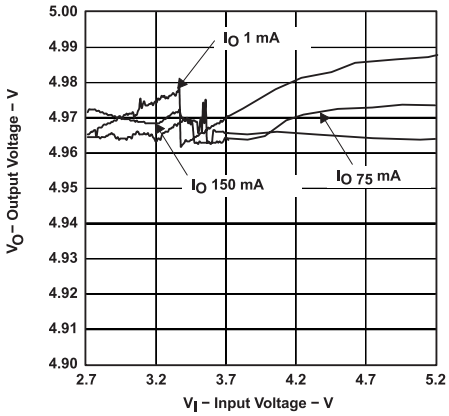


Figure 9. TPS60132 Output Voltage vs Input Voltage

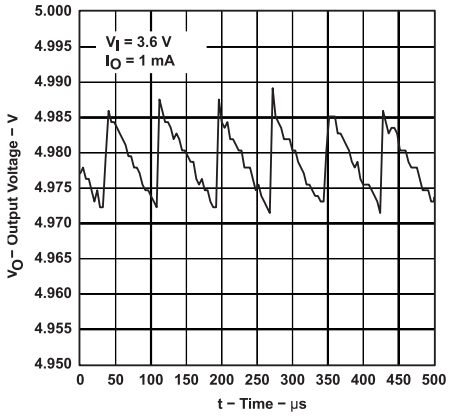


Figure 10. Output Voltage Ripple vs Time

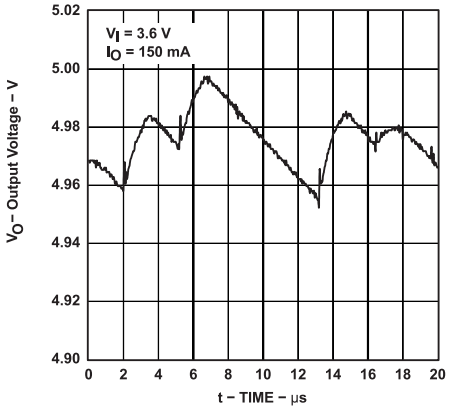


Figure 11. Output Voltage Ripple vs Time

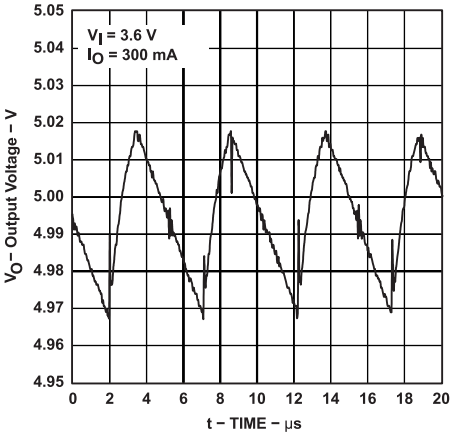


Figure 12. Output Voltage Ripple vs Time

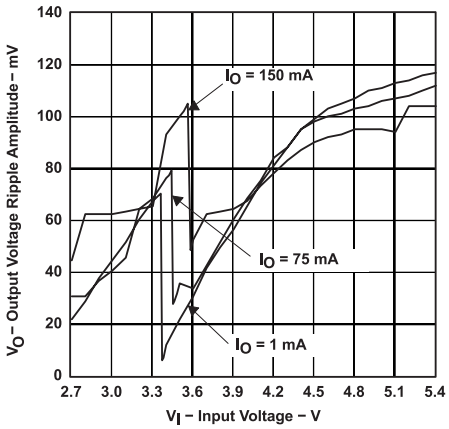


Figure 13. Output Voltage Ripple Amplitude vs Input Voltage

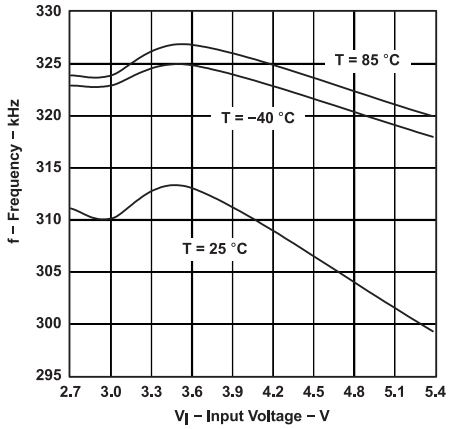


Figure 14. Oscillator Frequency vs Input Voltage

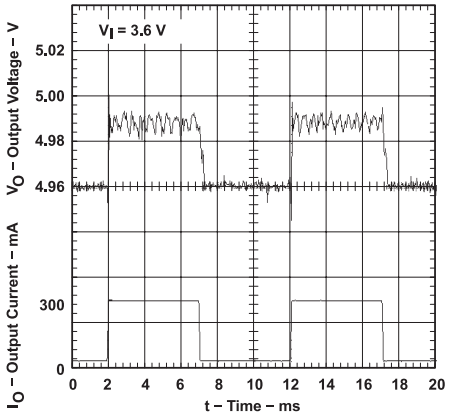


Figure 15. Load Transient Response

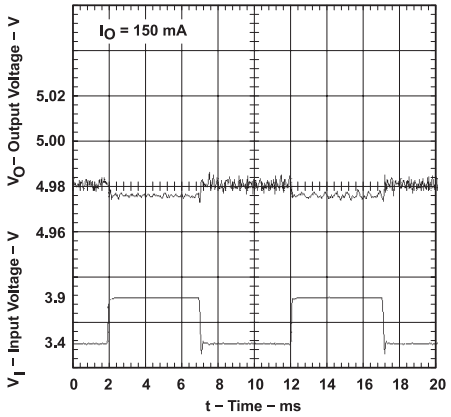


Figure 16. Line Transient Response

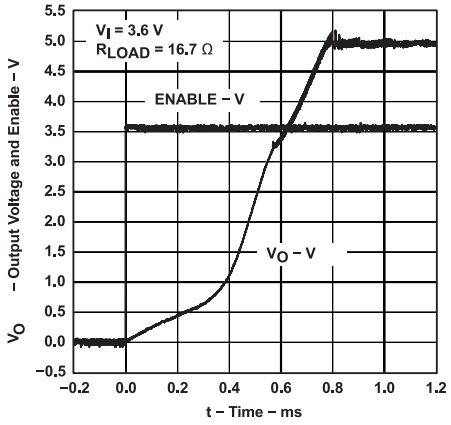


Figure 17. Output Voltage vs Time (Start-Up Timing)

8 Parameter Measurement Information

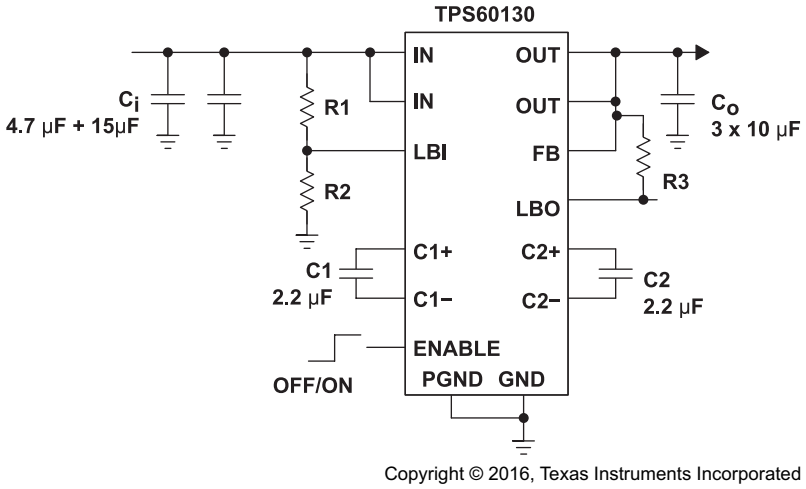


Figure 18. Circuit Used for Typical Characteristics Measurements

9 Detailed Description

9.1 Overview

The TPS6013x charge pump devices provide a regulated 5-V output from a 2.7-V to 5.4-V input. They deliver a maximum load current of 300 mA or 150 mA (respectively). Designed specifically for space-critical, battery-powered applications, the complete charge pump circuit requires four external capacitors. The circuit is optimized for efficiency over a wide input voltage range.

9.2 Functional Block Diagram

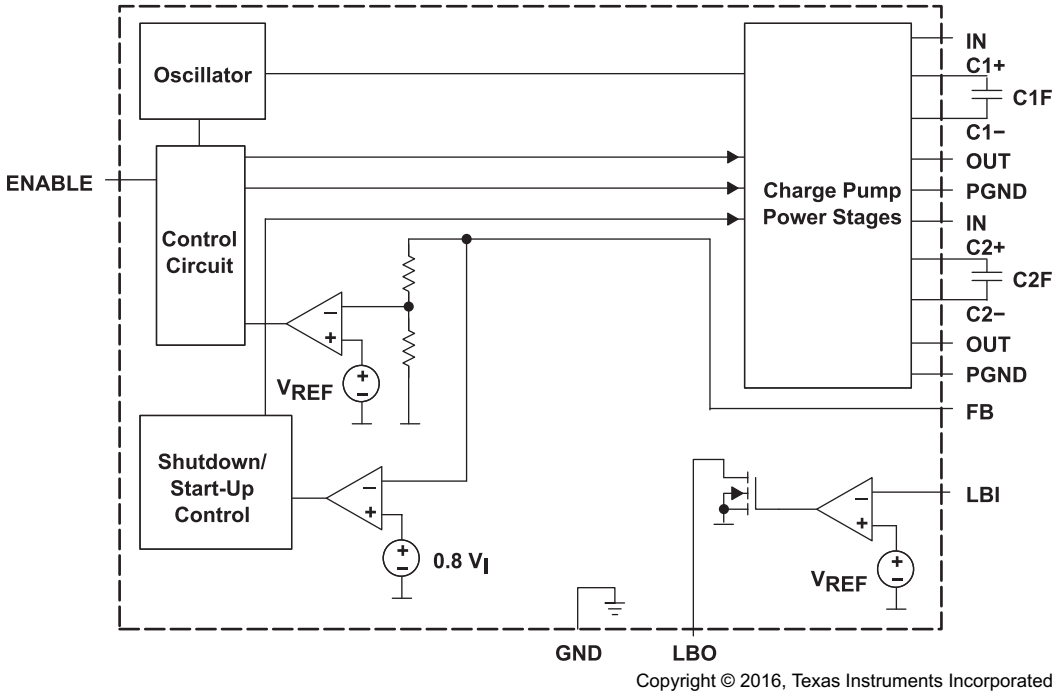


Figure 19. TPS60130 and TPS60132 Block Diagram

Functional Block Diagram (continued)

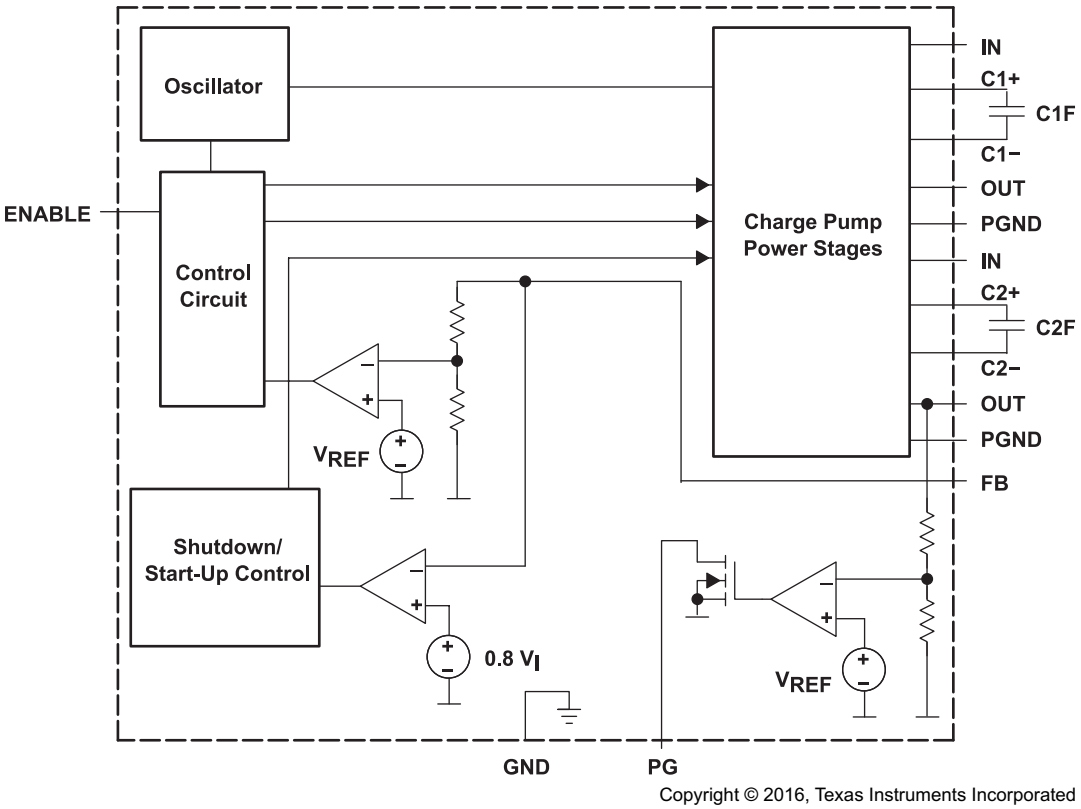


Figure 20. TPS60131 and TPS60133 Block Diagram

9.3 Feature Description

9.3.1 Operating Principle

The TPS6013x charge pumps consist of an oscillator, a 1.21-V bandgap reference, an internal resistive feedback circuit, an error amplifier, high current MOSFET switches, a shutdown/startup circuit, a low battery or Power Good comparator, and a control circuit (see Figure 19 and Figure 20).

The device consists of two single-ended charge pumps. These charge pumps are automatically configured to amplify the input voltage with a conversion factor of 1.5 or 2. The conversion ratio is dependent on the input voltage and load current. This assures high efficiency over a wide input voltage range and is further described in *Adaptive Mode Switching*.

Feature Description (continued)

9.3.2 Adaptive Mode Switching

The ON-resistance of the MOSFETs that are in the charge path of the flying capacitors is regulated when the charge pump operates in voltage doubler mode. It is changed depending on the output voltage that is fed back into the control loop. This way, the time-constant during the charging phase can be modified and increased versus a time-constant for fully switched-on MOSFETs. The ON-resistance of both switches and the capacitance of the flying capacitor define the time constant. The MOSFET switches in the discharge path of the charge pump are always fully switched on to their minimum $r_{DS(on)}$. With the time-constant during charge phase being bigger than the time constant in discharge phase, the voltage on the flying capacitors stabilizes to the lowest possible value necessary to get a stable V_O.

The voltage on the flying capacitors is measured and compared with the supply voltage V_I. If the voltage across the flying capacitors is smaller than half of the supply voltage, then the charge pump switches into the 1.5× conversion-mode. The charge pump switches back from a 1.5× conversion-mode to a voltage doubler mode if the load current in 1.5× conversion-mode can no more be delivered.

With this control mode the device runs in doubler-mode at low V_I and in 1.5× conversion-mode at high V_I to optimize the efficiency. The most desirable transfer mode is automatically selected depending on both V_I and I_L. This means that at light loads the device selects the 1.5× conversion-mode already at smaller supply voltages than at heavy loads.

The TPS60130 output voltage is regulated using the ACTIVE-CYCLE-regulation. An active cycle controlled charge pump uses two methods to control the output voltage. At high load currents it varies the on-resistances of the internal switches and keeps the ratio ON/OFF time (equal to frequency) constant. That means the charge pump runs at a fixed frequency. It also keeps the output voltage ripple as low as in linear-mode. At light loads the internal resistance and also the amount of energy transferred per pulse is fixed and the charge pump regulates the voltage by means of a variable ratio of ON-to-OFF time. In this operating point it runs like a skip mode controlled charge pump with a very high internal resistance, which also enables a low ripple in this operation mode. Because the charge pump does effectively switch at lower frequencies at light loads, it achieves a low quiescent current.

9.3.3 Pulse-Skip Mode

In pulse-skip mode, the error amplifier disables switching of the power stages when it detects an output higher than 5 V. The oscillator halts and the IC then skips switching cycles until the output voltage drops below 5 V. The error amplifier reactivates the oscillator and starts switching the power stages again. The pulse-skip regulation mode minimizes operating current, because it does not switch continuously and deactivates all functions except bandgap reference, error amplifier, and low battery or Power Good comparator when the output is higher than 5 V. When switching is disabled from the error amplifier, the load is also isolated from the input. In pulse-skip mode, a special current control circuitry, limits the peak current. This assures moderate output voltage ripple and also prevents the device from drawing excessive current spikes out of the battery.

9.3.4 Start-Up Procedure

During start-up (that is, when ENABLE is set from logic low to logic high), the output capacitor is charged up, with a limited current, until the output voltage (V_O) reaches 0.8 × V_I. When the start-up comparator detects this voltage limit, the IC begins switching. This start-up charging of the output capacitor assures a short start-up time and eliminates the requirement of a Schottky diode between IN and OUT. The IC starts with a maximum load, which is defined by a 16-Ω or 33-Ω resistor (respectively).

9.3.5 Shutdown

Driving ENABLE low places the device in shutdown mode. This disables all switches, the oscillator, and control logic. The device typically draws 0.05 µA (1 µA maximum) of supply current in this mode. Leakage current drawn from the output is as low as 1 µA maximum. The device exits shutdown once ENABLE is set to a high level. The typical no-load shutdown exit time is 10 µs. When the device is in shutdown, the load is isolated from the input.

9.3.6 Undervoltage Lockout

The TPS6013x devices have an undervoltage lockout feature that deactivates the device and places it in shutdown mode when the input voltage falls below 1.6 V.

Feature Description (continued)

9.3.7 Low Battery Detector (TPS60130 and TPS60132)

The internal low battery comparator trips at 1.21 V ±5% when the voltage on pin LBI ramps down. The battery voltage at which the comparator initiates a low battery warning at the LBO output can easily be programmed with a resistive divider as shown in Figure 34. TI recommends the sum of resistors R1 and R2 be in the range of 100 kΩ to 1 MΩ.

LBO is an open drain output. TI recommends an external pullup resistor to OUT in the 100-kΩ to 1-MΩ range. During start-up, the LBO output signal is invalid for the first 500 µs. LBO is high impedance when the device is disabled.

If the low battery comparator function is not used, connect LBI to ground and leave LBO unconnected.

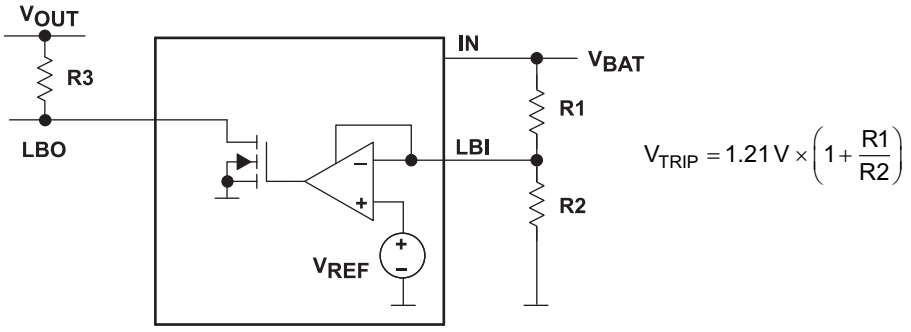


Figure 21. Programming of the Low Battery Comparator Trip Voltage

Use Equation 1 and Equation 2 to calculate the resistive divider for low battery detection with V_{LBI} = 1.15 V to 1.27 V.

$$R2 = 1\,M\Omega \times \frac{V_{LBI}}{B_{BAT}} \quad (1)$$

$$R1 = 1\,M\Omega - R2 \quad (2)$$

Use Equation 3 and Equation 4 to calculate the minimum and maximum battery voltage that triggers the low battery detector.

$$V_{BAT(min)} = V_{LBI(min)} \times \frac{R1_{(min)} + R2_{(max)}}{R2_{(max)}} \quad (3)$$

$$V_{BAT(max)} = V_{LBI(max)} \times \frac{R1_{(max)} + R2_{(min)}}{R2_{(min)}} \quad (4)$$

Table 4 lists the recommended values for the resistive divider.

Table 4. Recommended Values for the Resistive Divider From the E96 Series (±1%), V_{LBI} = 1.15 V to 1.27 V

VBAT/V	R1/kΩ	R2/kΩ	VBAT(MIN)/V		VBAT(MAX)/V	
2.7	562	453	2.548	−5.61%	2.877	6.57%
2.8	576	442	2.619	−6.47%	2.958	5.66%
2.9	590	422	2.726	−6%	3.081	6.26%
3	590	402	2.804	−6.53%	3.172	5.72%
3.1	604	383	2.928	−5.56%	3.313	6.88%
3.2	619	374	3.016	−5.76%	3.414	6.7%
3.3	649	374	3.106	−5.88%	3.518	6.62%

A 100-nF bypass capacitor must be connected in parallel to R2 if large line transients are expected. These voltage drops can inadvertently trigger the low battery comparator and produce a wrong low battery warning signal at the LBO pin.

9.3.8 Power Good Detector (TPS60131 and TPS60133)

The PG pin is an open-drain output that is pulled low when the output is out of regulation. When the output voltage rises to about 90% of its nominal voltage, Power Good output is released. PG is high impedance when the device is disabled. An external pullup resistor must be connected between PG and OUT. The pullup resistor must be in the 100-kΩ to 1-MΩ range. If the Power Good function is not used, the PG-pin must remain unconnected.

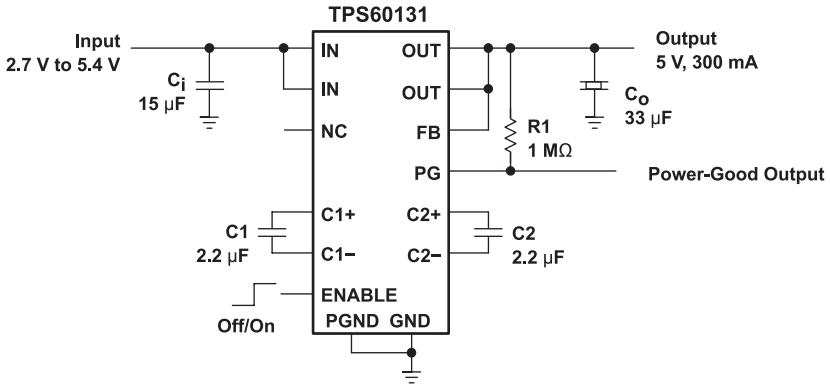


Figure 22. Typical Operating Circuit Using Power Good Comparator

10 Application and Implementation

NOTE

Information in the following applications sections is not part of the TI component specification, and TI does not warrant its accuracy or completeness. TI's customers are responsible for determining suitability of components for their purposes. Customers should validate and test their design implementation to confirm system functionality.

10.1 Application Information

The TPS6013x charge pumps provide a regulated 5-V output from a 2.7-V to 5.4-V input. They deliver a maximum load current of 300 mA or 150 mA (respectively).

10.2 Typical Applications

10.2.1 Paralleling of Two TPS6013x to Deliver 600-mA Total Output Current

Two TPS60130x devices can be connected in parallel to yield higher load currents. The circuit of Figure 23 can deliver up to 600 mA at an output voltage of 5 V.

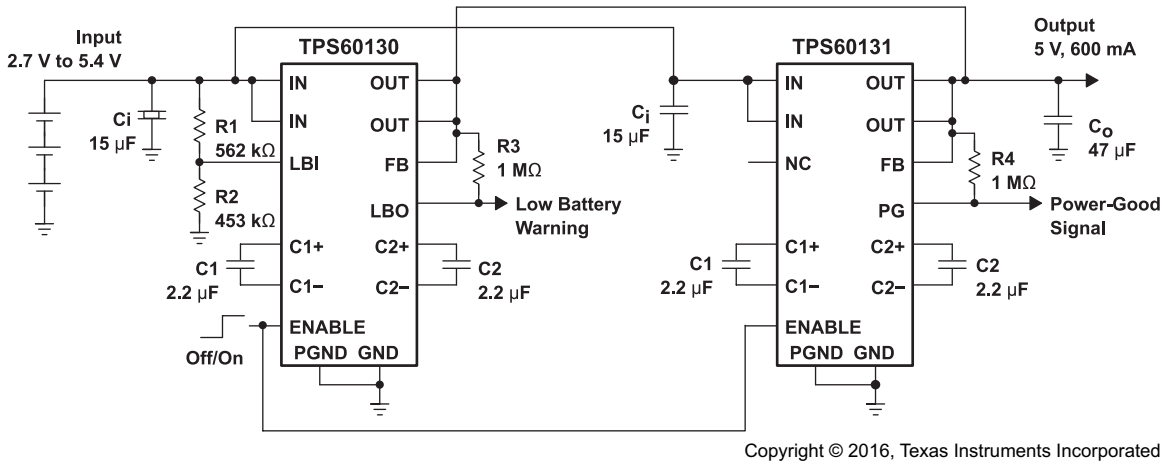


Figure 23. Paralleling of Two TPS6013x Charge Pumps

10.2.1.1 Design Requirements

The device operates over an input voltage range from 2.7 V to 5.4 V.

10.2.1.2 Detailed Design Procedure

The devices can share the output capacitors, but each one requires its own transfer capacitors and input capacitor. If both a TPS60130 and a TPS60131 are used, it is possible to monitor the battery voltage with the TPS60130 using the low battery comparator function and to supervise the output voltage with the TPS60131 using the Power Good comparator. Make the layout of the charge pumps as similar as possible, and position the output capacitor the same distance from both devices.

10.2.1.2.1 Capacitor Selection

The TPS6013x charge pump require only four external capacitors as shown in the basic application circuit. Their capacitance values and types are closely linked to the output current and output noise and ripple requirements. For lowest noise and ripple, low ESR (<0.1 Ω) capacitors must be used for input and output capacitors.

The input capacitor improves system efficiency by reducing the input impedance. It also stabilizes the input current of the power source. The input capacitor must be chosen according to the power supply used and the distance from power source to the converter IC. The input capacitor also has an impact on the output voltage ripple. The lower the ESR of the input capacitor C_i, the lower is the output ripple. TI recommends C_i be about two to four times as large as $C_{(xF)}$.

Typical Applications (continued)

The output capacitor C_o can be selected from 5-times to 50-times larger than $C_{(xF)}$, depending on the ripple tolerance. The larger C_o, the lower is the output voltage ripple. C_i and C_o can be either ceramic or low-ESR tantalum; aluminum capacitors are not recommended.

Generally, the flying capacitors $C_{(xF)}$ is the smallest. Only ceramic capacitors are recommended, due to their low ESR and because they retain their capacitance at the switching frequency. Because the device regulates the output voltage using the pulse-skip technique, a larger flying capacitor leads to a higher output voltage ripple if the size of the output capacitor is not increased. Be aware that, depending on the material used to manufacture them, ceramic capacitors might lose their capacitance over temperature. Ceramic capacitors of type X7R or X5R material keep their capacitance over temperature and voltage, whereas Z5U or Y5V-type capacitors decrease in capacitance. Table 5 lists recommended capacitor values.

Table 5. Recommended Capacitor Values

PART	V_I (V)	I_O (mA)	C_i (µF)		C_{xF} CERAMIC (X7R)	C_o (µF)		$V_{PP(TYP)}$ (V)
			TANTALUM	CERAMIC (X7R)		TANTALUM	CERAMIC (X7R)	
TPS60130, TPS60131	3.6	225	—	10	2.2	22	4.7	90
			—			—	22	60
TPS60132, TPS60133	3.6	300	—	10	2.2	33	4.7	120
			—			—	22 and 10 in parallel	45
		75	—	4.7	1	—	10	—
		150	4.7	2.2		15	22	100
			—	4.7		—	22	90

The TPS6013x devices are charge pumps that regulate the output voltage using pulse-skip regulation mode. The output voltage ripple is therefore dependent on the values and the ESR of the input, output and flying capacitors. The only possibility to reduce the output voltage ripple is to choose the appropriate capacitors. The lowest output voltage ripple can be achieved using ceramic capacitors because of their low ESR and their frequency characteristic.

Ceramic capacitors typically have an ESR that is more than 10 times lower than tantalum capacitors and they retain their capacitance at frequencies more than 10 times higher than tantalum. Many different tantalum capacitors act as an inductance for frequencies higher than 200 kHz. This behavior increases the output voltage ripple. Therefore, the best choice for a minimized ripple is the ceramic capacitor. For applications that do not require a higher performance in output voltage ripple, tantalum capacitors with a low ESR are a possibility for input and output capacitor, but a ceramic capacitor must be connected in parallel. Be aware that the ESR of tantalum capacitors is indirectly proportional to the physical size of the capacitor.

Table 5 is a good starting point for choosing the capacitors. If the output voltage ripple is too high for the application, it can be improved by selecting the appropriate capacitors. The first step is to increase the capacitance at the output. If the ripple is still too high, the second step would be to increase the capacitance at the input.

For the TPS60130 and TPS60131, the smallest board space can be achieved using Sprague's 595D-series tantalum capacitors for input and output. However, high-capacitance ceramic capacitors become competitive in package size soon.

The smallest size for the lower-current devices TPS60132 and TPS60133 can be achieved using the suggested ceramic capacitors.

Table 6 lists the manufacturers of recommended capacitors. In most applications, surface-mount tantalum capacitors is the right choice. However, ceramic capacitors provide the lowest output voltage ripple due to their typically lower ESR.

Table 6. Recommended Capacitors(1)

MANUFACTURER	PART NUMBER	CAPACITANCE	CASE SIZE	TYPE
Taiyo Yuden	LMK212BJ105KG−T	1 µF	0805	Ceramic
	LMK212BJ225MG−T	2.2 µF	0805	Ceramic
	LMK316BJ475KL−T	4.7 µF	1206	Ceramic
	LMK325BJ106MN−T	10 µF	1210	Ceramic
	LMK432BJ226MM−T	22 µF	1812	Ceramic
AVX	0805ZC105KAT2A	1 µF	0805	Ceramic
	1206ZC225KAT2A	2.2 µF	1206	Ceramic
	TPSC475035R0600	4.7 µF	Case C	Tantalum
	TPSC156025R0500	10 µF	Case C	Tantalum
	TPSC336010R0375	22 µF	Case C	Tantalum
Sprague	595D156X0016B2T	15 µF	Case B	Tantalum
	595D226X0016B2T	22 µF	Case B	Tantalum
	595D336X0016B2T	33 µF	Case B	Tantalum
	595D336X0016C2T	33 µF	Case C	Tantalum
Kemet	T494C156K010AS	15 µF	Case C	Tantalum
	T494C226K010AS	22 µF	Case C	Tantalum
	T494C336K010AS	33 µF	Case C	Tantalum

(1) Case code compatibility with EIA 535BAAC and CECC30801 molded chips.

10.2.1.3 Application Curves

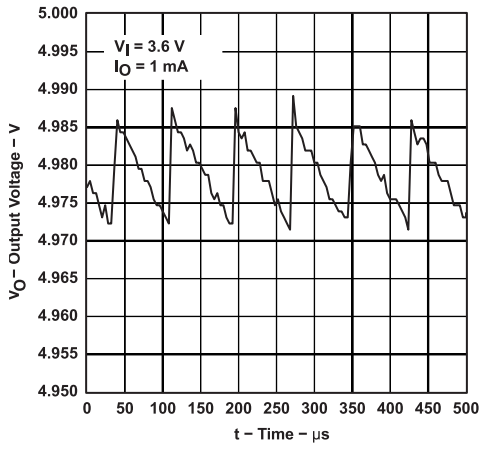


Figure 24. Output Voltage Ripple vs Time

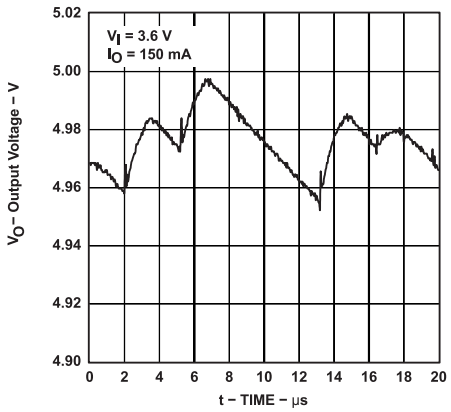


Figure 25. Output Voltage Ripple vs Time

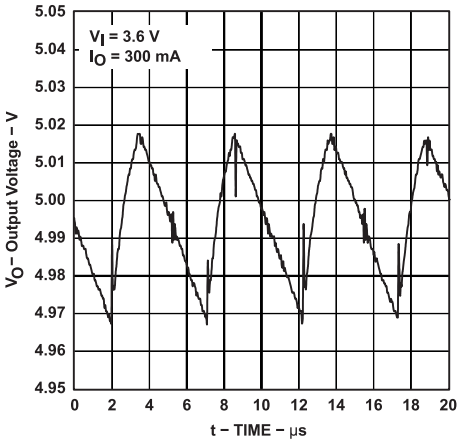


Figure 26. Output Voltage Ripple vs Time

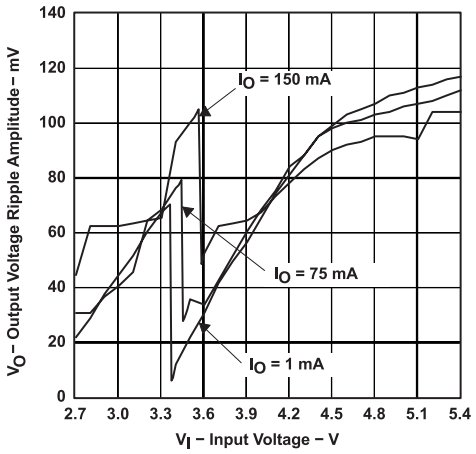


Figure 27. Output Voltage Ripple Amplitude vs Input Voltage

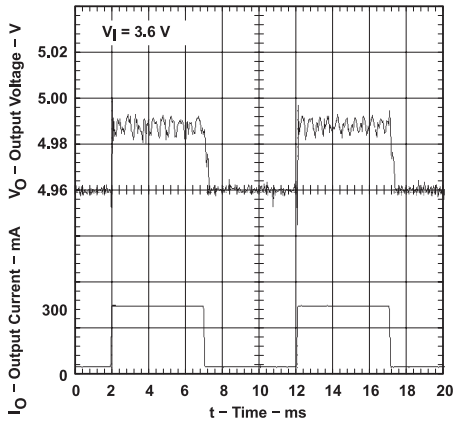


Figure 28. Load Transient Response

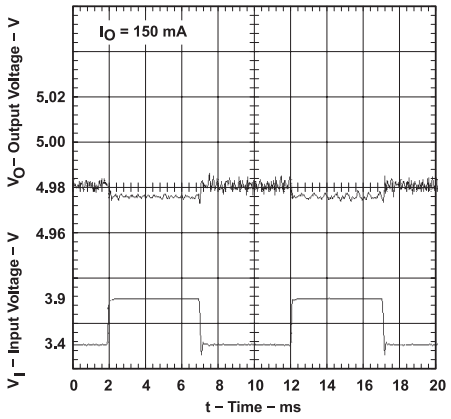


Figure 29. Line Transient Response

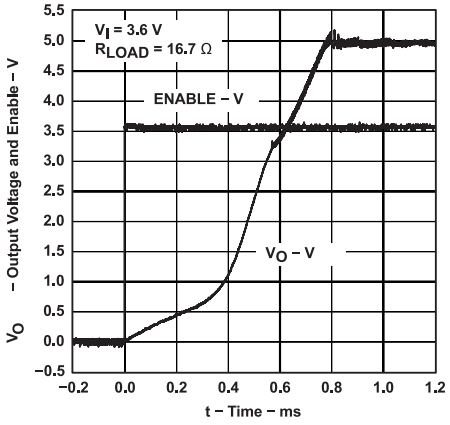


Figure 30. Output Voltage vs Time (Start-Up Timing)

10.2.2 TPS6013x Operated With Ultra-Low Quiescent Current

Because the output of the TPS6013x is isolated from the input when the devices are disabled, and because the internal resistive divider is disconnected in shutdown, an ultra-low quiescent current mode can be implemented. In this mode, the output voltage is sustained because the converter is periodically enabled to refresh the output capacitor. The necessary external control signal that is applied to the ENABLE-pin is generated from a microcontroller. For a necessary supply current for the system of 1 mA and a minimum supply voltage of 4.5 V with a 33-µF output capacitor, the refresh has to be done after 9 ms. Longer refresh periods can be achieved with a larger output capacitor.

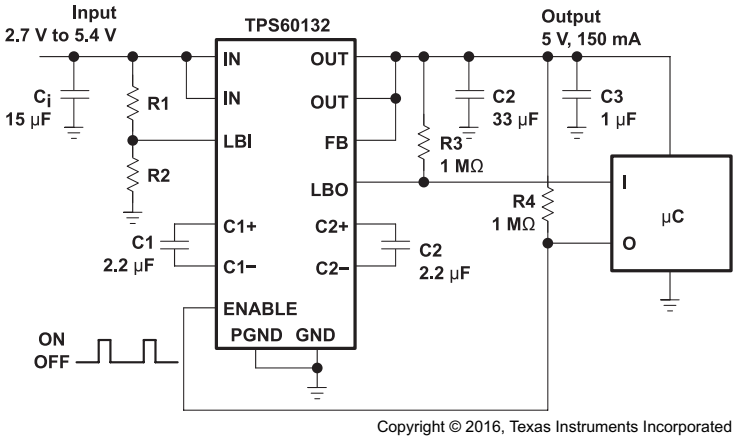


Figure 31. TPS60132 in Ultra-Low Quiescent Current Mode

10.2.2.1 Design Requirements

The device operates over an input voltage range from 2.7 V to 5.4 V.

10.2.3 Regulated Discharge of the Output Capacitors After Disabling of the TPS6013x

During shutdown of the charge pump TPS6013x the output is isolated from the input. Therefore, the discharging of the output capacitor depends on the load and on the leakage current of the capacitor. In certain applications it is necessary to completely remove the supply voltage from the load in shutdown mode. That means the output capacitor of the charge pump has to be actively discharged when the charge pump is disabled. Figure 5 shows one solution to this problem.

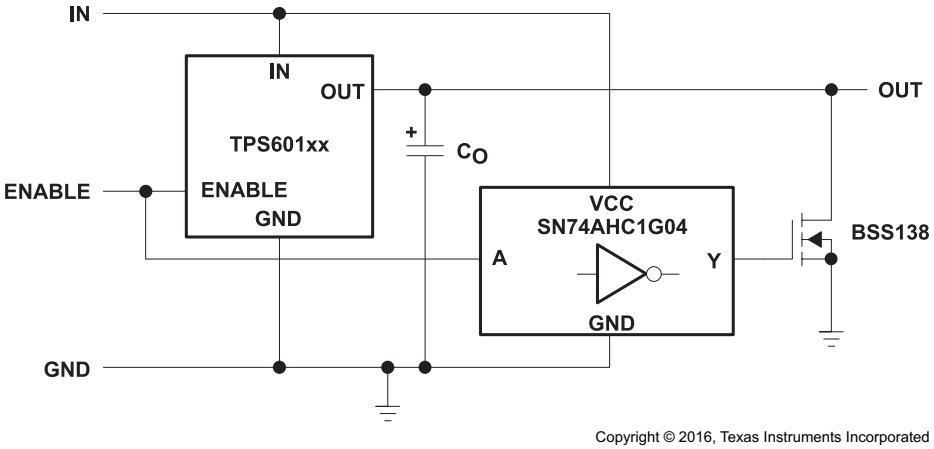


Figure 32. Block Diagram of the Regulated Discharge of the Output Capacitor

10.2.3.1 Design Requirements

The device operates over an input voltage range from 2.7 V to 5.4 V. TI's SN74AHC1G04 and BSS138 is required.

11 Power Supply Recommendations

The TPS6013x device has no special requirements for its input power supply. The output current of the input power supply must be rated according to the supply voltage, output voltage, and output current of the TPS6013x.

12 Layout

12.1 Layout Guidelines

Careful board layout is necessary due to the high transient currents and switching frequency of the converter. All capacitors must be soldered in close proximity to the IC. Connect ground and power ground pins through a short, low-impedance trace. A PCB layout proposal for a two-layer board is given in Figure 33. The bottom layer of the board carries only ground potential for best performance. The layout also provides improved thermal performance as the exposed lead frame is soldered to the PCB.

An evaluation module for the TPS60130 is available and can be ordered under product code TPS60130EVM-143. The EVM uses the layout shown in Figure 33 and components in Table 7.

The best performance of the converter is achieved with the additional bypass capacitors C5 and C6 at input and output. Capacitor C7 must be included if the large line transients are expected. The capacitors are not required. They can be omitted in most applications.

12.2 Layout Example

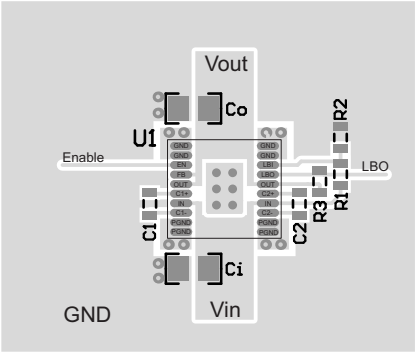


Figure 33. Recommended PCB Layout for TPS6013x

Table 7. Component Identification

COMPONENT	DESCRIPTION
IC1	TPS6013x
C1, C2	Flying capacitors
C3, C6	Input capacitors
C4, C5	Onput capacitors
C7	Stabilization capacitor for LBI
R1, R2	Resistive divider for LBI
R3	Pullup resistor for LBO

12.3 Power Dissipation

The power dissipated in the TPS6013x depends on output current and the mode of operation (1.5× or doubler voltage conversion mode). It is described by Equation 5.

$$P_{DISS} = \left(\frac{1}{\eta} - 1\right) V_O \times I_O \quad (5)$$

Power Dissipation (continued)

P_{DISS} must be less than that allowed by the package rating. See *Absolute Maximum Ratings* for 20-pin PWP package power-dissipation limits and deratings.

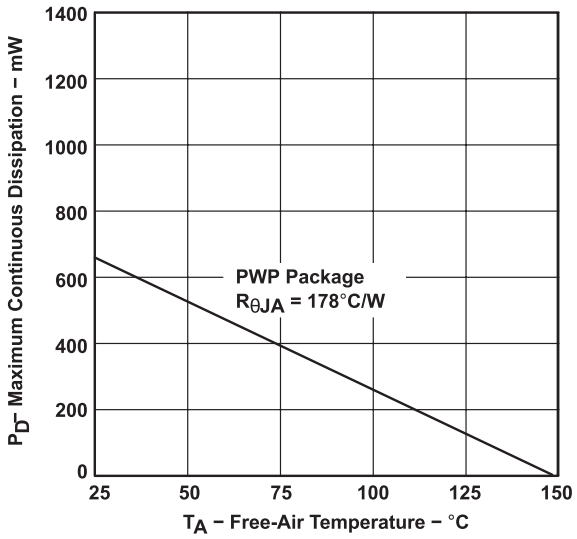


Figure 34. Dissipation Derating Curves vs Free-Air Temperature

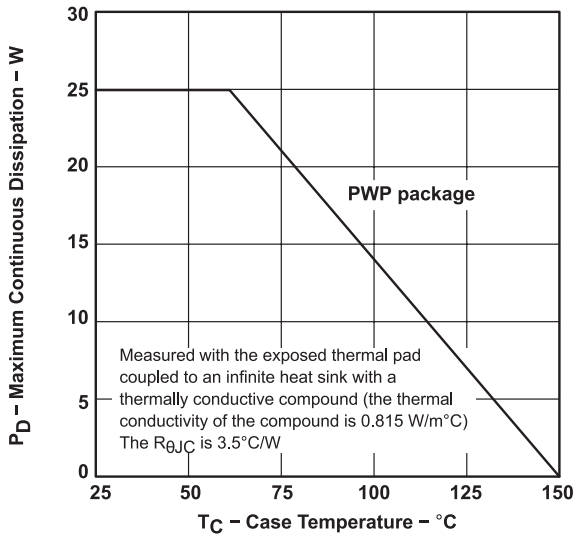


Figure 35. Maximum Continuous Dissipation vs Case Temperature

13 Device and Documentation Support

13.1 Documentation Support

13.1.1 Related Documentation

For related documentation see the following:

- *PowerPAD™ Application Report* (SLMA002)
- *TPS6010x/TPS6011x Charge Pump Application Report* (SLVA070)
- *Powering the TMS320C5420 Using the TPS60100, TPS76918, and the TPS3305-18* (SLVA082)
- *Evaluation Modules (EVMs) for TPS6012x and TPS6013x* (SLVU022)

13.2 Related Links

The table below lists quick access links. Categories include technical documents, support and community resources, tools and software, and quick access to sample or buy.

Table 8. Related Links

PARTS	PRODUCT FOLDER	SAMPLE & BUY	TECHNICAL DOCUMENTS	TOOLS & SOFTWARE	SUPPORT & COMMUNITY
TPS60130	Click here	Click here	Click here	Click here	Click here
TPS60131	Click here	Click here	Click here	Click here	Click here
TPS60132	Click here	Click here	Click here	Click here	Click here
TPS60133	Click here	Click here	Click here	Click here	Click here

13.3 Receiving Notification of Documentation Updates

To receive notification of documentation updates, navigate to the device product folder on ti.com. In the upper right corner, click on *Alert me* to register and receive a weekly digest of any product information that has changed. For change details, review the revision history included in any revised document.

13.4 Community Resources

The following links connect to TI community resources. Linked contents are provided "AS IS" by the respective contributors. They do not constitute TI specifications and do not necessarily reflect TI's views; see TI's Terms of Use.

TI E2E™ Online Community ***TI's Engineer-to-Engineer (E2E) Community.*** Created to foster collaboration among engineers. At e2e.ti.com, you can ask questions, share knowledge, explore ideas and help solve problems with fellow engineers.

Design Support ***TI's Design Support*** Quickly find helpful E2E forums along with design support tools and contact information for technical support.

13.5 Trademarks

PowerPAD, E2E are trademarks of Texas Instruments.
All other trademarks are the property of their respective owners.

13.6 Electrostatic Discharge Caution

These devices have limited built-in ESD protection. The leads should be shorted together or the device placed in conductive foam during storage or handling to prevent electrostatic damage to the MOS gates.

13.7 Glossary

SLYZ022 — *TI Glossary*.

This glossary lists and explains terms, acronyms, and definitions.

14 Mechanical, Packaging, and Orderable Information

The following pages include mechanical, packaging, and orderable information. This information is the most current data available for the designated devices. This data is subject to change without notice and revision of this document. For browser-based versions of this data sheet, refer to the left-hand navigation.

PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead finish/ Ball material (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
TPS60130PWP	ACTIVE	HTSSOP	PWP	20	70	RoHS & Green	NIPDAU	Level-2-260C-1 YEAR	-40 to 85	TPS60130	Samples
TPS60130PWPR	ACTIVE	HTSSOP	PWP	20	2000	RoHS & Green	NIPDAU	Level-2-260C-1 YEAR	-40 to 85	TPS60130	Samples
TPS60131PWP	ACTIVE	HTSSOP	PWP	20	70	RoHS & Green	NIPDAU	Level-2-260C-1 YEAR	-40 to 85	TPS60131	Samples
TPS60131PWPG4	ACTIVE	HTSSOP	PWP	20	70	RoHS & Green	NIPDAU	Level-2-260C-1 YEAR	-40 to 85	TPS60131	Samples
TPS60131PWPR	ACTIVE	HTSSOP	PWP	20	2000	RoHS & Green	NIPDAU	Level-2-260C-1 YEAR	-40 to 85	TPS60131	Samples
TPS60132PWP	ACTIVE	HTSSOP	PWP	20	70	RoHS & Green	NIPDAU	Level-2-260C-1 YEAR	-40 to 85	TPS60132	Samples
TPS60133PWP	ACTIVE	HTSSOP	PWP	20	70	RoHS & Green	NIPDAU	Level-2-260C-1 YEAR	-40 to 85	TPS60133	Samples
TPS60133PWPR	ACTIVE	HTSSOP	PWP	20	2000	RoHS & Green	NIPDAU	Level-2-260C-1 YEAR	-40 to 85	TPS60133	Samples

(1) The marketing status values are defined as follows:
ACTIVE: Product device recommended for new designs.
LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
PREVIEW: Device has been announced but is not in production. Samples may or may not be available.
OBSOLETE: TI has discontinued the production of the device.

(2) **RoHS:** TI defines "RoHS" to mean semiconductor products that are compliant with the current EU RoHS requirements for all 10 RoHS substances, including the requirement that RoHS substance do not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, "RoHS" products are suitable for use in specified lead-free processes. TI may reference these types of products as "Pb-Free".
RoHS Exempt: TI defines "RoHS Exempt" to mean products that contain lead but are compliant with EU RoHS pursuant to a specific EU RoHS exemption.
Green: TI defines "Green" to mean the content of Chlorine (Cl) and Bromine (Br) based flame retardants meet JS709B low halogen requirements of <=1000ppm threshold. Antimony trioxide based flame retardants must also meet the <=1000ppm threshold requirement.

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

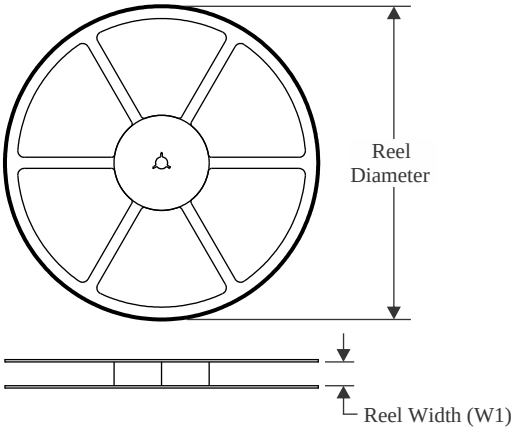
(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

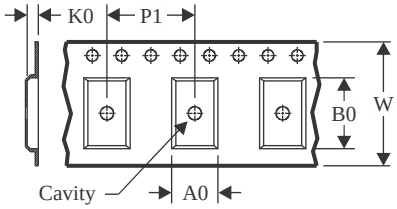
(6) Lead finish/Ball material - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

TAPE AND REEL INFORMATION

REEL DIMENSIONS

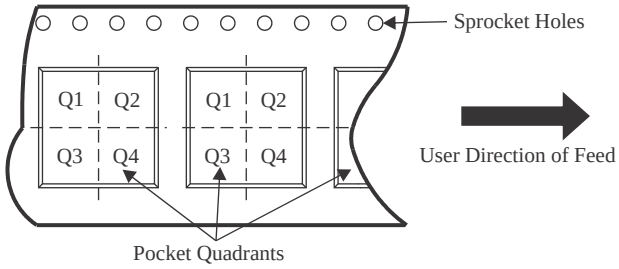


TAPE DIMENSIONS



A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

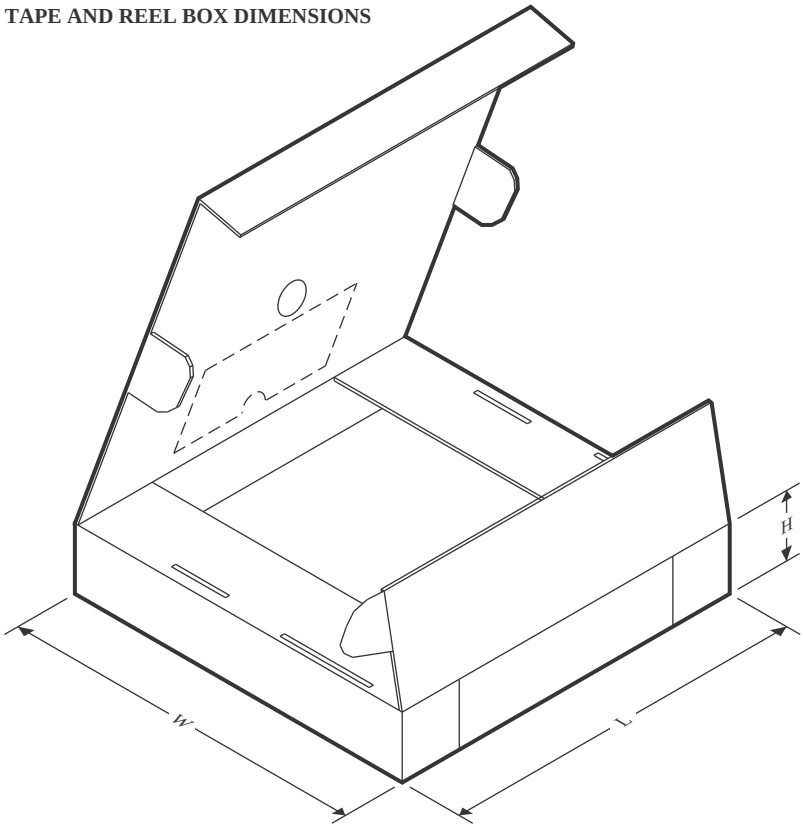
QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
TPS60130PWPR	HTSSOP	PWP	20	2000	330.0	16.4	6.95	7.1	1.6	8.0	16.0	Q1
TPS60131PWPR	HTSSOP	PWP	20	2000	330.0	16.4	6.95	7.1	1.6	8.0	16.0	Q1
TPS60133PWPR	HTSSOP	PWP	20	2000	330.0	16.4	6.95	7.1	1.6	8.0	16.0	Q1

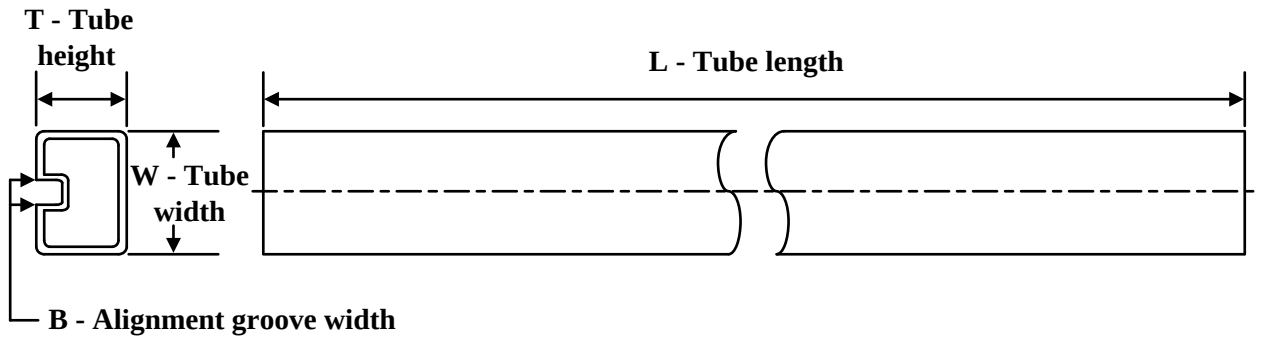
TAPE AND REEL BOX DIMENSIONS



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
TPS60130PWPR	HTSSOP	PWP	20	2000	350.0	350.0	43.0
TPS60131PWPR	HTSSOP	PWP	20	2000	350.0	350.0	43.0
TPS60133PWPR	HTSSOP	PWP	20	2000	350.0	350.0	43.0

TUBE



*All dimensions are nominal

Device	Package Name	Package Type	Pins	SPQ	L (mm)	W (mm)	T (µm)	B (mm)
TPS60130PWP	PWP	HTSSOP	20	70	530	10.2	3600	3.5
TPS60131PWP	PWP	HTSSOP	20	70	530	10.2	3600	3.5
TPS60131PWPG4	PWP	HTSSOP	20	70	530	10.2	3600	3.5
TPS60132PWP	PWP	HTSSOP	20	70	530	10.2	3600	3.5
TPS60133PWP	PWP	HTSSOP	20	70	530	10.2	3600	3.5

GENERIC PACKAGE VIEW

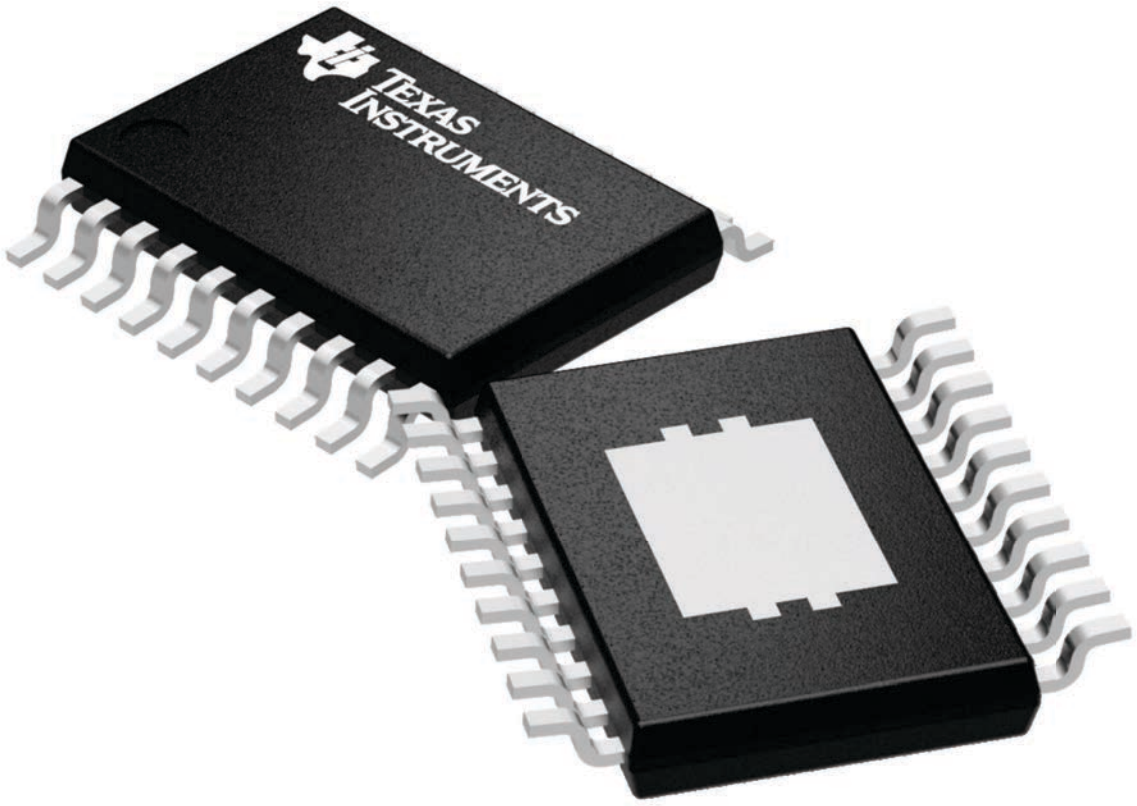
PWP 20

HTSSOP - 1.2 mm max height

6.5 x 4.4, 0.65 mm pitch

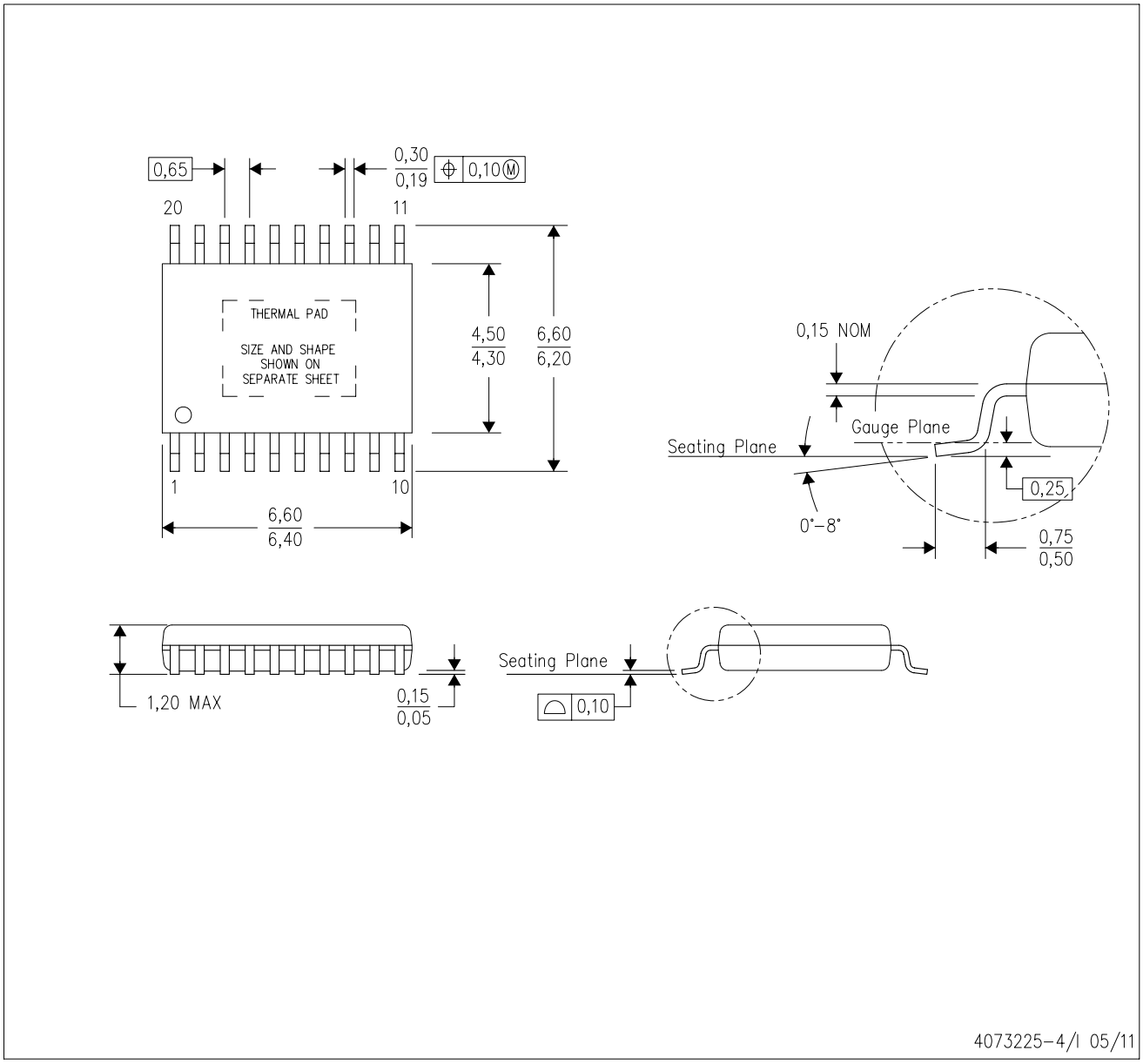
SMALL OUTLINE PACKAGE

This image is a representation of the package family, actual package may vary.
Refer to the product data sheet for package details.



4224669/A

PWP (R–PDSO–G20) PowerPAD™ PLASTIC SMALL OUTLINE



NOTES:
A. All linear dimensions are in millimeters.
B. This drawing is subject to change without notice.
C. Body dimensions do not include mold flash or protrusions. Mold flash and protrusion shall not exceed 0.15 per side.
D. This package is designed to be soldered to a thermal pad on the board. Refer to Technical Brief, PowerPad Thermally Enhanced Package, Texas Instruments Literature No. SLMA002 for information regarding recommended board layout. This document is available at www.ti.com <http://www.ti.com>.
E. See the additional figure in the Product Data Sheet for details regarding the exposed thermal pad features and dimensions.
E. Falls within JEDEC MO–153

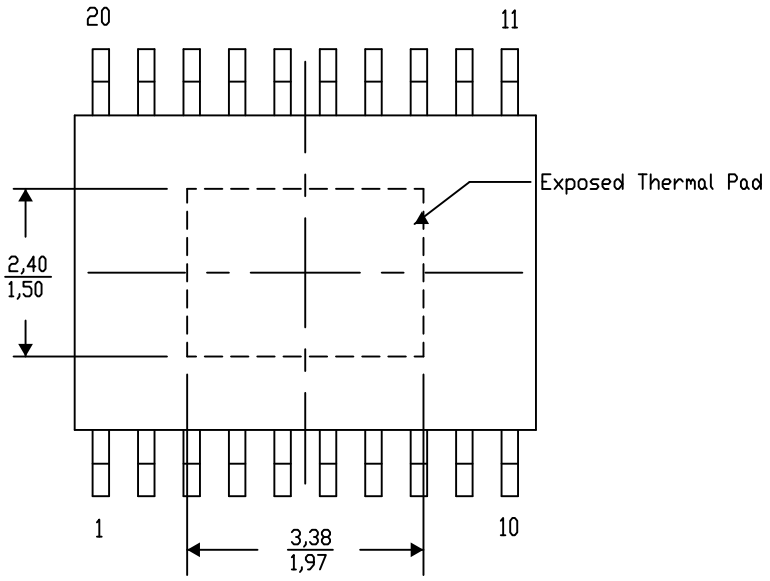
PWP (R–PDSO–G20) PowerPAD™ SMALL PLASTIC OUTLINE

THERMAL INFORMATION

This PowerPAD™ package incorporates an exposed thermal pad that is designed to be attached to a printed circuit board (PCB). The thermal pad must be soldered directly to the PCB. After soldering, the PCB can be used as a heatsink. In addition, through the use of thermal vias, the thermal pad can be attached directly to the appropriate copper plane shown in the electrical schematic for the device, or alternatively, can be attached to a special heatsink structure designed into the PCB. This design optimizes the heat transfer from the integrated circuit (IC).

For additional information on the PowerPAD package and how to take advantage of its heat dissipating abilities, refer to Technical Brief, PowerPAD Thermally Enhanced Package, Texas Instruments Literature No. SLMA002 and Application Brief, PowerPAD Made Easy, Texas Instruments Literature No. SLMA004. Both documents are available at www.ti.com.

The exposed thermal pad dimensions for this package are shown in the following illustration.



Top View

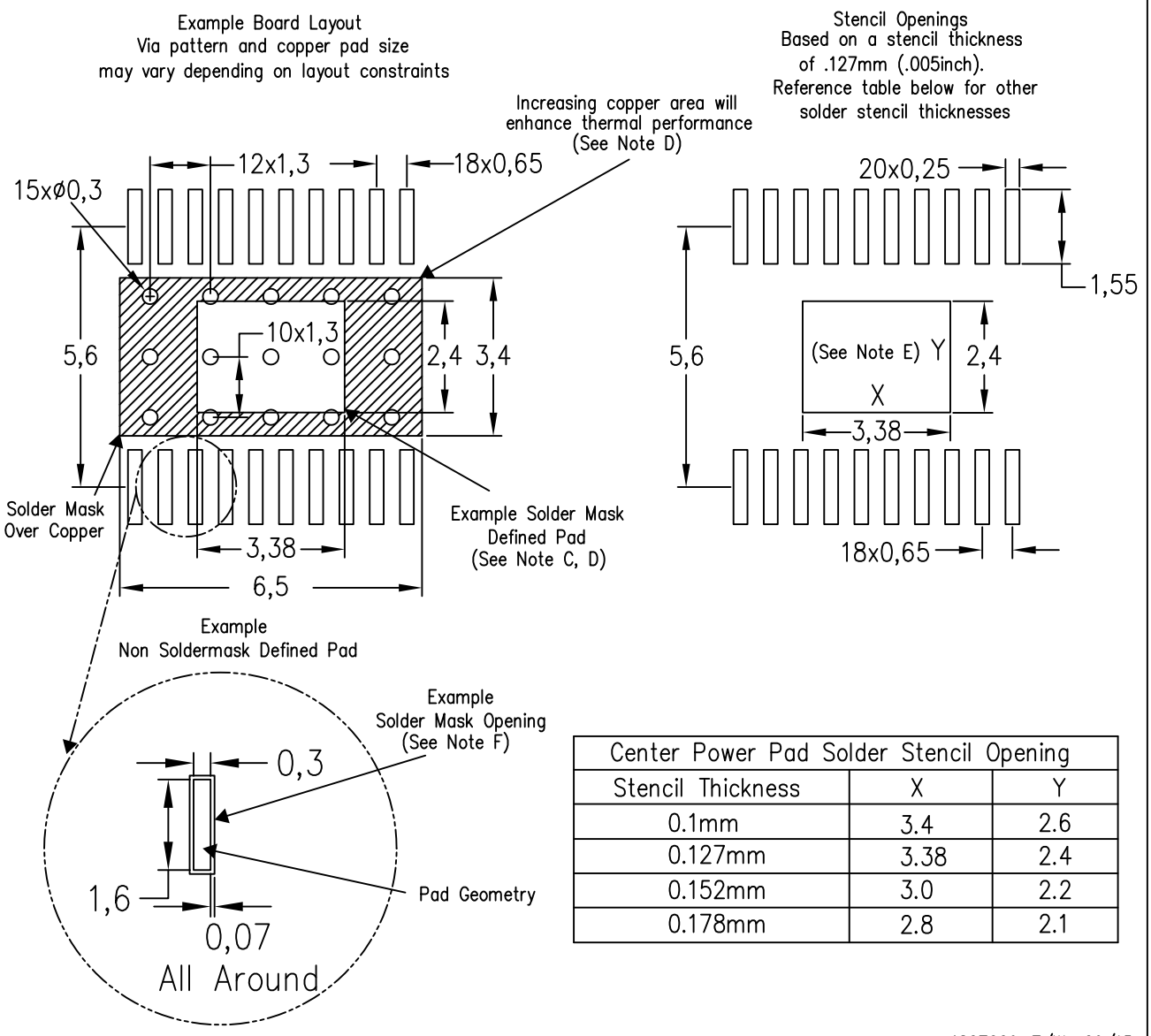
Exposed Thermal Pad Dimensions

4206332–19/AO 01/16

NOTE: A. All linear dimensions are in millimeters

PowerPAD is a trademark of Texas Instruments

PWP (R–PDSO–G20) PowerPAD™ PLASTIC SMALL OUTLINE



Center Power Pad Solder Stencil Opening		
Stencil Thickness	X	Y
0.1mm	3.4	2.6
0.127mm	3.38	2.4
0.152mm	3.0	2.2
0.178mm	2.8	2.1

4207609–7/W 09/15

NOTES:
A. All linear dimensions are in millimeters.
B. This drawing is subject to change without notice.
C. Customers should place a note on the circuit board fabrication drawing not to alter the center solder mask defined pad.
D. This package is designed to be soldered to a thermal pad on the board. Refer to Technical Brief, PowerPad Thermally Enhanced Package, Texas Instruments Literature No. SLMA002, SLMA004, and also the Product Data Sheets for specific thermal information, via requirements, and recommended board layout. These documents are available at www.ti.com <http://www.ti.com>. Publication IPC–7351 is recommended for alternate designs.
E. Laser cutting apertures with trapezoidal walls and also rounding corners will offer better paste release. Customers should contact their board assembly site for stencil design recommendations. Example stencil design based on a 50% volumetric metal load solder paste. Refer to IPC–7525 for other stencil recommendations.
F. Customers should contact their board fabrication site for solder mask tolerances between and around signal pads.

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