

## TPS7510x Low Dropout, Two-Bank LED Driver With PWM Brightness Control

### 1 Features

- Regulated Output Current with 2% LED-to-LED Matching
- Drives Up to Four LEDs at 25 mA Each in a Common Cathode Topology
- 28-mV Typical Dropout Voltage Extends Usable Supply Range in Li-Ion Battery Applications
- Brightness Control Using PWM Signals
- Two 2-LED Banks With Independent Enable and PWM Brightness Control per Bank
- No Internal Switching Signals—Eliminates EMI
- Default LED Current Eliminates External Components
  - Default Values from 3 mA to 10 mA (in 1-mA Increments) Available Using Innovative Factory EEPROM Programming
  - Optional External Resistor can be Used for High-Accuracy, User-Programmable Current
- Over current and Over temperature Protection
- Available in Wafer Chip-Scale Package or 2.50-mm × 2.50-mm WSON-10

### 2 Applications

- Keypad and Display Backlighting
- White and Color LEDs
- Cellular Handsets
- PDAs and Smartphones

### 3 Description

The TPS7510x linear low dropout (LDO) matching LED current source is optimized for low-power keypad and navigation pad LED backlighting applications. The device provides a constant current to up to four unmatched LEDs organized in two banks of two LEDs each in a common-cathode topology. Without an external resistor, the current source defaults to a factory-programmable, preset current level with  $\pm 0.5\%$  accuracy (typical). An optional external resistor can be used to set initial brightness to user-programmable values with higher accuracy. Brightness can be varied from off to full brightness by inputting a pulse width modulation (PWM) signal on each enable pin (ENx, where x indicates LED bank A or B). Each bank has independent enable and brightness control, but current matching is done to all four channels concurrently. The input supply range is ideally suited for single-cell Li-Ion battery supplies and the TPS7510x can provide up to 25 mA per LED.

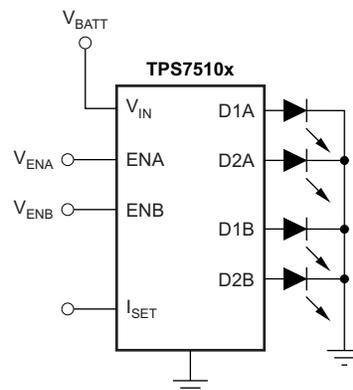
No internal switching signals are used, eliminating troublesome electromagnetic interference (EMI). The TPS7510x is offered in an ultra-small, 9-ball, 0.4-mm ball-pitch wafer chip-scale package (WCSP) and a 2.50-mm × 2.50-mm, 10-pin WSON package, yielding a very compact total solution size ideal for mobile handsets and portable backlighting applications. The device is fully specified over  $T_J = -40^\circ\text{C}$  to  $+85^\circ\text{C}$ .

#### Device Information<sup>(1)</sup>

PART NUMBER	PACKAGE	BODY SIZE (NOM)
TPS7510x	WSON (10)	2.50 mm × 2.50 mm
	DSBGA (9)	1.208 mm × 1.208 mm

(1) For all available packages, see the orderable addendum at the end of the data sheet.

#### Typical Application Diagram



## Table of Contents

<b>1 Features</b> .....	<b>1</b>	<b>8 Application and Implementation</b> .....	<b>10</b>
<b>2 Applications</b> .....	<b>1</b>	8.1 Application Information.....	10
<b>3 Description</b> .....	<b>1</b>	8.2 Typical Application .....	12
<b>4 Revision History</b> .....	<b>2</b>	<b>9 Power Supply Recommendations</b> .....	<b>14</b>
<b>5 Pin Configuration and Functions</b> .....	<b>3</b>	<b>10 Layout</b> .....	<b>14</b>
<b>6 Specifications</b> .....	<b>4</b>	10.1 Layout Guidelines .....	14
6.1 Absolute Maximum Ratings .....	4	10.2 Layout Example .....	14
6.2 ESD Ratings.....	4	<b>11 Device and Documentation Support</b> .....	<b>15</b>
6.3 Recommended Operating Conditions.....	4	11.1 Device Support.....	15
6.4 Thermal Information .....	4	11.2 Documentation Support .....	15
6.5 Electrical Characteristics.....	5	11.3 Related Links .....	15
6.6 Typical Characteristics .....	6	11.4 Receiving Notification of Documentation Updates	15
<b>7 Detailed Description</b> .....	<b>8</b>	11.5 Community Resources.....	15
7.1 Overview .....	8	11.6 Trademarks .....	16
7.2 Functional Block Diagram .....	8	11.7 Electrostatic Discharge Caution.....	16
7.3 Feature Description.....	9	11.8 Glossary .....	16
7.4 Device Functional Modes.....	9	<b>12 Mechanical, Packaging, and Orderable Information</b> .....	<b>16</b>

## 4 Revision History

NOTE: Page numbers for previous revisions may differ from page numbers in the current version.

### Changes from Revision I (November 2013) to Revision J

Page

• Added <i>Device Information</i> table, <i>Typical Application Diagram</i> title to front-page diagram, <i>ESD Ratings</i> table, <i>Thermal Information</i> table, <i>Feature Description</i> section, <i>Device Functional Modes</i> section, <i>Application and Implementation</i> section, <i>Power Supply Recommendations</i> section, <i>Layout</i> section, <i>Device and Documentation Support</i> section, and <i>Mechanical, Packaging, and Orderable Information</i> section .....	1
• Changed SON to WSON throughout document .....	1
• Deleted pin out drawings from <i>Typical Application Diagram</i> figure.....	1
• Changed I/O status to I from O in D1B row of <i>Pin Functions</i> table .....	3
• Deleted <i>Dissipation Ratings</i> table.....	4

### Changes from Revision H (January 2010) to Revision I

Page

• Changed test conditions for ground current parameter in the Electrical Characteristics .....	5
• Deleted Figure 14; duplicate mechanical image. ....	12

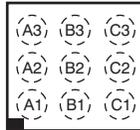
### Changes from Revision G (March 2009) to Revision H

Page

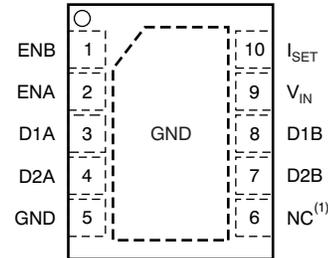
• Revised ground current parameter, Electrical Characteristics; changed symbol from $I_Q$ to $I_{GND}$ ; added specifications for YFF and DSK packages.....	5
• Added YFF and DSK package specifications for current matching parameter, Electrical Characteristics .....	5
• Changed diode current accuracy parameter, Electrical Characteristics, to reflect YFF and DSK package specifications....	5
• Deleted operating junction temperature range specification from Electrical Characteristics table to eliminate redundancy .	5

## 5 Pin Configuration and Functions

**YFF Package  
9-Pin DSBGA  
Top View**



**DSK Package  
10-Pin WSON  
Top View**



NOTE (1): Not connected

### Pin Functions

PIN			I/O	DESCRIPTION
NAME	WCSP	WSON		
ENA	A3	2	I	Enable pin, Bank A. Driving this pin high turns on the current source to Bank A outputs. Driving this pin low turns off the current source to Bank A outputs. An applied PWM signal reduces the LED current (between 0 mA and the maximum current set by $I_{SET}$ ) as a function of the duty cycle of the PWM signal. ENA and ENB can be tied together. ENA can be left OPEN or connected to GND if not used. See the <a href="#">Application and Implementation</a> section for more details.
D1A	B3	3	O	Diode source current output, Bank A. Connect to LED anode.
D2A	C3	4	O	Diode source current output, Bank A. Connect to LED anode.
ENB	A2	1	I	Enable pin, Bank B. Driving this pin high turns on the current source to Bank B outputs. Driving this pin low turns off the current source to Bank B outputs. An applied PWM signal reduces the LED current (between 0 mA and the maximum current set by $I_{SET}$ ) as a function of the duty cycle of the PWM signal. ENA and ENB can be tied together. ENB can be left OPEN or connected to GND if not used. See the <a href="#">Application and Implementation</a> section for more details.
$V_{IN}$	B2	9	I	Supply input
GND	C2	5, Pad	—	Ground
$I_{SET}$	A1	10	I	An optional resistor can be connected between this pin and GND to set the maximum current through the LEDs. If no resistor is connected, $I_{SET}$ defaults to the internally programmed value.
D1B	B1	8	O	Diode source current output, Bank B. Connect to LED anode.
D2B	C1	7	O	Diode source current output, Bank B. Connect to LED anode.
NC	—	6	—	Not internally connected

## 6 Specifications

### 6.1 Absolute Maximum Ratings

over operating free-air temperature range (unless otherwise noted)

	MIN	MAX	UNIT
$V_{IN}$ range	-0.3	7	V
$V_{ISET}$ , $V_{ENA}$ , $V_{ENB}$ , $V_{DX}$ range	-0.3	$V_{IN}$	V
$I_{DX}$ for D1A, D2A, D1B, D2B	35		mA
D1A, D2A, D1B, D2B short-circuit duration	Indefinite		
Continuous total power dissipation	Internally limited		
Junction temperature, $T_J$	-55	150	°C
Storage temperature, $T_{stg}$	-55	150	°C

### 6.2 ESD Ratings

		VALUE	UNIT
$V_{(ESD)}$ Electrostatic discharge	Human-body model (HBM), per ANSI/ESDA/JEDEC JS-001 <sup>(1)</sup>	±2000	V
	Charged-device model (CDM), per JEDEC specification JESD22-C101 <sup>(2)</sup>	±500	

(1) JEDEC document JEP155 states that 500-V HBM allows safe manufacturing with a standard ESD control process.

(2) JEDEC document JEP157 states that 250-V CDM allows safe manufacturing with a standard ESD control process.

### 6.3 Recommended Operating Conditions

PARAMETER		MIN	NOM	MAX	UNIT
$V_{IN}$	Input voltage	2.7		5.5	V
$I_{DX}$	Operating current per LED	3		25	mA
$t_{PWM}$	On-time for PWM signal	33			µs
$T_J$	Operating junction temperature range	-40		85	°C

### 6.4 Thermal Information

THERMAL METRIC <sup>(1)</sup>		TPS7510x		UNIT
		YFF (DSBGA)	DSK (WSON)	
		9 PINS	10 PINS	
$R_{\theta JA}$	Junction-to-ambient thermal resistance	101.6	65.3	°C/W
$R_{\theta JC(top)}$	Junction-to-case (top) thermal resistance	1.2	54.0	°C/W
$R_{\theta JB}$	Junction-to-board thermal resistance	17.6	39.5	°C/W
$\Psi_{JT}$	Junction-to-top characterization parameter	0.6	1.6	°C/W
$\Psi_{JB}$	Junction-to-board characterization parameter	17.8	39.7	°C/W
$R_{\theta JC(bot)}$	Junction-to-case (bottom) thermal resistance	N/A	23.6	°C/W

(1) For more information about traditional and new thermal metrics, see the [Semiconductor and IC Package Thermal Metrics](#) application report.

## 6.5 Electrical Characteristics

over operating junction temperature range ( $T_J = -40^\circ\text{C}$  to  $+85^\circ\text{C}$ ),  $V_{IN} = 3.8\text{ V}$ ,  $DxA$  and  $DxB = 3.3\text{ V}$ ,  $R_{SET} = 32.4\text{ k}\Omega$ , and  $ENA$  and  $ENB = 3.8\text{ V}$  (unless otherwise noted); typical values are at  $T_A = 25^\circ\text{C}$

PARAMETER		TEST CONDITIONS		MIN	TYP	MAX	UNIT
$I_{SHDN}$	Shutdown supply current	$V_{ENA,B} = 0\text{ V}$ , $V_{DX} = 0\text{ V}$			0.03	1	$\mu\text{A}$
$I_{GND}$	Ground current	DSK package	$I_{DX} \leq 5\text{ mA}$ , $V_{IN} = 3.8\text{ V}$		170	230	$\mu\text{A}$
			$I_{DX} > 5\text{ mA}$ , $V_{IN} = 3.8\text{ V}$		250	300	
		YFF package	$I_{DX} \leq 5\text{ mA}$ , $V_{IN} = 4.5\text{ V}$		170	200	
			$I_{DX} > 5\text{ mA}$ , $V_{IN} = 4.5\text{ V}$		250	300	
$\Delta I_D$	Current matching ( $I_{DXMAX} - I_{DXMIN} / I_{DXMAX}$ ) $\times 100\%$	$T_A = 25^\circ\text{C}$		0%	2%	4%	
		$T_A = -40^\circ\text{C}$ to $+85^\circ\text{C}$	YFF package	0%		5%	
			DSK package	0%		6%	
$\Delta I_{DX}\%/\Delta V_{IN}$	Line regulation	$3.5\text{ V} \leq V_{IN} \leq 4.5\text{ V}$ , $I_{DX} = 5\text{ mA}$			2.0		$\%/V$
$\Delta I_{DX}\%/\Delta V_{DX}$	Load regulation	$1.8\text{ V} \leq V_{DX} \leq 3.5\text{ V}$ , $I_{DX} = 5\text{ mA}$			0.8		$\%/V$
$V_{DO}$	Dropout voltage of any DX current source ( $V_{DX}$ at $I_{DX} = 0.8 \times I_{DX, nom}$ )	$I_{DXnom} = 5\text{ mA}$			28	100	mV
		$I_{DXnom} = 15\text{ mA}$			70		
$V_{ISET}$	Reference voltage for current set			1.183	1.225	1.257	V
$I_{OPEN}$	Diode current accuracy <sup>(1)</sup>	$I_{SET} = \text{open}$ , $V_{DX} = V_{IN} - 0.2\text{ V}$	YFF package		0.5%	3%	
			DSK package		0.5%	4%	
$I_{SET}$	$I_{SET}$ pin current range			2.5		62.5	$\mu\text{A}$
k	$I_{SET}$ to $I_{DX}$ current ratio <sup>(1)</sup>				420		
$V_{IH}$	Enable high level input voltage			1.2			V
$V_{IL}$	Enable low level input voltage					0.4	V
$I_{INA}$	Enable pin A ( $V_{ENA}$ ) input current	$V_{ENA} = 3.8\text{ V}$			5.0	6.1	$\mu\text{A}$
		$V_{ENA} = 1.8\text{ V}$			2.2		
$I_{INB}$	Enable pin B ( $V_{ENB}$ ) input current	$V_{ENB} = 3.8\text{ V}$			4.0	4.9	$\mu\text{A}$
		$V_{ENB} = 1.8\text{ V}$			1.8		
$t_{SD}$	Shutdown delay time	Delay from $ENA$ and $ENB = \text{low}$ to reach shutdown current ( $I_{DX} = 0.1 \times I_{DX, nom}$ )		5	13	30	$\mu\text{s}$
$T_{SD}$	Thermal shutdown temperature	Shutdown, temperature increasing			165		$^\circ\text{C}$
		Reset, temperature decreasing			140		

(1) Average of all four  $I_{DX}$  outputs.

## 6.6 Typical Characteristics

over operating junction temperature range ( $T_J = -40^\circ\text{C}$  to  $+85^\circ\text{C}$ ),  $V_{IN} = 3.8\text{ V}$ ,  $DxA$  and  $DxB = 3.3\text{ V}$ ,  $R_{SET} = 32.4\text{ k}\Omega$ , and  $ENA$  and  $ENB = \text{high}$  (unless otherwise noted); typical values are at  $T_A = 25^\circ\text{C}$



Figure 1. LED Current vs Duty Cycle ( $f = 300\text{ Hz}$ )

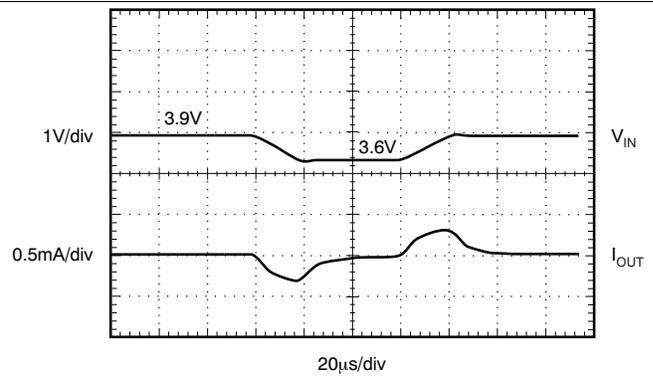


Figure 2. Line Transient (600-mV Pulse)

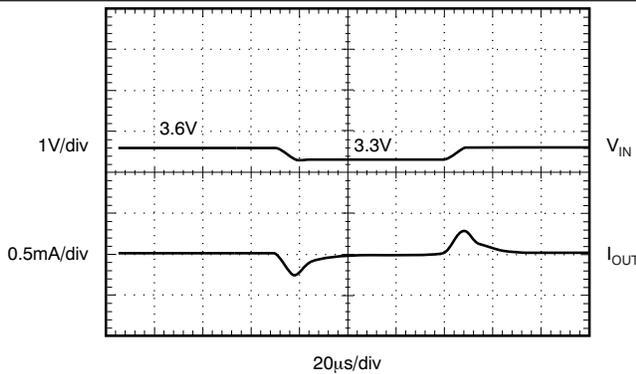


Figure 3. Line Transient (300-mV Pulse)

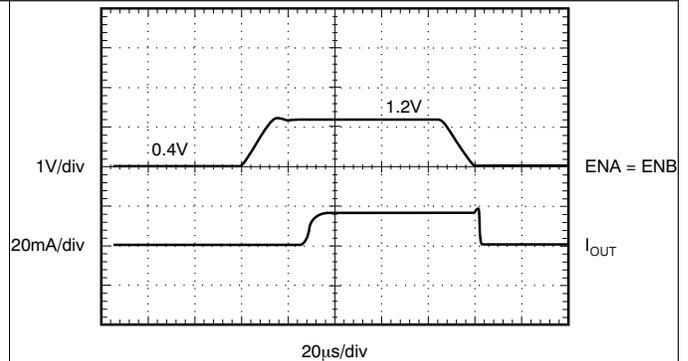


Figure 4. Dimming Response (Both Channels)

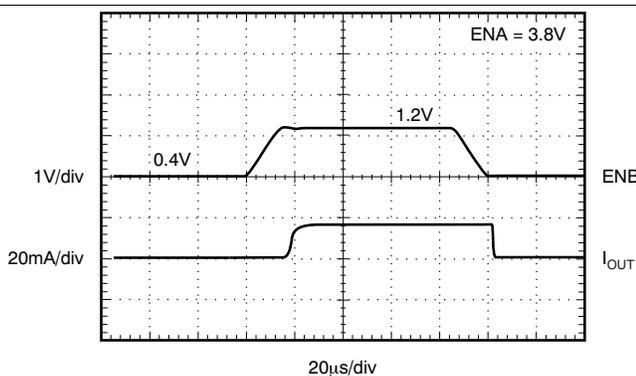


Figure 5. Dimming Response (Single Channel)

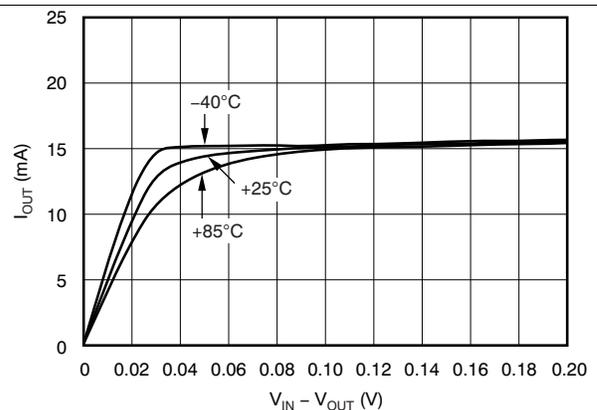
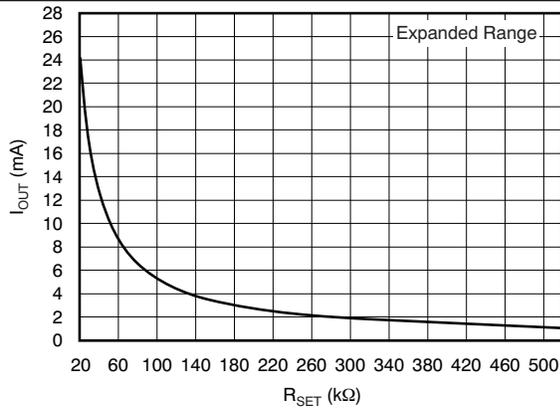


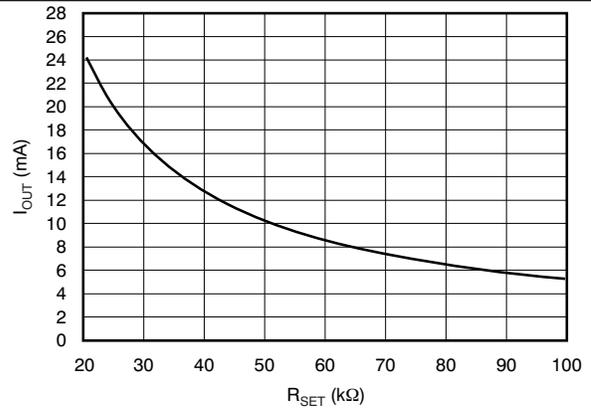
Figure 6. Output Current vs Headroom Voltage

**Typical Characteristics (continued)**

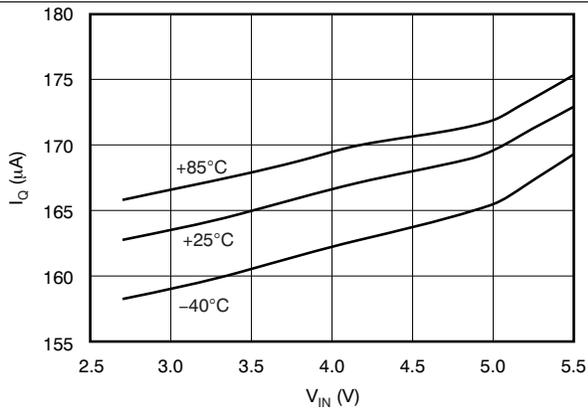
over operating junction temperature range ( $T_J = -40^{\circ}\text{C}$  to  $+85^{\circ}\text{C}$ ),  $V_{IN} = 3.8\text{ V}$ ,  $DxA$  and  $DxB = 3.3\text{ V}$ ,  $R_{SET} = 32.4\text{ k}\Omega$ , and  $ENA$  and  $ENB = \text{high}$  (unless otherwise noted); typical values are at  $T_A = 25^{\circ}\text{C}$



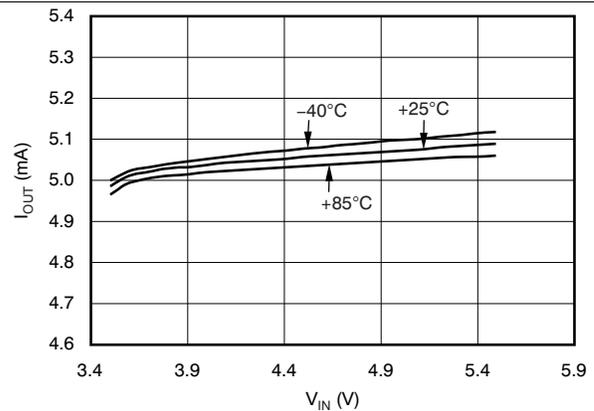
**Figure 7. Output Current vs  $R_{SET}$**



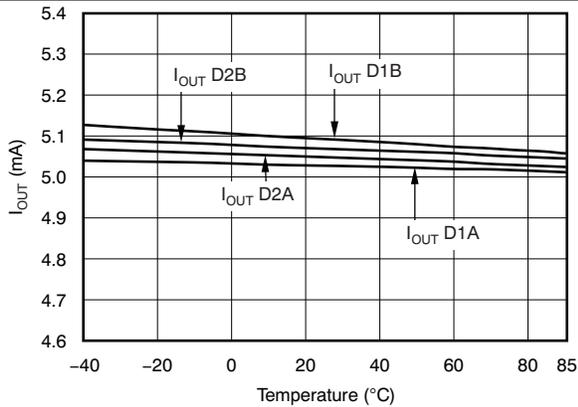
**Figure 8. Output Current vs  $R_{SET}$**



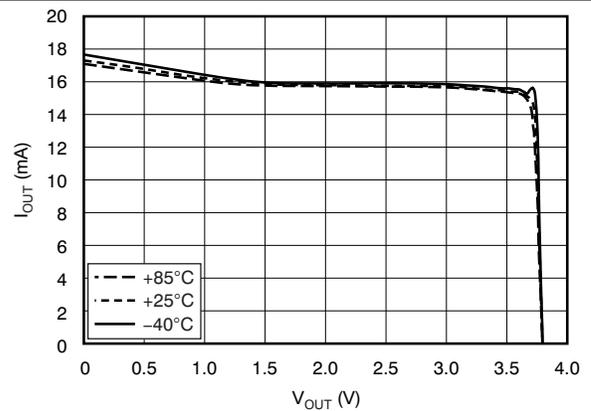
**Figure 9. Ground Current vs Input Voltage**



**Figure 10. TPS75105 Output Current vs Input Voltage  
 $R_{SET} = \text{Open}$**



**Figure 11. TPS75105 Output Current vs Temperature  
 $R_{SET} = \text{Open}$**



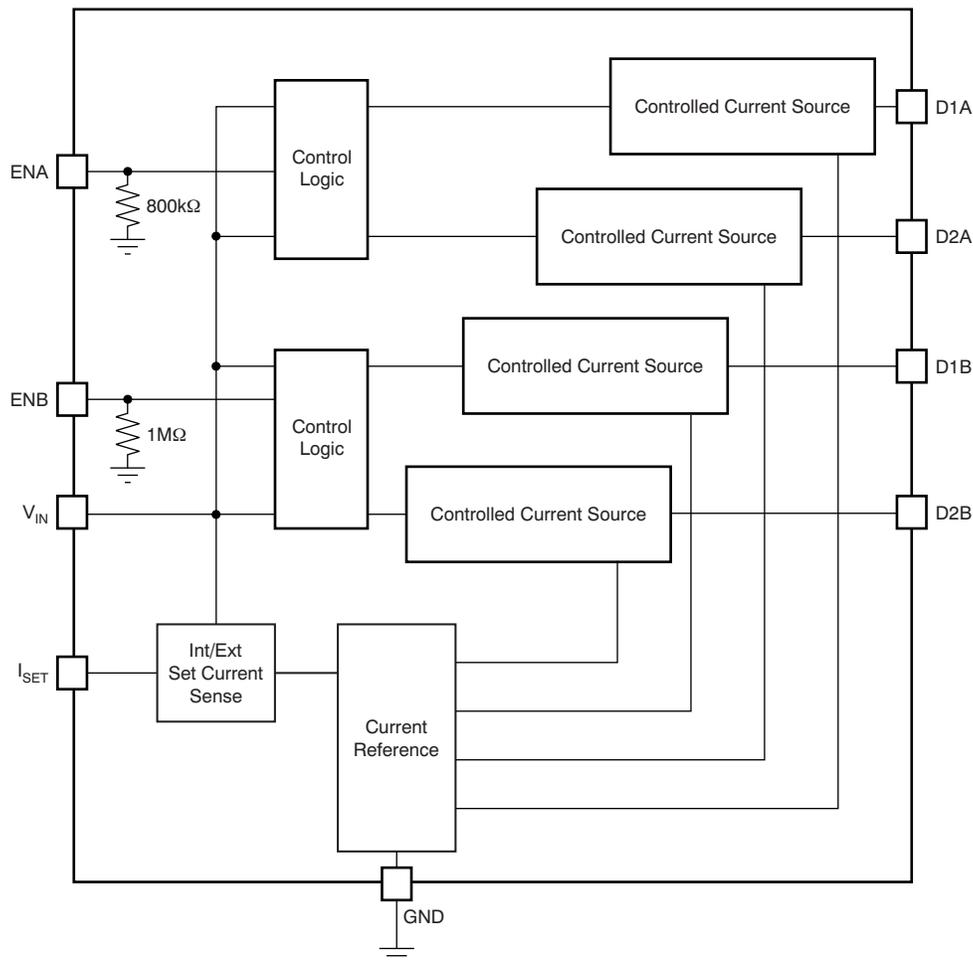
**Figure 12. Output Current vs Output Voltage**

## 7 Detailed Description

### 7.1 Overview

The TPS7510x linear low dropout (LDO) matching LED current source is optimized for low-power keypad and navigation pad LED backlighting applications. The device provides a constant current to up to four unmatched LEDs organized in two banks of two LEDs each in a common-cathode topology. Brightness can be varied from off to full brightness by inputting a pulse width modulation (PWM) signal on each enable pin (ENx, where x indicates LED bank A or B). Each bank has independent enable and brightness control, but current matching is done to all four channels concurrently. The input supply range is ideally suited for single-cell Li-Ion battery supplies and the TPS7510x can provide up to 25 mA per LED.

### 7.2 Functional Block Diagram



## 7.3 Feature Description

### 7.3.1 Load Regulation

The TPS7510x is designed to provide very tight load regulation. In the case of a fixed current source, the output load change is a change in voltage. Tight load regulation means that output voltages (LED forward voltages) with large variations can be used without impacting the fixed current being sourced by the output or the output-to-output current matching. The permissible variation on the output not only allows for large variations in white LED forward voltages, but even permits the use of different color LEDs on different outputs with minimal effect on output current.

### 7.3.2 Line Regulation

The TPS7510x is also designed to provide very tight line regulation. This architecture allows for voltage transient events to occur on the power supply (battery) without effecting the fixed output current levels or the output-to-output current matching. A prime example of such a supply transient event is the occurrence of a transmit pulse on the radio of a mobile handset. These transient pulses can cause variations of 300 mV and 600 mV on the supply to the TPS7510x. The line regulation limitation is that the lower supply voltage level of the event does not cause the input-to-output voltage difference to drop below the dropout voltage range.

## 7.4 Device Functional Modes

### 7.4.1 LED ON

Apply 1.2 V or more to ENx to turn the LED bank on.

### 7.4.2 LED OFF

Apply a voltage less than or equal to 0.4V to ENx to turn the LED bank off.

## 8 Application and Implementation

### NOTE

Information in the following applications sections is not part of the TI component specification, and TI does not warrant its accuracy or completeness. TI's customers are responsible for determining suitability of components for their purposes. Customers should validate and test their design implementation to confirm system functionality.

### 8.1 Application Information

The TPS7510x provides a constant current to up to four unmatched LEDs organized in two banks of two LEDs each in a common-cathode topology. Without an external resistor, the current source defaults to a factory-programmable, preset current level with  $\pm 0.5\%$  accuracy (typical). An optional external resistor can be used to set initial brightness to user-programmable values with higher accuracy. Brightness can be varied from off to full brightness by inputting a pulse width modulation (PWM) signal on each enable pin (ENx, where x indicates LED bank A or B). Each bank has independent enable and brightness control, but current matching is done to all four channels concurrently. The input supply range is ideally suited for single-cell Li-Ion battery supplies and the TPS7510x can provide up to 25 mA per LED. No internal switching signals are used, eliminating troublesome electromagnetic interference (EMI). The device is fully specified over  $T_J = -40^\circ\text{C}$  to  $+85^\circ\text{C}$ .

#### 8.1.1 Setting the Output Current Level

The TPS7510x is a quad matched current source. Each of the four current source output levels is set by a single reference current. An internal voltage reference of 1.225 V (nominal) in combination with a resistor sets the reference current level. This reference current is then mirrored onto each of the four outputs with a ratio of typically 420:1. The resistor required to set the LED current is calculated using [Equation 1](#):

$$R_{\text{ISET}} = \frac{K \times V_{\text{ISET}}}{I_{\text{LED}}}$$

where:

- K is the current ratio
- $V_{\text{ISET}}$  is the internal reference voltage
- $I_{\text{LED}}$  is the desired LED current

(1)

For example, to set the LED current level to 10mA, a resistor value of 51.1 k $\Omega$  is required. This value sets up a reference current of 23.9  $\mu\text{A}$  (1.22 V / 51.1 k $\Omega$ ). In turn, this reference current is mirrored to each output current source, resulting in an output current of 10 mA (23.9  $\mu\text{A}$   $\times$  420).

The TPS7510x offers two methods for setting the output current levels. The LED current is set either by connecting a resistor (calculated using [Equation 1](#)) from the  $I_{\text{SET}}$  pin to GND, or leaving  $I_{\text{SET}}$  unconnected to employ the factory-programmed  $R_{\text{SET}}$  resistance. The internal programmed resistance is implemented using high-precision processing and yields a reference current accuracy of 0.5%, nominal. Accuracy using external resistors is subject to the tolerance of the external resistor and the accuracy of the internal reference voltage.

The TPS7510x automatically detects the presence of an external resistor by monitoring the current out of the  $I_{\text{SET}}$  pin. Current levels in excess of 3  $\mu\text{A}$  signify the presence of an external resistor and the device uses the external resistor to set the reference current. If the current from  $I_{\text{SET}}$  is less than 3  $\mu\text{A}$ , the device defaults to the preset internal reference set resistor. The TPS7510x is available with eight preset current levels, from 3 mA to 10 mA (per output) in 1-mA increments. Solutions using the preset internal current level eliminate an external component, thereby increasing accuracy and reducing cost.

**Application Information (continued)**
**Table 1. Recommended (1% Tolerance) Set Resistor Values**

$R_{SET}$ (k $\Omega$ )	$I_{SET}$ ( $\mu$ A)	$I_{DX}$ (mA) <sup>(1)</sup>
511	2.4	1.0
255	4.8	2.0
169	7.2	3.0
127	9.6	4.1
102	12.0	5.0
84.5	14.5	6.1
73.2	16.7	7.0
64.9	18.9	7.9
56.2	21.8	9.2
51.1	24.0	10.1
46.4	26.4	11.1
42.2	29.0	12.2
39.2	31.3	13.1
36.5	33.6	14.1
34.0	36.0	15.1
32.4	37.8	15.9
30.1	40.7	17.1
28.7	42.7	17.9
26.7	45.9	19.3
25.5	48.0	20.2
24.3	50.4	21.2
23.2	52.8	22.2
22.1	55.4	23.3
21.5	57.0	23.9
20.5	59.8	25.1

(1)  $I_{DX} = (V_{SET} / R_{SET}) \times k$ .

**8.1.2 Limitations on LED Forward Voltages**

The TPS7510x is a linear current source implementing LDO regulator building blocks. Therefore, to maintain accurate operation, there are some limitations to the forward (output) voltages that can be used. The first limitation is the maximum LED forward voltage. The dropout voltage must be considered because LDO technology is employed. The TPS7510x is an ultra-low dropout device with typical dropouts in the range of 30 mV at 5 mA. Care must be taken in the design to ensure that the difference between the lowest possible input voltage (for example, battery cut-off) and the highest possible forward voltage yields at least 100 mV of headroom. Headroom levels less than dropout decrease the accuracy of the current source (see [Figure 6](#)).

The other limitation to consider is the minimum output voltage required to yield accurate operation. The current source employs NMOS MOSFETs, and a minimum forward LED voltage of approximately 1.5 V on the output is required to maintain highest accuracy. The TPS7510x is ideal for white LEDs and color LEDs with forward voltages greater than 1.5 V. This range includes red LEDs that have typical forward voltages of 1.7 V.

**8.1.3 Use of External Capacitors**

The TPS7510x does not require the use of any external capacitors for stable operation. Nominal stray and power-supply decoupling capacitance on the input is adequate for stable operation. Capacitors are not needed for stability and are therefore not recommended on the outputs.

### 8.1.4 Use of Unused Outputs or Tying Outputs Together

Unused outputs can be left unconnected or tied to the  $V_{IN}$  supply. Although open outputs are acceptable, tying unused outputs to the  $V_{IN}$  supply increases ESD protection. Connecting unused outputs to ground violates the minimum recommended output voltage, results in current levels that potentially exceed the set or preset LED current, and must be avoided.

Connecting outputs in parallel is an acceptable way of increasing the amount of LED current drive. This configuration is a useful trick when the higher current level is a multiple of the preset value.

### 8.1.5 Use of Enable Pins for PWM Dimming

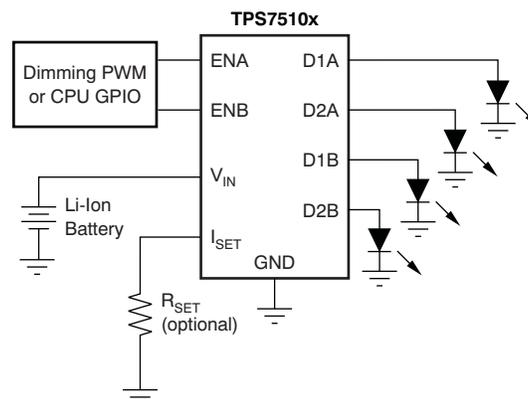
The TPS7510x divides control of the LED outputs into two banks of two current sources each. Each bank is controlled by the use of an independent, active-high enable pin (ENA and ENB). The enable pin can be used for standard ON or OFF operation of the current source, driven by standard logic levels from processor GPIO pins, for example. Drive ENx high to turn on the bank of LEDs; drive ENx low to turn off the bank of LEDs.

Another use of the enable pins is for LED dimming. LED brightness is a function of the current level being driven across the diode and the time that current is being driven through the diode. The perceived brightness of an LED can be changed by either varying the current level or, more effectively, by changing the time in which that current is present. When a PWM signal is input into the enable pin, the duty cycle (high- or on-time) determines how long the fixed current is driven across the LEDs. Reducing or increasing that duration has the effect of dimming or brightening the LED, without having to employ the more complex method of varying the current level. This technique is particularly useful for reducing LED brightness in low ambient light conditions, where LED brightness is not required, thereby decreasing current consumption. The enable pins can also be used for LED blinking, varying blink rates based on system status.

Although providing many useful applications, PWM dimming does have a minimum duty cycle required to achieve the required current level. The recommended minimum on-time of the TPS7510x is approximately 33  $\mu$ s. On-times less than 33  $\mu$ s result in reductions in the output current by not allowing enough time for the output to reach the desired current level. Also, having both enables switching together, asynchronously, or having one enable on at all times, effects the minimum recommended on-time (see [Figure 4](#) and [Figure 5](#)). If one enable is already on, the speed at which the other channel turns on is faster than if both channels are turning on together or if the other channel is off. Therefore, already having one channel enabled allows for approximately 10- $\mu$ s to 12- $\mu$ s shorter minimum on-times for the switching channel.

Unused enable pins can be left unconnected or connected to ground to minimize current consumption. Connecting unused enable pins to ground increases ESD protection. If connected to  $V_{IN}$ , a small amount of current drains through the enable input (see the [Electrical Characteristics](#) table).

## 8.2 Typical Application



**Figure 13. Typical Application Diagram**

## Typical Application (continued)

### 8.2.1 Design Requirements

Table 2 shows the design requirements.

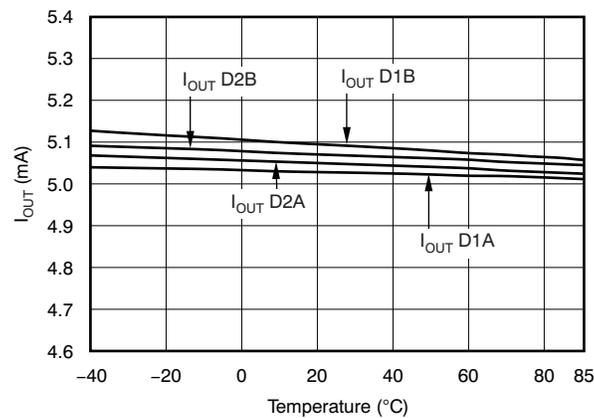
Table 2. Design Parameters

PARAMETER	DESIGN REQUIREMENT
Input voltage	3.8 V
Number of LEDs	4
LED current	5 mA (per LED)

### 8.2.2 Detailed Design Procedure

Select the TPS75105 so that no external resistor is required to set the LED current.

### 8.2.3 Application Curve



$R_{SET} = \text{open}$

Figure 14. TPS75105 Output Current vs Temperature

## 9 Power Supply Recommendations

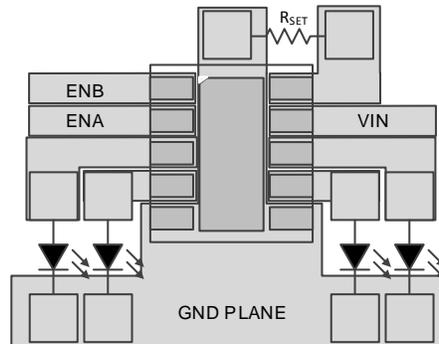
The TPS7510x is designed to operate with an input voltage between 2.7 V to 5.5 V.

## 10 Layout

### 10.1 Layout Guidelines

Figure 15 demonstrates an example layout for the WSON package.

### 10.2 Layout Example



**Figure 15. Layout Example for the WSON (DSK) Package**

## 11 Device and Documentation Support

### 11.1 Device Support

#### 11.1.1 Development Support

Two evaluation modules (EVMs) are available to assist in the initial circuit performance evaluation using the TPS7510x. The TPS75105EVM-174 and TPS75105DSKEVM-529 evaluation modules (and related user guides) can be requested at the Texas Instruments website through the product folders or purchased directly from the TI eStore.

#### 11.1.2 Device Nomenclature

PRODUCT ID	OPTIONS <sup>(1)(2)</sup>
TPS7510x <i>yyyz</i>	<p><b>X</b> is the nominal default diode output current (for example, 3 = 3 mA, 5 = 5 mA, and 0 = 10 mA).</p> <p><b>YYY</b> is the package designator.</p> <p><b>Z</b> is the reel quantity (R = 3000, T = 250).</p>

- (1) For the most current package and ordering information see the Package Option Addendum at the end of this document, or see the TI web site at [www.ti.com](http://www.ti.com).
- (2) Default set currents from 3 mA to 10 mA in 1-mA increments are available through the use of innovative factory EEPROM programming. Minimum order quantities may apply. Contact factory for details and availability.

### 11.2 Documentation Support

#### 11.2.1 Related Documentation

For related documentation see the following:

- [TPS75105EVM-174 Evaluation Module](#) (SLVU182)
- [TPS75105DSKEVM-529 Evaluation Module](#) (SLVU334)

#### 11.3 Related Links

The table below lists quick access links. Categories include technical documents, support and community resources, tools and software, and quick access to sample or buy.

**Table 3. Related Links**

PARTS	PRODUCT FOLDER	SAMPLE & BUY	TECHNICAL DOCUMENTS	TOOLS & SOFTWARE	SUPPORT & COMMUNITY
TPS75100	<a href="#">Click here</a>				
TPS75103	<a href="#">Click here</a>				
TPS75105	<a href="#">Click here</a>				

#### 11.4 Receiving Notification of Documentation Updates

To receive notification of documentation updates, navigate to the device product folder on ti.com. In the upper right corner, click on *Alert me* to register and receive a weekly digest of any product information that has changed. For change details, review the revision history included in any revised document.

#### 11.5 Community Resources

The following links connect to TI community resources. Linked contents are provided "AS IS" by the respective contributors. They do not constitute TI specifications and do not necessarily reflect TI's views; see TI's [Terms of Use](#).

**TI E2E™ Online Community** *TI's Engineer-to-Engineer (E2E) Community*. Created to foster collaboration among engineers. At e2e.ti.com, you can ask questions, share knowledge, explore ideas and help solve problems with fellow engineers.

**Design Support** *TI's Design Support* Quickly find helpful E2E forums along with design support tools and contact information for technical support.

## 11.6 Trademarks

E2E is a trademark of Texas Instruments.  
All other trademarks are the property of their respective owners.

## 11.7 Electrostatic Discharge Caution



This integrated circuit can be damaged by ESD. Texas Instruments recommends that all integrated circuits be handled with appropriate precautions. Failure to observe proper handling and installation procedures can cause damage.

ESD damage can range from subtle performance degradation to complete device failure. Precision integrated circuits may be more susceptible to damage because very small parametric changes could cause the device not to meet its published specifications.

## 11.8 Glossary

[SLYZ022](#) — *TI Glossary*.

This glossary lists and explains terms, acronyms, and definitions.

## 12 Mechanical, Packaging, and Orderable Information

The following pages include mechanical, packaging, and orderable information. This information is the most current data available for the designated devices. This data is subject to change without notice and revision of this document. For browser-based versions of this data sheet, refer to the left-hand navigation.

**PACKAGING INFORMATION**

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead finish/ Ball material (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
TPS75100DSKR	ACTIVE	SON	DSK	10	3000	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-40 to 85	SKX	<a href="#">Samples</a>
TPS75100DSKT	ACTIVE	SON	DSK	10	250	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-40 to 85	SKX	<a href="#">Samples</a>
TPS75100YFFR	ACTIVE	DSBGA	YFF	9	3000	RoHS & Green	SNAGCU	Level-1-260C-UNLIM	-40 to 85	FB	<a href="#">Samples</a>
TPS75100YFFT	ACTIVE	DSBGA	YFF	9	250	RoHS & Green	SNAGCU	Level-1-260C-UNLIM	-40 to 85	FB	<a href="#">Samples</a>
TPS75103YFFR	ACTIVE	DSBGA	YFF	9	3000	RoHS & Green	SNAGCU	Level-1-260C-UNLIM	-40 to 85	FC	<a href="#">Samples</a>
TPS75103YFFT	ACTIVE	DSBGA	YFF	9	250	RoHS & Green	SNAGCU	Level-1-260C-UNLIM	-40 to 85	FC	<a href="#">Samples</a>
TPS75105DSKR	ACTIVE	SON	DSK	10	3000	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-40 to 85	CHH	<a href="#">Samples</a>
TPS75105DSKT	ACTIVE	SON	DSK	10	250	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-40 to 85	CHH	<a href="#">Samples</a>
TPS75105YFFR	ACTIVE	DSBGA	YFF	9	3000	RoHS & Green	SNAGCU	Level-1-260C-UNLIM	-40 to 85	FE	<a href="#">Samples</a>
TPS75105YFFT	ACTIVE	DSBGA	YFF	9	250	RoHS & Green	SNAGCU	Level-1-260C-UNLIM	-40 to 85	FE	<a href="#">Samples</a>

(1) The marketing status values are defined as follows:

**ACTIVE:** Product device recommended for new designs.

**LIFEBUY:** TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.

**NRND:** Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.

**PREVIEW:** Device has been announced but is not in production. Samples may or may not be available.

**OBSOLETE:** TI has discontinued the production of the device.

(2) **RoHS:** TI defines "RoHS" to mean semiconductor products that are compliant with the current EU RoHS requirements for all 10 RoHS substances, including the requirement that RoHS substance do not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, "RoHS" products are suitable for use in specified lead-free processes. TI may reference these types of products as "Pb-Free".

**RoHS Exempt:** TI defines "RoHS Exempt" to mean products that contain lead but are compliant with EU RoHS pursuant to a specific EU RoHS exemption.

**Green:** TI defines "Green" to mean the content of Chlorine (Cl) and Bromine (Br) based flame retardants meet JS709B low halogen requirements of <=1000ppm threshold. Antimony trioxide based flame retardants must also meet the <=1000ppm threshold requirement.

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

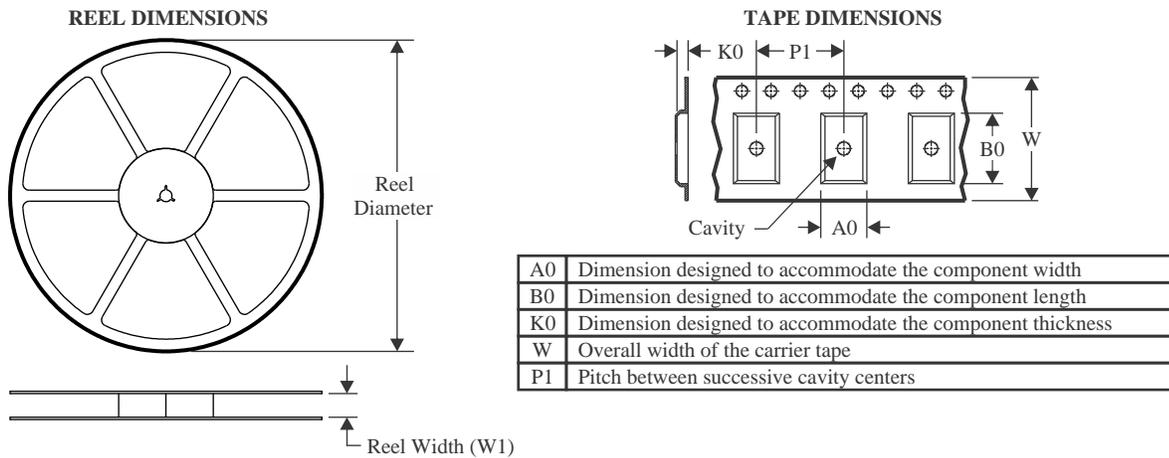
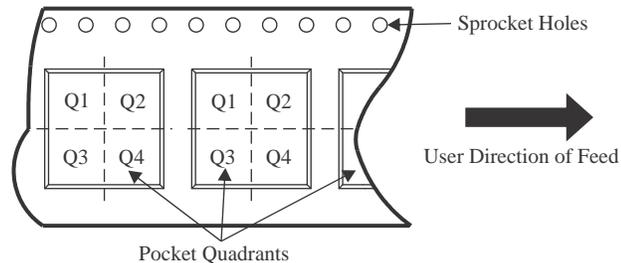
(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

<sup>(5)</sup> Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

<sup>(6)</sup> Lead finish/Ball material - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

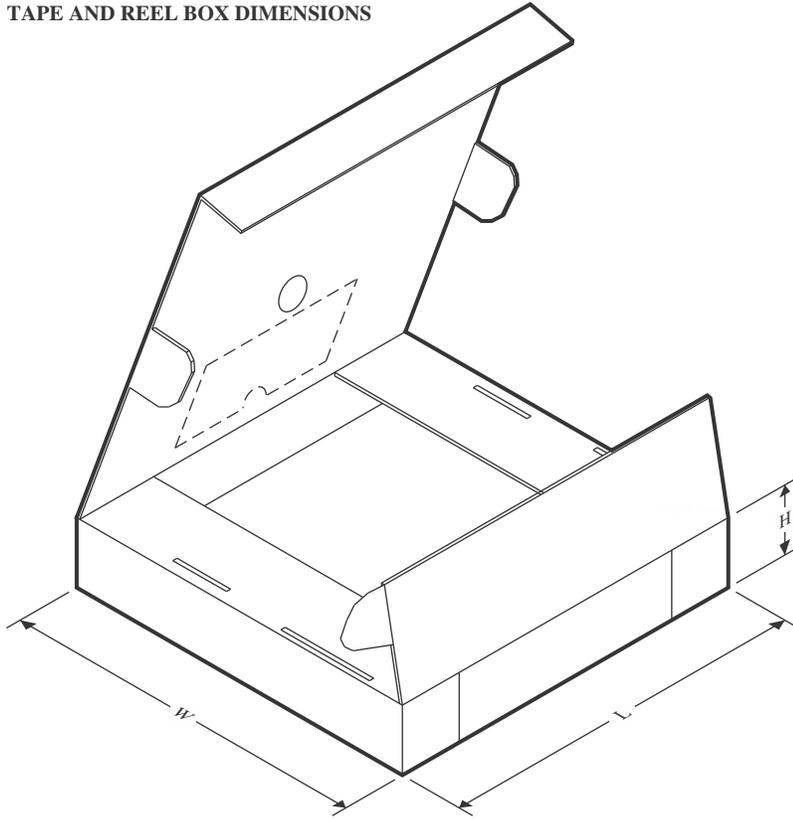
**Important Information and Disclaimer:**The information provided on this page represents TI's knowledge and belief as of the date that it is provided. TI bases its knowledge and belief on information provided by third parties, and makes no representation or warranty as to the accuracy of such information. Efforts are underway to better integrate information from third parties. TI has taken and continues to take reasonable steps to provide representative and accurate information but may not have conducted destructive testing or chemical analysis on incoming materials and chemicals. TI and TI suppliers consider certain information to be proprietary, and thus CAS numbers and other limited information may not be available for release.

In no event shall TI's liability arising out of such information exceed the total purchase price of the TI part(s) at issue in this document sold by TI to Customer on an annual basis.

**TAPE AND REEL INFORMATION**

**QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE**


\*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
TPS75100DSKR	SON	DSK	10	3000	179.0	8.4	2.73	2.73	0.8	4.0	8.0	Q2
TPS75100DSKT	SON	DSK	10	250	179.0	8.4	2.73	2.73	0.8	4.0	8.0	Q2
TPS75100YFFR	DSBGA	YFF	9	3000	180.0	8.4	1.34	1.34	0.81	4.0	8.0	Q1
TPS75100YFFT	DSBGA	YFF	9	250	180.0	8.4	1.34	1.34	0.81	4.0	8.0	Q1
TPS75103YFFR	DSBGA	YFF	9	3000	180.0	8.4	1.45	1.45	0.8	4.0	8.0	Q1
TPS75103YFFT	DSBGA	YFF	9	250	180.0	8.4	1.45	1.45	0.8	4.0	8.0	Q1
TPS75105DSKR	SON	DSK	10	3000	179.0	8.4	2.73	2.73	0.8	4.0	8.0	Q2
TPS75105DSKT	SON	DSK	10	250	179.0	8.4	2.73	2.73	0.8	4.0	8.0	Q2
TPS75105YFFR	DSBGA	YFF	9	3000	180.0	8.4	1.45	1.45	0.8	4.0	8.0	Q1
TPS75105YFFT	DSBGA	YFF	9	250	180.0	8.4	1.45	1.45	0.8	4.0	8.0	Q1

**TAPE AND REEL BOX DIMENSIONS**


\*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
TPS75100DSKR	SON	DSK	10	3000	200.0	183.0	25.0
TPS75100DSKT	SON	DSK	10	250	203.0	203.0	35.0
TPS75100YFFR	DSBGA	YFF	9	3000	182.0	182.0	20.0
TPS75100YFFT	DSBGA	YFF	9	250	182.0	182.0	20.0
TPS75103YFFR	DSBGA	YFF	9	3000	182.0	182.0	20.0
TPS75103YFFT	DSBGA	YFF	9	250	182.0	182.0	20.0
TPS75105DSKR	SON	DSK	10	3000	200.0	183.0	25.0
TPS75105DSKT	SON	DSK	10	250	200.0	183.0	25.0
TPS75105YFFR	DSBGA	YFF	9	3000	182.0	182.0	20.0
TPS75105YFFT	DSBGA	YFF	9	250	182.0	182.0	20.0

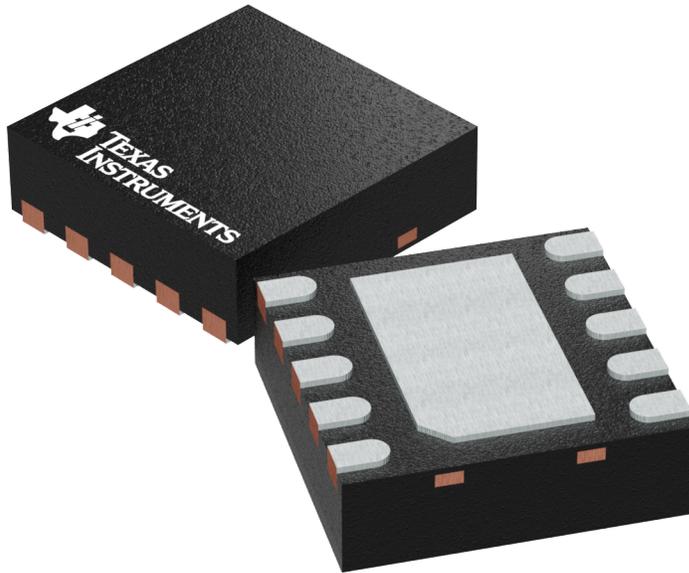
## GENERIC PACKAGE VIEW

**DSK 10**

**WSON - 0.8 mm max height**

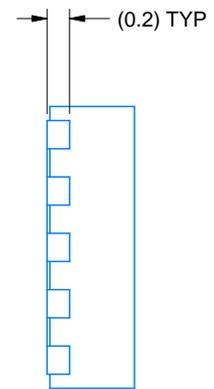
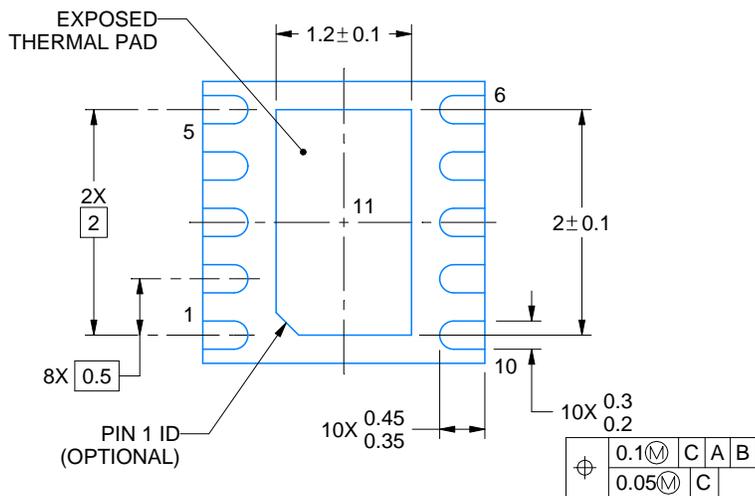
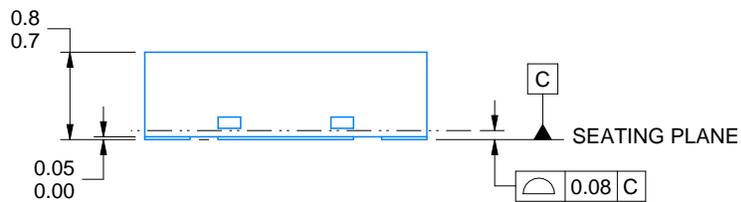
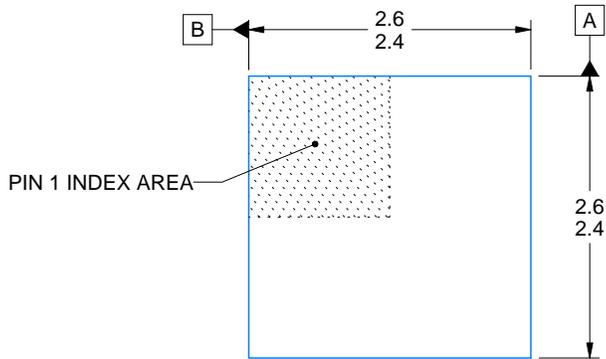
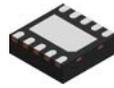
**2.5 x 2.5 mm, 0.5 mm pitch**

PLASTIC SMALL OUTLINE - NO LEAD



Images above are just a representation of the package family, actual package may vary.  
Refer to the product data sheet for package details.

4225304/A



4218903/B 10/2020

NOTES:

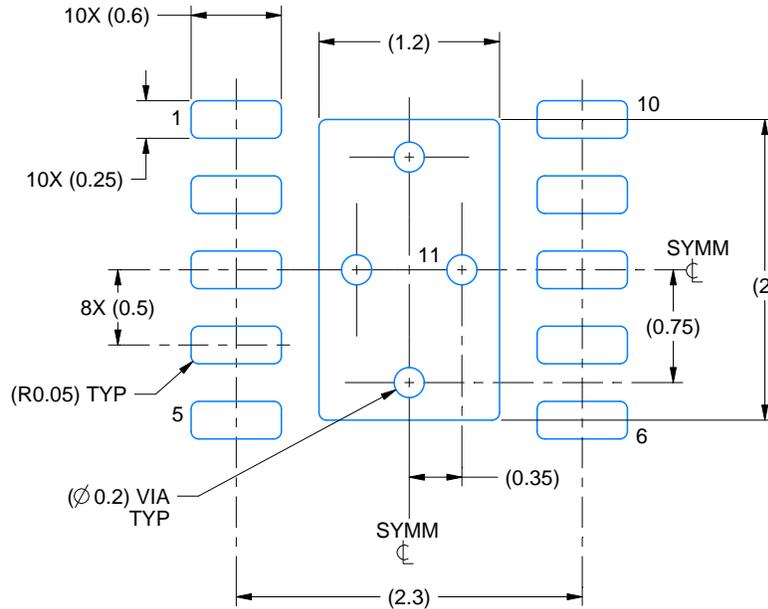
1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. The package thermal pad must be soldered to the printed circuit board for thermal and mechanical performance.

# EXAMPLE BOARD LAYOUT

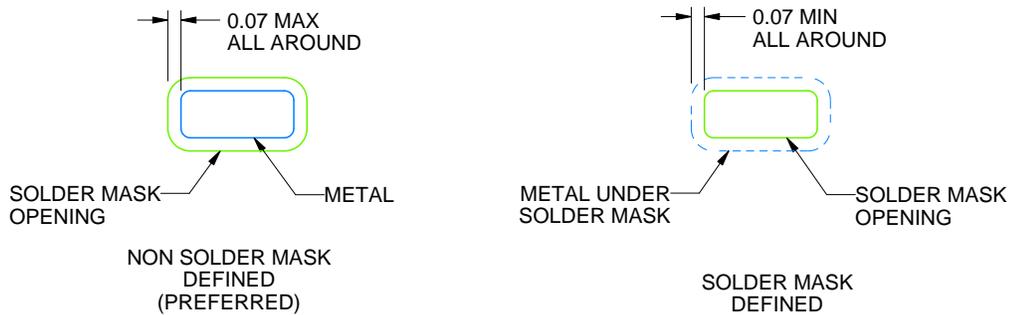
DSK0010A

WSON - 0.8 mm max height

PLASTIC SMALL OUTLINE - NO LEAD



LAND PATTERN EXAMPLE  
SCALE:20X



SOLDER MASK DETAILS

4218903/B 10/2020

NOTES: (continued)

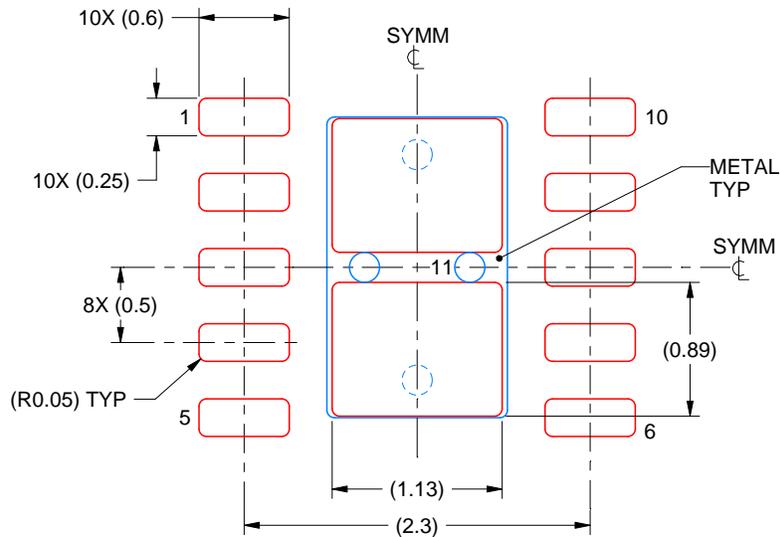
4. This package is designed to be soldered to a thermal pad on the board. For more information, see Texas Instruments literature number SLUA271 ([www.ti.com/lit/slue271](http://www.ti.com/lit/slue271)).
5. Vias are optional depending on application, refer to device data sheet. If some or all are implemented, recommended via locations are shown.

# EXAMPLE STENCIL DESIGN

DSK0010A

WSON - 0.8 mm max height

PLASTIC SMALL OUTLINE - NO LEAD



SOLDER PASTE EXAMPLE  
BASED ON 0.125 mm THICK STENCIL

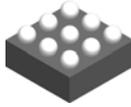
EXPOSED PAD 11  
84% PRINTED SOLDER COVERAGE BY AREA  
SCALE:20X

4218903/B 10/2020

NOTES: (continued)

6. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.

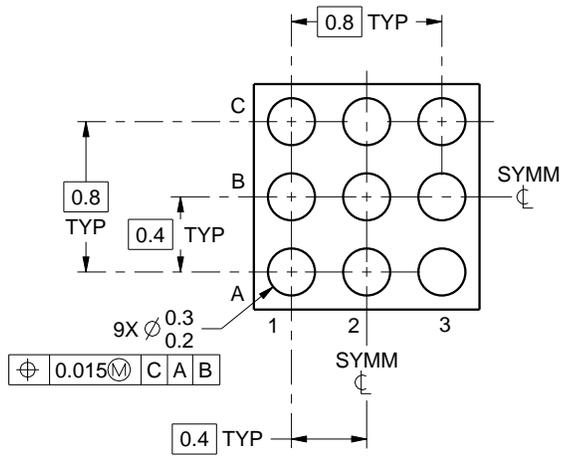
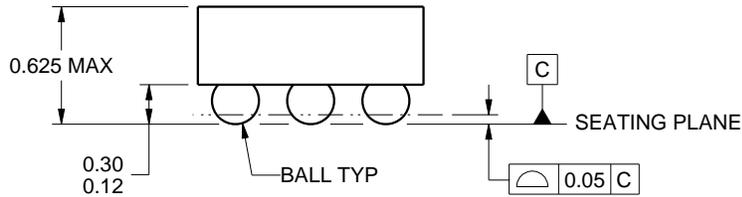
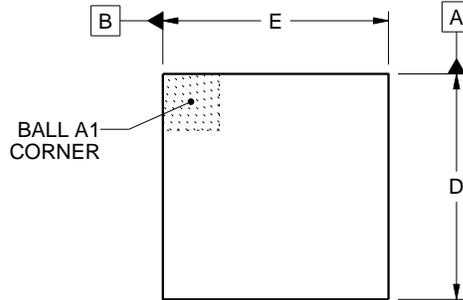
YFF0009



# PACKAGE OUTLINE

## DSBGA - 0.625 mm max height

DIE SIZE BALL GRID ARRAY



D: Max = 1.238 mm, Min = 1.178 mm  
 E: Max = 1.238 mm, Min = 1.178 mm

4219552/A 05/2016

NOTES:

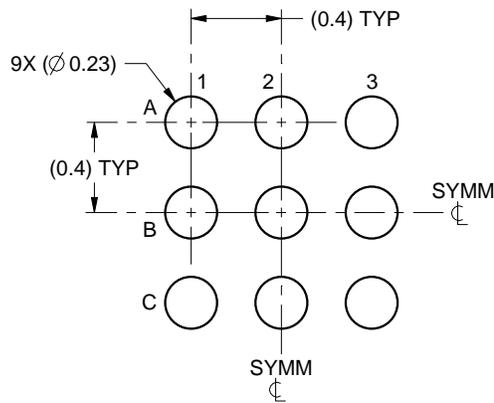
1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.

# EXAMPLE BOARD LAYOUT

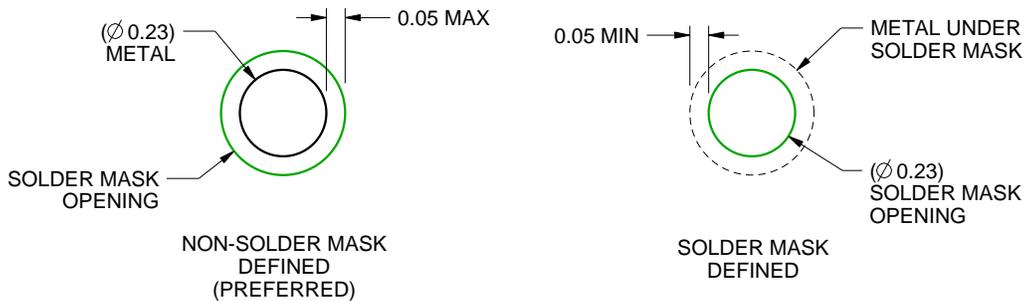
YFF0009

DSBGA - 0.625 mm max height

DIE SIZE BALL GRID ARRAY



LAND PATTERN EXAMPLE  
SCALE:30X



SOLDER MASK DETAILS  
NOT TO SCALE

4219552/A 05/2016

NOTES: (continued)

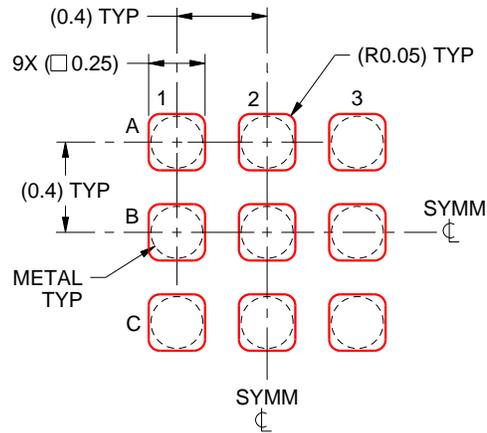
3. Final dimensions may vary due to manufacturing tolerance considerations and also routing constraints. For more information, see Texas Instruments literature number SNVA009 ([www.ti.com/lit/snva009](http://www.ti.com/lit/snva009)).

# EXAMPLE STENCIL DESIGN

YFF0009

DSBGA - 0.625 mm max height

DIE SIZE BALL GRID ARRAY



SOLDER PASTE EXAMPLE  
BASED ON 0.1 mm THICK STENCIL  
SCALE:30X

4219552/A 05/2016

NOTES: (continued)

4. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release.

## IMPORTANT NOTICE AND DISCLAIMER

TI PROVIDES TECHNICAL AND RELIABILITY DATA (INCLUDING DATA SHEETS), DESIGN RESOURCES (INCLUDING REFERENCE DESIGNS), APPLICATION OR OTHER DESIGN ADVICE, WEB TOOLS, SAFETY INFORMATION, AND OTHER RESOURCES "AS IS" AND WITH ALL FAULTS, AND DISCLAIMS ALL WARRANTIES, EXPRESS AND IMPLIED, INCLUDING WITHOUT LIMITATION ANY IMPLIED WARRANTIES OF MERCHANTABILITY, FITNESS FOR A PARTICULAR PURPOSE OR NON-INFRINGEMENT OF THIRD PARTY INTELLECTUAL PROPERTY RIGHTS.

These resources are intended for skilled developers designing with TI products. You are solely responsible for (1) selecting the appropriate TI products for your application, (2) designing, validating and testing your application, and (3) ensuring your application meets applicable standards, and any other safety, security, regulatory or other requirements.

These resources are subject to change without notice. TI grants you permission to use these resources only for development of an application that uses the TI products described in the resource. Other reproduction and display of these resources is prohibited. No license is granted to any other TI intellectual property right or to any third party intellectual property right. TI disclaims responsibility for, and you will fully indemnify TI and its representatives against, any claims, damages, costs, losses, and liabilities arising out of your use of these resources.

TI's products are provided subject to [TI's Terms of Sale](#) or other applicable terms available either on [ti.com](https://www.ti.com) or provided in conjunction with such TI products. TI's provision of these resources does not expand or otherwise alter TI's applicable warranties or warranty disclaimers for TI products.

TI objects to and rejects any additional or different terms you may have proposed.

Mailing Address: Texas Instruments, Post Office Box 655303, Dallas, Texas 75265  
Copyright © 2024, Texas Instruments Incorporated