INTEGRATED CIRCUITS
UNITRODE

UC1832
UC2832/3
UC3832/3

Precision Low Dropout Linear Controllers

FEATURES

- Precision 1% Reference
- Over-Current Sense Threshold Accurate to 5%
- Programmable Duty-Ratio Over-Current Protection
- 4.5 V to 36 V Operation
- 100mA Output Drive, Source, or Sink
- Under-Voltage Lockout

Additional Features of the UC2832 series:

- Adjustable Current Limit to Current Sense Ratio
- Separate $+V_{IN}$ terminal
- Programmable Driver Current Limit
- Access to V_{REF} and E/A(+)
- Logic-Level Disable Input

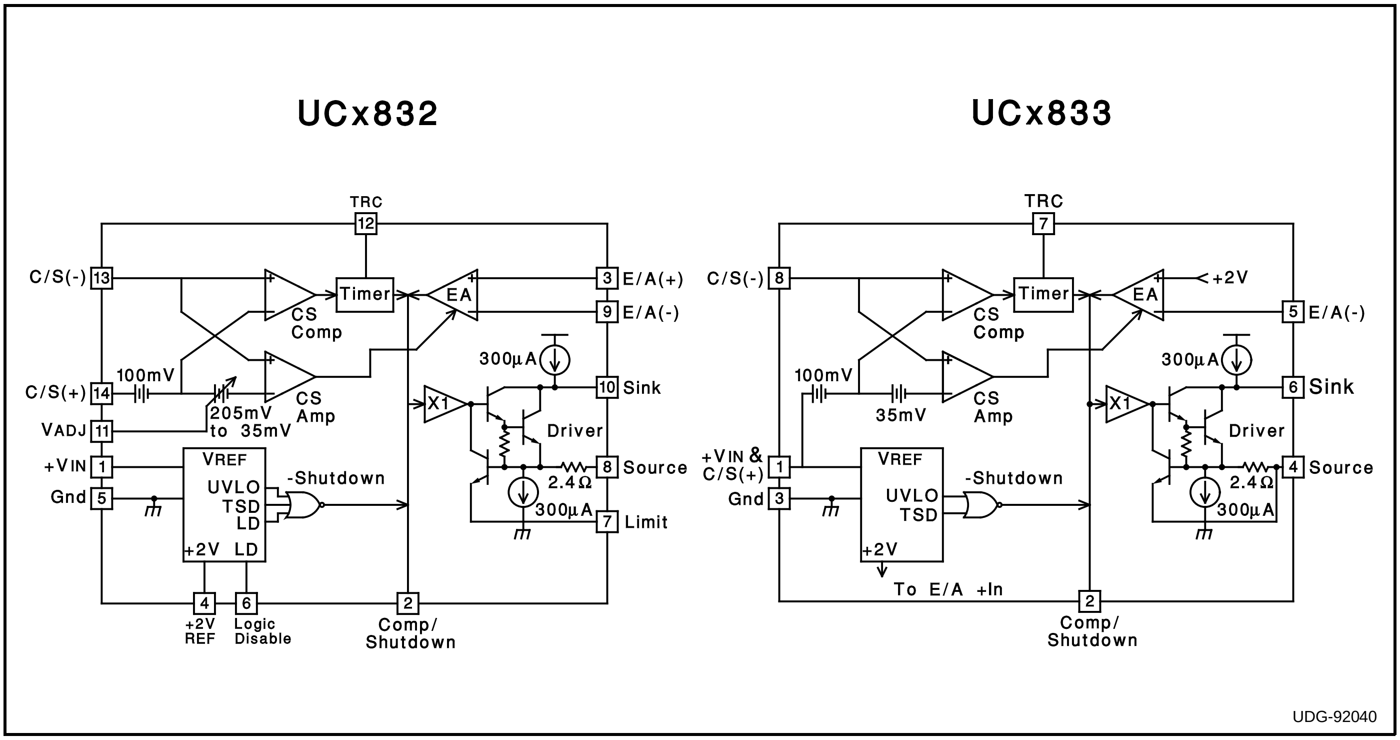
DESCRIPTION

The UC2832 and UC3833 series of precision linear regulators include all the control functions required in the design of very low dropout linear regulators. Additionally, they feature an innovative duty-ratio current limiting technique which provides peak load capability while limiting the average power dissipation of the external pass transistor during fault conditions. When the load current reaches an accurately programmed threshold, a gated-astable timer is enabled, which switches the regulator's pass device off and on at an externally programmable duty-ratio. During the on-time of the pass element, the output current is limited to a value slightly higher than the trip threshold of the duty-ratio timer. The constant-current-limit is programmable on the UCx832 to allow higher peak current during the on-time of the pass device. With duty-ratio control, high initial load demands and short circuit protection may both be accommodated without extra heat sinking or foldback current limiting. Additionally, if the timer pin is grounded, the duty-ratio timer is disabled, and the IC operates in constant-voltage/constant-current regulating mode.

These IC's include a 2 Volt (±1%) reference, error amplifier, UVLO, and a high current driver that has both source and sink outputs, allowing the use of either NPN or PNP external pass transistors. Safe operation is assured by the inclusion of under-voltage lockout (UVLO) and thermal shutdown.

The UC3833 family includes the basic functions of this design in a low-cost, 8-pin mini-dip package, while the UC2832 series provides added versatility with the availability of 14 pins. Packaging options include plastic (N suffix), or ceramic (J suffix). Specified operating temperature ranges are: commercial (0°C to 70°C), order UC3832/3 (N or J); and industrial (–40°C to 85°C), order UC2832/3 (N or J). Surface mount packaging is also available.

BLOCK DIAGRAMS



SLUS387A - JUNE 1994 - REVISED - MAY 2003

ABSOLUTE MAXIMUM RATINGS

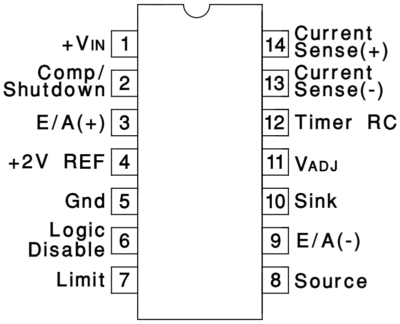
Supply Voltage $+V_{IN}$	40V
Driver Output Current (Sink or Source)	450mA
Driver Sink to Source Voltage	40V
TRC Pin Voltage	–0.3V to 3.2V
Other Input Voltages	–0.3V to $+V_{IN}$
Operating Junction Temperature (note 2)	–55°C to +150°C
Storage Temperature	–65°C to +150°C
Lead Temperature (Soldering, 10 Seconds)	300°C

Note 1: Unless otherwise indicated, voltages are referenced to ground and currents are positive into, negative out of, the specified terminals.
Note 2: See Unitrode Integrated Circuits databook for information regarding thermal specifications and limitations of packages.

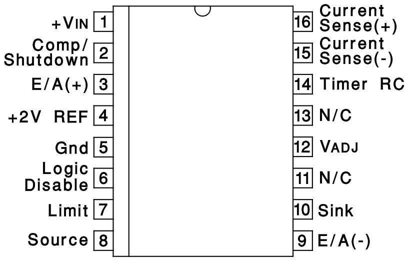
CONNECTION DIAGRAMS

UC2832

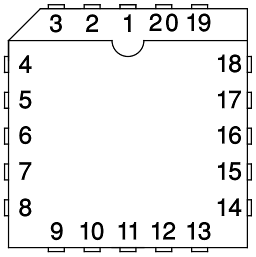
DIL-14 (Top View)
J Or N Package



SOIC-16 (Top View)
DW Package



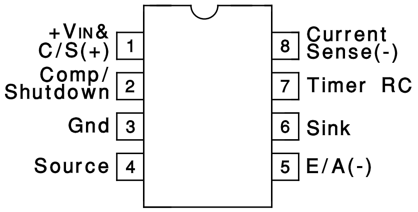
LCC-20 & PLCC-20
L & Q Package
(Top View)



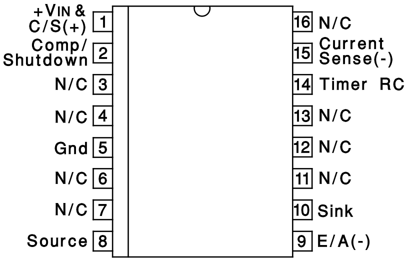
PACKAGE PIN FUNCTION	
FUNCTION	PIN
N/C	1
$+V_{IN}$	2
Comp/Shutdown	3
E/A(+)	4
+2V REF	5
N/C	6
Gnd	7
Logic Disable	8
Limit	9
Source	10
N/C	11
E/A(-)	12
Sink	13
V_{ADJ}	14
N/C	15-17
Timer RC	18
Current Sense(-)	19
Current Sense(+)	20

UC3833

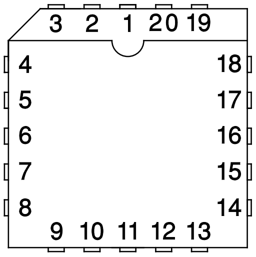
DIL-8 (Top View)
J Or N Package



SOIC-16 (Top View)
DW Package



LCC-20 & PLCC-20
L & Q Package
(Top View)



PACKAGE PIN FUNCTION	
FUNCTION	PIN
$+V_{IN}$ & C/S(+)	1
N/C	2
N/C	3
N/C	4
Comp/Shutdown	5
Gnd	6
N/C	7
N/C	8
N/C	9
Source	10
N/C	11
E/A(-)	12
N/C	13
N/C	14
Sink	15
Timer RC	16
Current Sense(+)	17
N/C	18-20

ELECTRICAL CHARACTERISTICS: Unless otherwise stated, specifications hold for T_A = 0°C to 70°C for the UC3832/3, –40°C to 85°C for the UC2832/3, $+V_{IN}$ = 15V, Driver sink = $+V_{IN}$, C/S(+) voltage = $+V_{IN}$. T_A=T_J.

PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNITS
Input Supply					
Supply Current	$+V_{IN}$ = 6 V		6.5	10	mA
	$+V_{IN}$ = 36 V		9.5	15	mA
	Logic Disable = 2 V (UCx832 only)		3.3		mA
Reference Section					
Output Voltage (Note 3)	T_J = 25°C, I_{DRIVER} = 10 mA	1.98	2.00	2.02	V
	over temperature, I_{DRIVER} = 10 mA	1.96	2.00	2.04	V
Load Regulation (UCx832 only)	I_O = 0 to 10 m	-10	-5.0		mV
Line Regulation	$+V_{IN}$ = 4.5 V to 36 V, I_{DRIVER} = 10 m		0.033	0.5	mV/V
Under-Voltage Lockout Threshold			3.6	4.5	V
Logic Disable Input (UCx832 only)					
Threshold Voltage		1.3	1.4	1.5	V
Input Bias Current	Logic Disable = 0 V	-5.0	-1.0		µA
Current Sense Section					
Comparator Offset		95	100	105	mV
	Over Temperature	93	100	107	mV
Amplifier Offset (UCx833 only)		110	135	170	mV
Amplifier Offset (UCx832 only)	V_{ADJ} = Open	110	135	170	mV
	V_{ADJ} = 1 V	180	235	290	mV
	V_{ADJ} = 0 V	250	305	360	mV
Input Bias Current	V_{CM} = $+V_{IN}$	65	100	135	µA
Input Offset Current (UCx832 only)	V_{CM} = $+V_{IN}$	-10		10	µA
Amplifier CMRR (UCx832 only)	V_{CM} = 4.1 V to + V_{IN} + 0.3		80		dB
Transconductance	I_{COMP} = ±100 µA		65		mS
V_{ADJ} Input Current (UCx832 only)	V_{ADJ} = 0V	-10	-1		µA
Timer					
Inactive Leakage Current	C/S(+) = C/S(-) = $+V_{IN}$; TRC pin = 2 V		0.25	1.0	µA
Active Pullup Current	C/S(+) = $+V_{IN}$, C/S(-) = $+V_{IN}$ - 0.4V; TRC pin = 0 V	-345	-270	-175	µA
Duty Ratio (note 4)	ontime/period, R_T = 200k, C_T = 0.27µF		4.8		%
Period (notes 4,5)	ontime + offtime, R_T = 200k, C_T = 0.27µF		36		ms
Upper Trip Threshold (Vu)			1.8		V
Lower Trip Threshold (Vl)			0.9		V
Trip Threshold Ratio	Vu/Vl		2.0		V/V
Error Amplifier					
Input Offset Voltage (UCx832 only)	V_{CM} = V_{COMP} = 2 V	-8.0		8.0	mV
Input Bias Current	V_{CM} = V_{COMP} = 2 V	-4.5	-1.1		µA
Input Offset Current (UCx832 only)	V_{CM} = V_{COMP} = 2 V	-1.5		1.5	µA
AVOL	V_{COMP} = 1 V to 13 V	50	70		dB
CMRR (UCx832 only)	V_{CM} = 0V to $+V_{IN}$ - 3 V	60	80		dB
PSRR (UCx832 only)	V_{CM} = 2 V, $+V_{IN}$ = 4.5 V to 36		90		dB
Transconductance	I_{COMP} = ±10 µA		43		mS
VOH	I_{COMP} = 0, Volts below $+V_{IN}$		.95	1.3	V
VOL	I_{COMP} = 0		.45	0.7	V
IOH	V_{COMP} = 2 V	-700	-500	-100	µA

ELECTRICAL CHARACTERISTICS (cont.)

Unless otherwise stated, specifications hold for T_A = 0°C to 70°C for the UC3832/3, –40°C to 85°C for the UC2832/3, +VIN = 15 V, Driver sink = +V_{IN}, C/S(+) voltage = +V_{IN}. T_A=T_J.

PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNITS
Error Amplifier (cont.)					
IOL	V_{COMP} = 2 V, C/S(-) = +V_{IN}	100	500	700	µA
	V_{COMP} = 2 V, C/S(-) = +V_{IN} - 0.4 V	2	6		mA
Driver					
Maximum Current	Driver Limit & Source pins common; T_J = 25°C	200	300	400	mA
	Over Temperature	100	300	450	mA
Limiting Voltage (UCx832 only)	Driver Limit to Source voltage at current limit, I_{SOURCE} = -10 mA; T_J = 25°C (Note 6)		.72		V
Internal Current Sense Resistance	T_J = 25°C (Note 6)		2.4		Ω
Pull-Up Current at Driver Sink	Compensation/Shutdown = 0.4 V; Driver Sink = +V_{IN} - 1V	-800	-300	-100	µA
	Compensation/Shutdown = 0.4 V, +V_{IN} = 36 V; Driver Sink = 35 V	-1000	-300	-75	µA
Pull-Down Current at Driver Source	Compensation/Shutdown = 0.4 V; Driver Source = 1 V	150	300	700	µA
Saturation Voltage Sink to Source	Driver Source = 0 V; Driver Current = 100 mA		1.5		V
Maximum Source Voltage	Driver Sink = +V_{IN}, Driver Current = 100 mA Volts below + V_{IN}		3.0		V
UVLO Sink Leakage	+V_{IN} = C/S(+) = C/S(-) = 2.5 V, Driver Sink = 15 V, Driver Source = 0 V, TA = 25°C		25		µA
Maximum Reverse Source Voltage	Compensation/Shutdown = 0 V; I_{SOURCE} = 100 µA, +V_{IN} = 3 V		1.6		V
Thermal Shutdown			160		°C

Note 3: On the UCx833 this voltage is defined as the regulating level at the error amplifier inverting input, with the error amplifier driving V_{SOURCE} to 2 V.

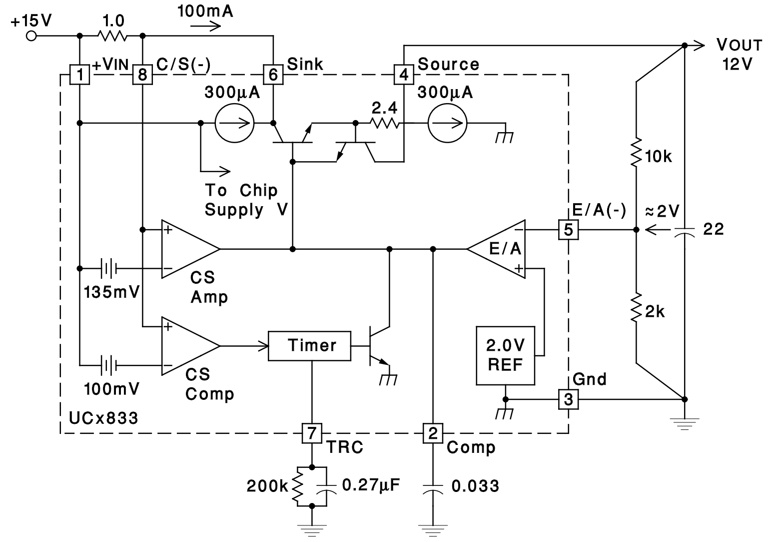
Note 4: These parameters are first-order supply-independent, however both may vary with supply for +V_{IN} less than about 4 V. This supply variation will cause a slight change in the timer period and duty cycle, although a high off-time/on-time ratio will be maintained.

Note 5: With recommended R_T value of 200k, $T_{OFF} \approx R_T C_T * \ln(V_u/V_l) \pm 10\%$.

Note 6: The internal current limiting voltage has a temperature dependence of approximately -2.0 mV/°C, or -2800 ppm/°C. The internal 2.4 Ω sense resistor has a temperature dependance of approximately +1500 ppm/°C.

APPLICATION AND OPERATION INFORMATION

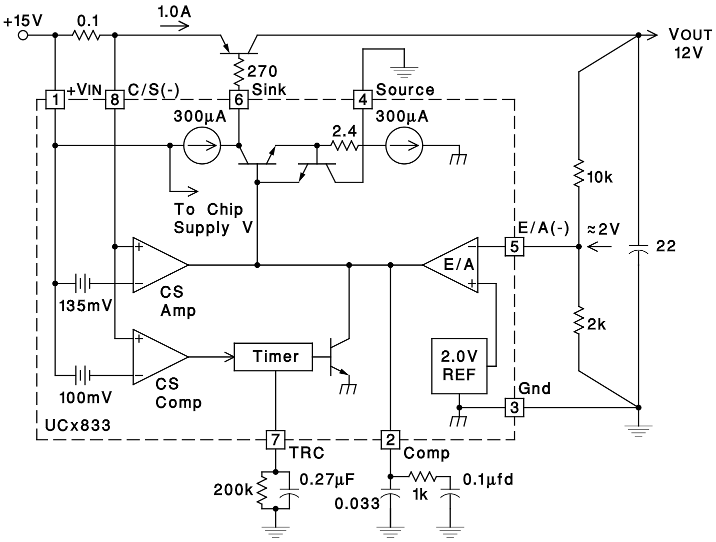
NPN Pass (Local 100mA Regulator) (UCx833)



UDG-92041-1

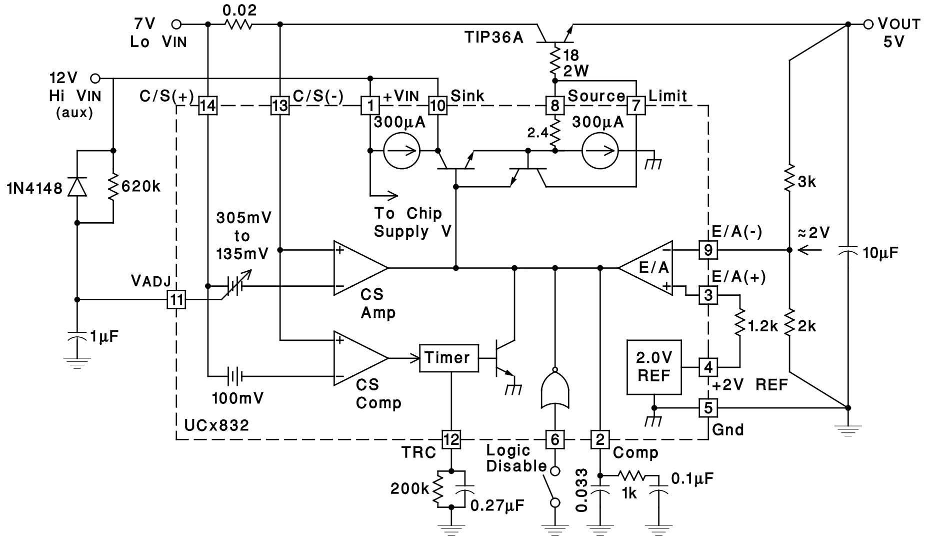
APPLICATION AND OPERATION INFORMATION (cont.)

PNP Pass (Low Drop-Out Regulator) (UCx833)



UDG-92042-1

NPN Pass (Medium Power, Low Drop-Out Regulator) (UCx832)



UDG-92043-1

Estimating Maximum Load Capacitance

For any power supply, the rate at which the total output capacitance can be charged depends on the maximum output current available and on the nature of the load. For a constant-current current-limited power supply, the output will come up if the load asks for less than the maximum available short-circuit limit current.

To guarantee recovery of a duty-ratio current-limited power supply from a short-circuited load condition, there is a maximum total output capacitance which can be charged for a given unit ON time. The design value of ON time can be adjusted by changing the timing capacitor. Nominally, $T_{ON} = 0.693 \times 10k \times C_T$.

Typically, the IC regulates output current to a maximum of $I_{MAX} = K \times I_{TH}$, where I_{TH} is the timer trip-point current,

and $$K = \frac{\text{Current Sense Amplifier Offset Voltage}}{100mA}$$

≈1.35 for UCx833, and is variable from 1.35 to 3.05 with V_{ADJ} for the UCx832.

For a worst-case constant-current load of value just less than I_{TH}, C_{MAX} can be estimated from:

$$C_{MAX} = ((K-1) I_{TH}) \left(\frac{T_{ON}}{V_{OUT}}\right),$$

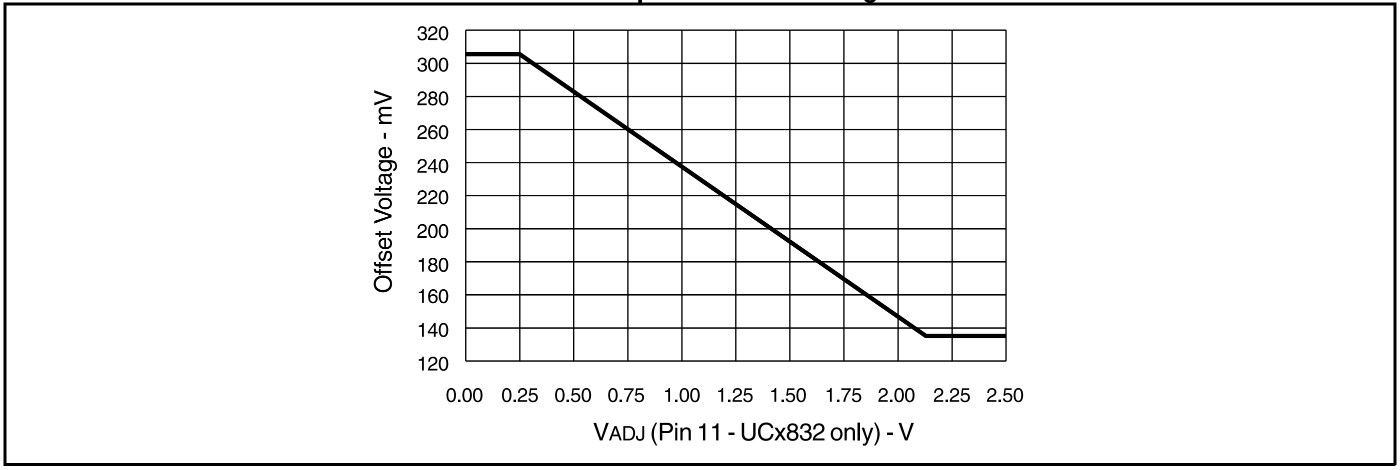
where V_{OUT} is the nominal regulator output voltage.

For a resistive load of value R_L, the value of C_{MAX} can be estimated from:

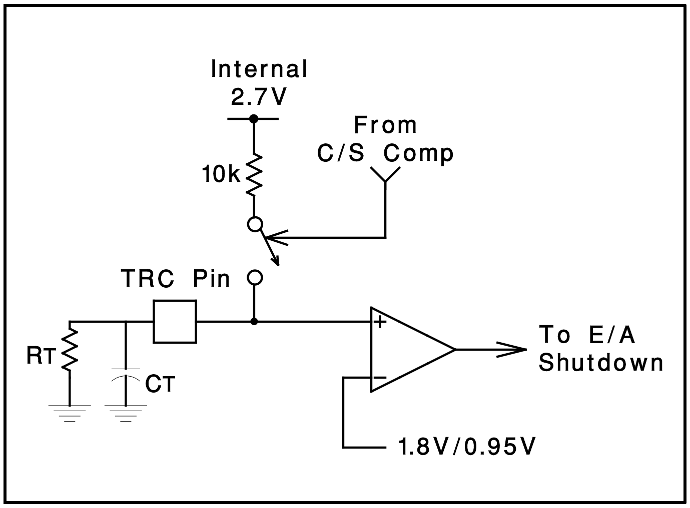
$$C_{MAX} = \frac{T_{ON}}{R_L} \bullet \frac{1}{ln\left[\left(1 - \frac{V_{OUT}}{K \bullet I_{TH} \bullet R_L}\right)^{-1}\right]}.$$

APPLICATION AND OPERATION INFORMATION (cont.)

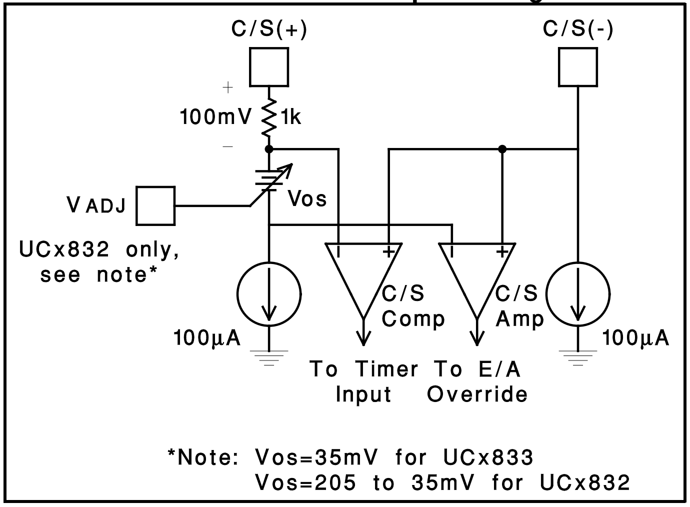
Current Sense Amplifier Offset Voltage vs VADJ



UCx832/33 Timer Function

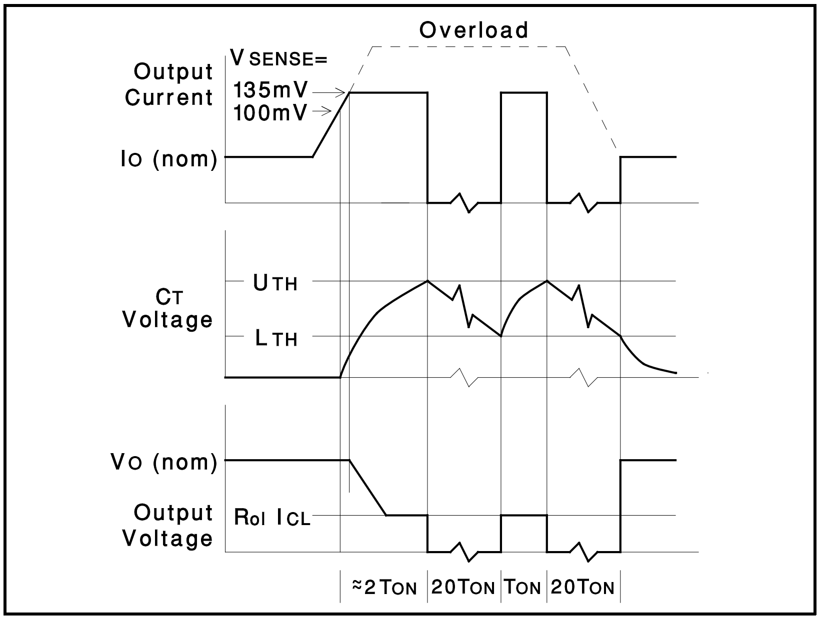


UCx832/33 Current Sense Input Configuration

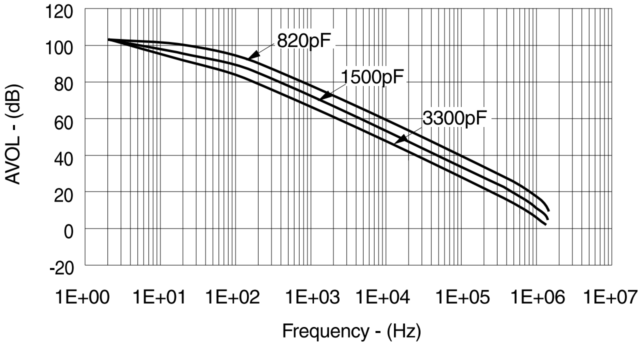


*Note: Vos=35mV for UCx833
Vos=205 to 35mV for UCx832

Load current, timing capacitor voltage, and output voltage of the regulator under fault conditions.

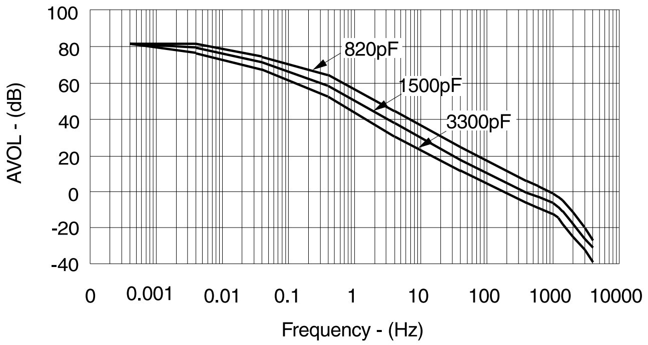


APPLICATION AND OPERATION INFORMATION (cont.)



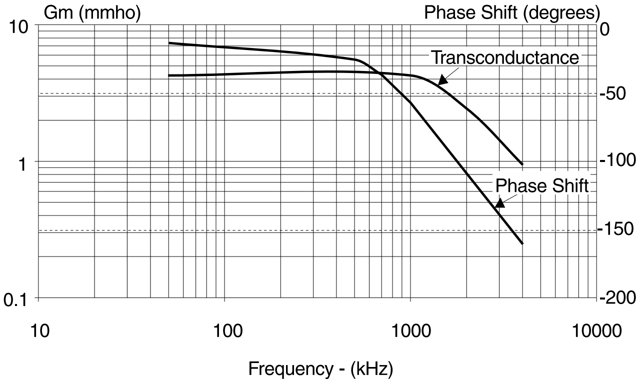
UCx832 Error Amplifier

AVOL vs Frequency and CC



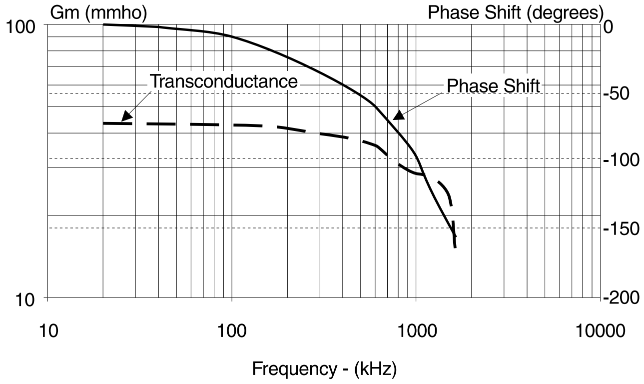
UCx832 Current Sense Amplifier

AVOL vs Frequency and CC



UCx832 Error Amplifier

Transconductance and Phase vs Frequency



UCx832 Current Sense Amplifier

Transconductance and Phase vs Frequency

PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead finish/ Ball material (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
5962-9326501M2A	ACTIVE	LCCC	FK	20	55	Non-RoHS & Green	SNPB	N / A for Pkg Type	-55 to 125	5962-9326501M2A UC1832L/883B	Samples
5962-9326501MCA	ACTIVE	CDIP	J	14	25	Non-RoHS & Green	SNPB	N / A for Pkg Type	-55 to 125	5962-9326501MCA UC1832J/883B	Samples
5962-9326501V2A	ACTIVE	LCCC	FK	20	55	Non-RoHS & Green	SNPB	N / A for Pkg Type	-55 to 125	5962-9326501V2A UC1832LQMLV	Samples
5962-9326501VCA	ACTIVE	CDIP	J	14	25	Non-RoHS & Green	SNPB	N / A for Pkg Type	-55 to 125	5962-9326501VCA UC1832JQMLV	Samples
UC1832J	ACTIVE	CDIP	J	14	25	Non-RoHS & Green	SNPB	N / A for Pkg Type	-55 to 125	UC1832J	Samples
UC1832J883B	ACTIVE	CDIP	J	14	25	Non-RoHS & Green	SNPB	N / A for Pkg Type	-55 to 125	5962-9326501MCA UC1832J/883B	Samples
UC1832L883B	ACTIVE	LCCC	FK	20	55	Non-RoHS & Green	SNPB	N / A for Pkg Type	-55 to 125	5962-9326501M2A UC1832L/883B	Samples
UC2832DW	ACTIVE	SOIC	DW	16	40	RoHS & Green	NIPDAU	Level-2-260C-1 YEAR	-25 to 85	UC2832DW	Samples
UC2833DW	ACTIVE	SOIC	DW	16	40	RoHS & Green	NIPDAU	Level-2-260C-1 YEAR	-40 to 85	UC2833DW	Samples
UC2833DWG4	ACTIVE	SOIC	DW	16	40	RoHS & Green	NIPDAU	Level-2-260C-1 YEAR	-40 to 85	UC2833DW	Samples
UC2833DWTR	ACTIVE	SOIC	DW	16	2000	RoHS & Green	NIPDAU	Level-2-260C-1 YEAR	-40 to 85	UC2833DW	Samples
UC3832DW	ACTIVE	SOIC	DW	16	40	RoHS & Green	NIPDAU	Level-2-260C-1 YEAR	0 to 70	UC3832DW	Samples
UC3833DW	ACTIVE	SOIC	DW	16	40	RoHS & Green	NIPDAU	Level-2-260C-1 YEAR	0 to 70	UC3833DW	Samples
UC3833DWTR	ACTIVE	SOIC	DW	16	2000	RoHS & Green	NIPDAU	Level-2-260C-1 YEAR	0 to 70	UC3833DW	Samples

[1] The marketing status values are defined as follows:
ACTIVE: Product device recommended for new designs.
LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
PREVIEW: Device has been announced but is not in production. Samples may or may not be available.
OBSOLETE: TI has discontinued the production of the device.

[2] **RoHS:** TI defines "RoHS" to mean semiconductor products that are compliant with the current EU RoHS requirements for all 10 RoHS substances, including the requirement that RoHS substance do not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, "RoHS" products are suitable for use in specified lead-free processes. TI may reference these types of products as "Pb-Free".
RoHS Exempt: TI defines "RoHS Exempt" to mean products that contain lead but are compliant with EU RoHS pursuant to a specific EU RoHS exemption.
Green: TI defines "Green" to mean the content of Chlorine (Cl) and Bromine (Br) based flame retardants meet JS709B low halogen requirements of <=1000ppm threshold. Antimony trioxide based flame retardants must also meet the <=1000ppm threshold requirement.

[3] MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

[4] There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

[5] Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

[6] Lead finish/Ball material - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

Important Information and Disclaimer: The information provided on this page represents TI's knowledge and belief as of the date that it is provided. TI bases its knowledge and belief on information provided by third parties, and makes no representation or warranty as to the accuracy of such information. Efforts are underway to better integrate information from third parties. TI has taken and continues to take reasonable steps to provide representative and accurate information but may not have conducted destructive testing or chemical analysis on incoming materials and chemicals. TI and TI suppliers consider certain information to be proprietary, and thus CAS numbers and other limited information may not be available for release.

In no event shall TI's liability arising out of such information exceed the total purchase price of the TI part(s) at issue in this document sold by TI to Customer on an annual basis.

OTHER QUALIFIED VERSIONS OF UC1832, UC1832-SP, UC2832, UC3832 :

- Catalog : UC3832, UC1832

- Enhanced Product : UC2832-EP

- Military : UC1832

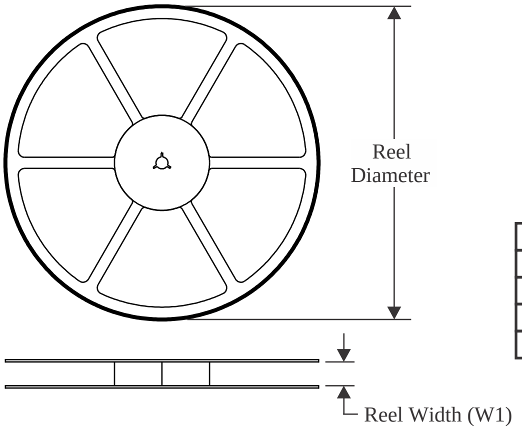
- Space : UC1832-SP

NOTE: Qualified Version Definitions:

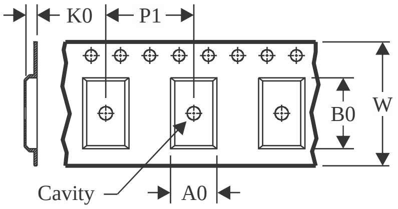
- Catalog - TI's standard catalog product
- Enhanced Product - Supports Defense, Aerospace and Medical Applications
- Military - QML certified for Military and Defense Applications
- Space - Radiation tolerant, ceramic packaging and qualified for use in Space-based application

TAPE AND REEL INFORMATION

REEL DIMENSIONS

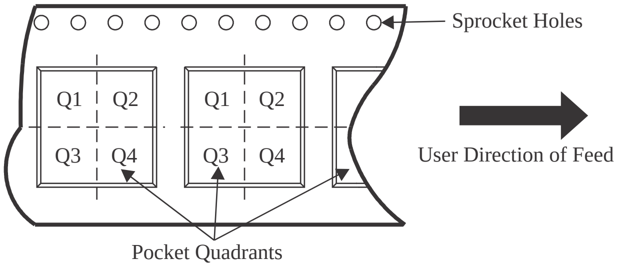


TAPE DIMENSIONS



A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

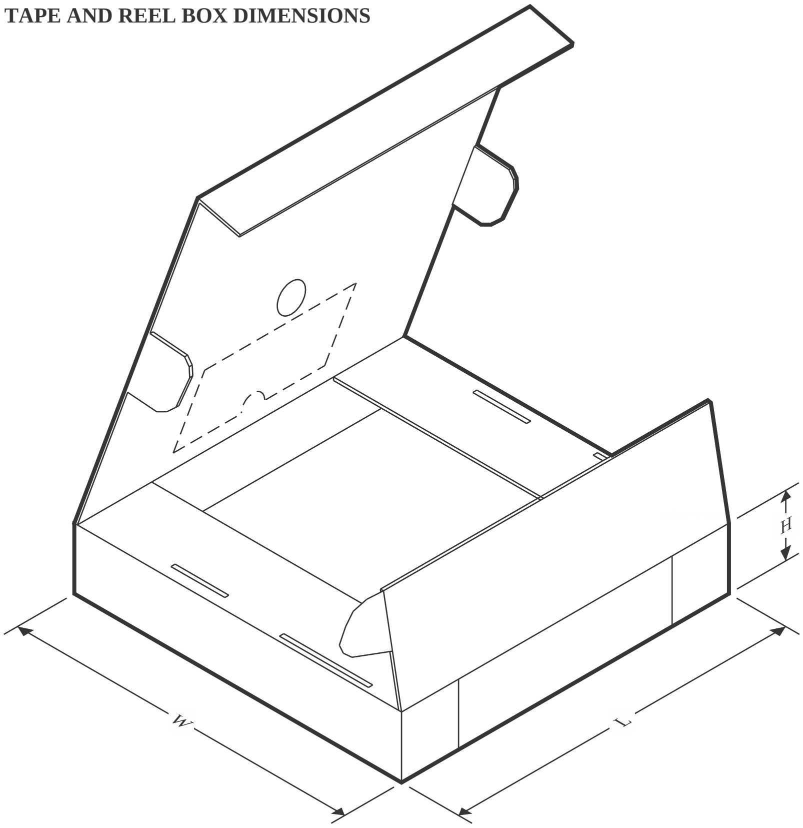
QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
UC2833DWTR	SOIC	DW	16	2000	330.0	16.4	10.75	10.7	2.7	12.0	16.0	Q1
UC3833DWTR	SOIC	DW	16	2000	330.0	16.4	10.75	10.7	2.7	12.0	16.0	Q1

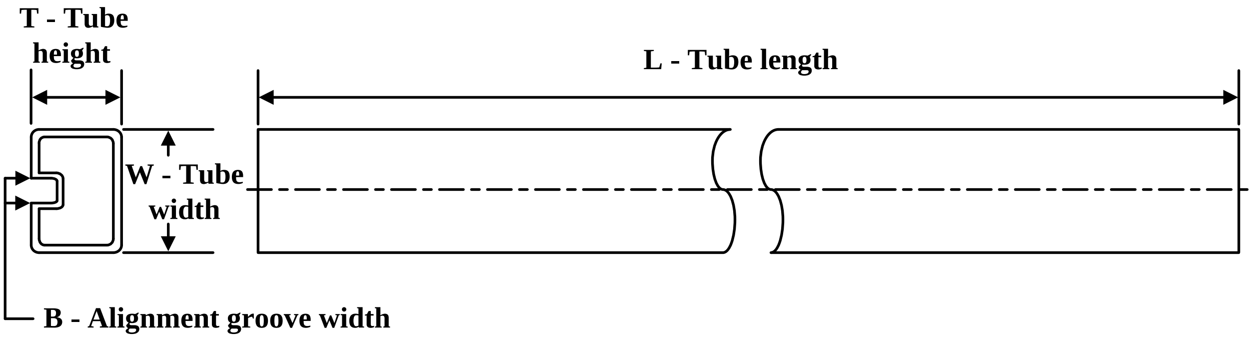
TAPE AND REEL BOX DIMENSIONS



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
UC2833DWTR	SOIC	DW	16	2000	356.0	356.0	35.0
UC3833DWTR	SOIC	DW	16	2000	356.0	356.0	35.0

TUBE



*All dimensions are nominal

Device	Package Name	Package Type	Pins	SPQ	L (mm)	W (mm)	T (µm)	B (mm)
5962-9326501M2A	FK	LCCC	20	55	506.98	12.06	2030	NA
5962-9326501V2A	FK	LCCC	20	55	506.98	12.06	2030	NA
UC1832L883B	FK	LCCC	20	55	506.98	12.06	2030	NA
UC2832DW	DW	SOIC	16	40	507	12.83	5080	6.6
UC2833DW	DW	SOIC	16	40	507	12.83	5080	6.6
UC2833DWG4	DW	SOIC	16	40	507	12.83	5080	6.6
UC3832DW	DW	SOIC	16	40	507	12.83	5080	6.6
UC3833DW	DW	SOIC	16	40	507	12.83	5080	6.6

GENERIC PACKAGE VIEW

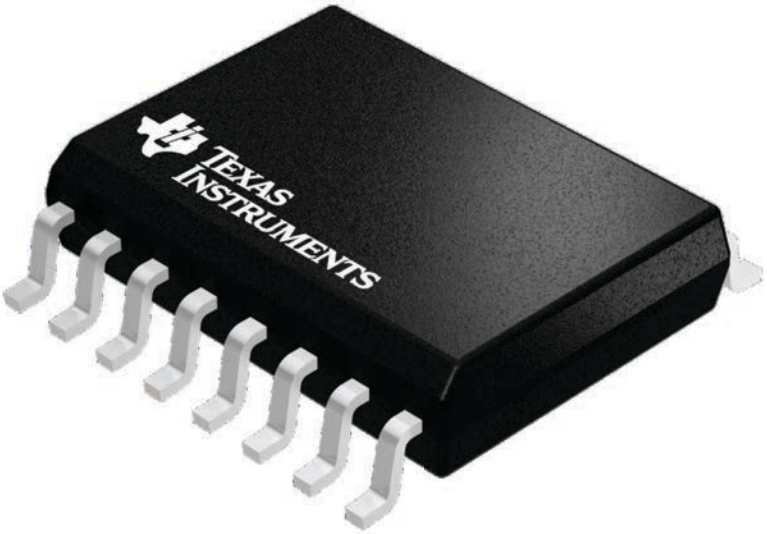
DW 16

SOIC - 2.65 mm max height

7.5 x 10.3, 1.27 mm pitch

SMALL OUTLINE INTEGRATED CIRCUIT

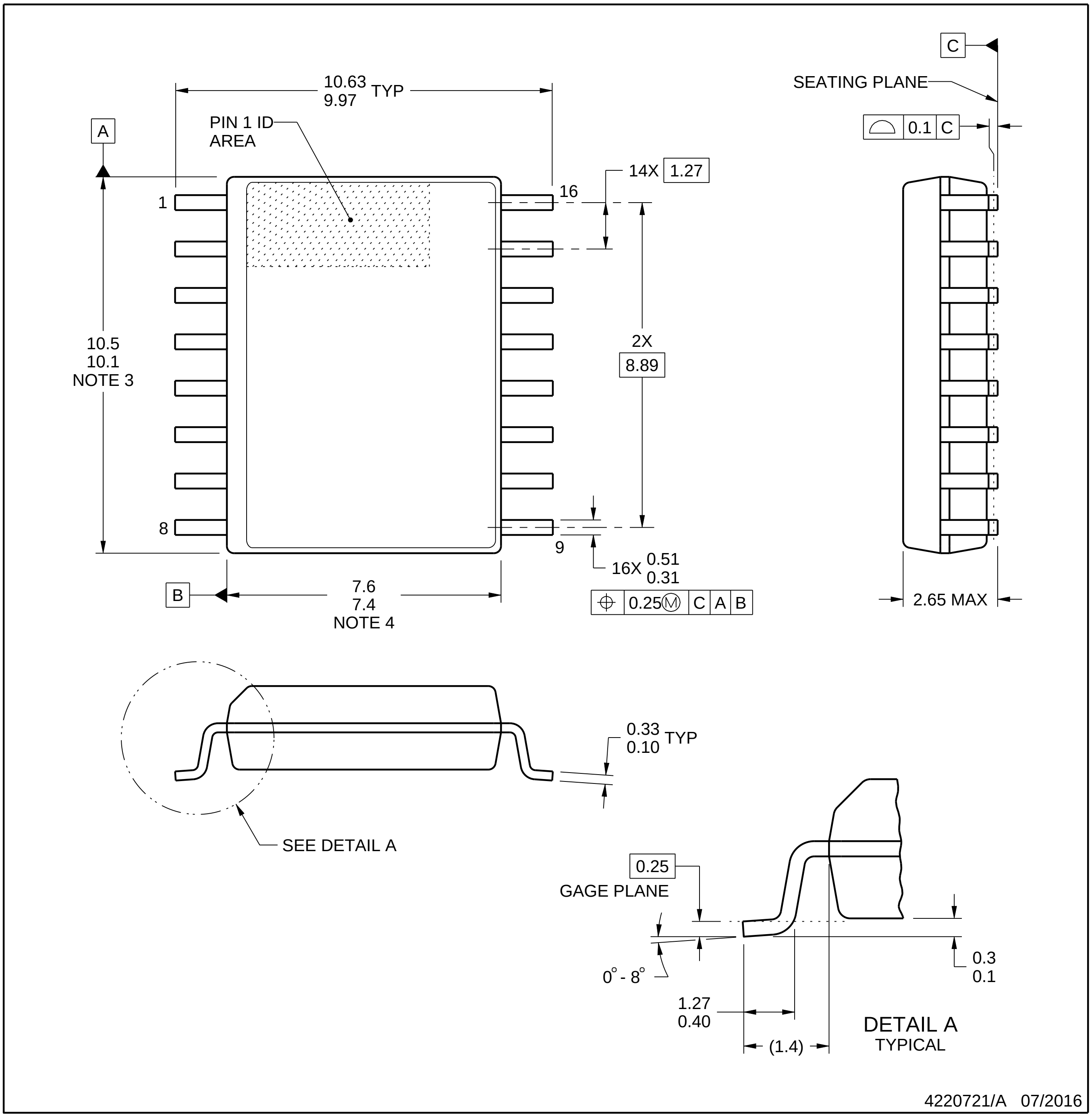
This image is a representation of the package family, actual package may vary.
Refer to the product data sheet for package details.



PACKAGE OUTLINE

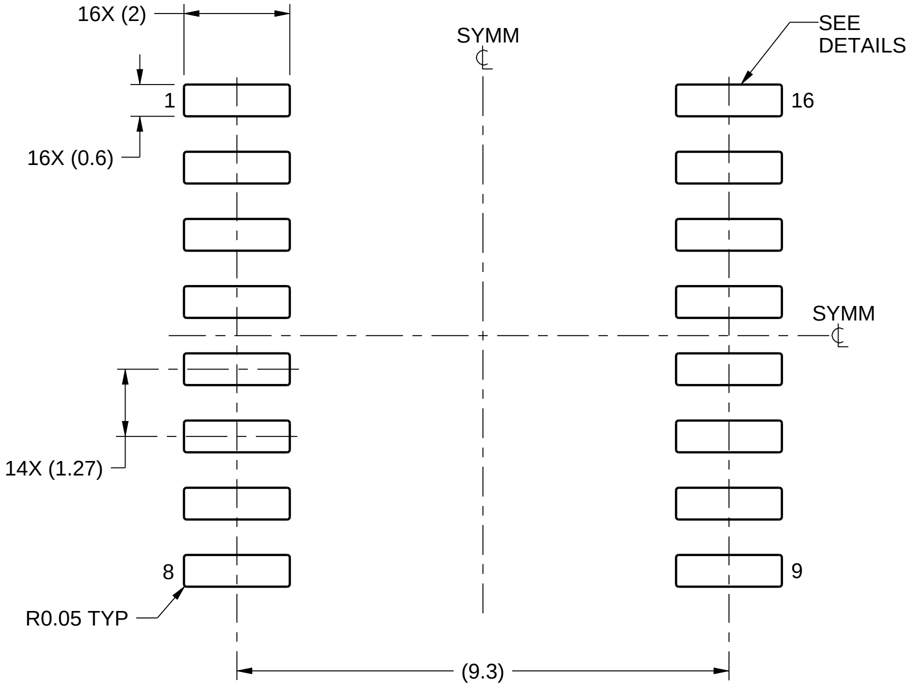
SOIC - 2.65 mm max height

SOIC

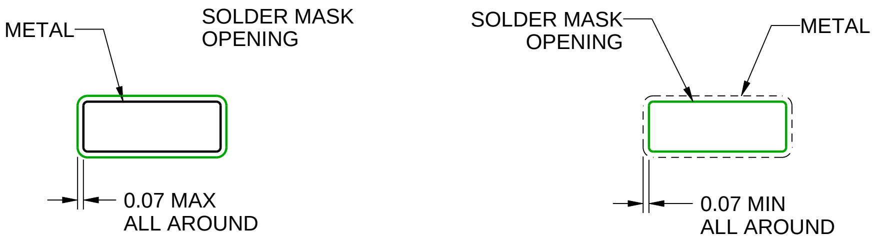


NOTES:

1. All linear dimensions are in millimeters. Dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.15 mm, per side.
4. This dimension does not include interlead flash. Interlead flash shall not exceed 0.25 mm, per side.
5. Reference JEDEC registration MS-013.



LAND PATTERN EXAMPLE
SCALE:7X



NON SOLDER MASK
DEFINED

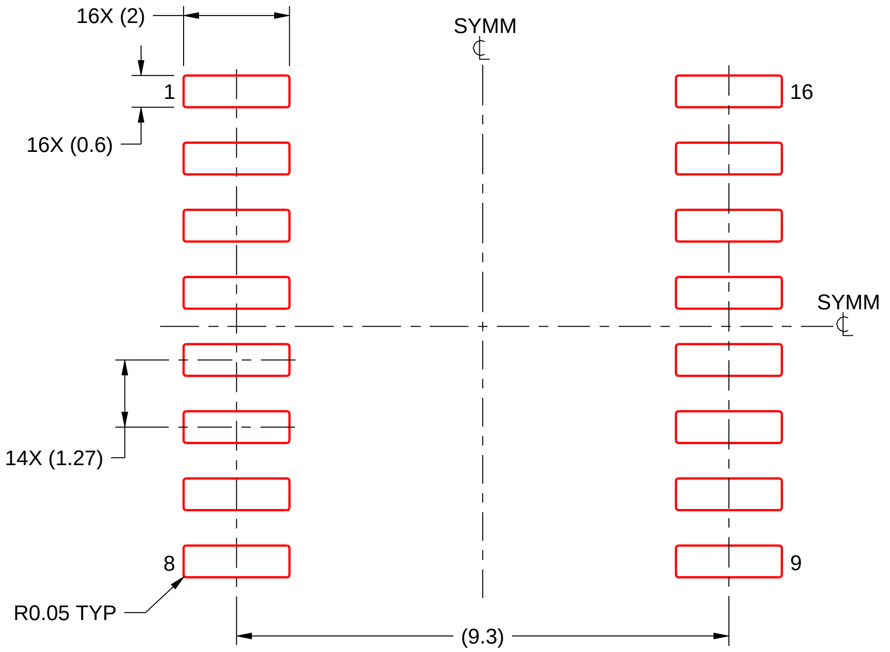
SOLDER MASK
DEFINED

SOLDER MASK DETAILS

4220721/A 07/2016

NOTES: (continued)

6. Publication IPC-7351 may have alternate designs.
7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.



SOLDER PASTE EXAMPLE
BASED ON 0.125 mm THICK STENCIL
SCALE:7X

4220721/A 07/2016

NOTES: (continued)

8. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
9. Board assembly site may have different recommendations for stencil design.

GENERIC PACKAGE VIEW

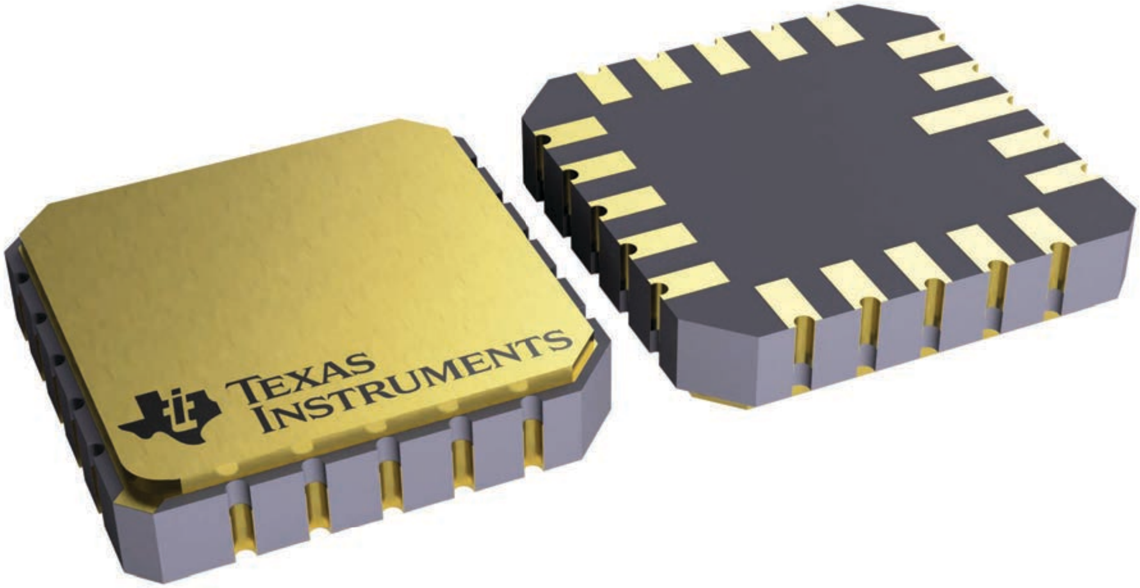
FK 20

LCCC - 2.03 mm max height

8.89 x 8.89, 1.27 mm pitch

LEADLESS CERAMIC CHIP CARRIER

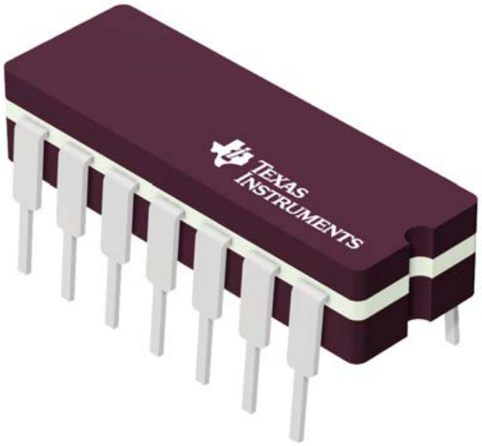
This image is a representation of the package family, actual package may vary.
Refer to the product data sheet for package details.



GENERIC PACKAGE VIEW

J 14 **CDIP - 5.08 mm max height**

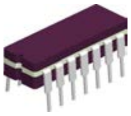
CERAMIC DUAL IN LINE PACKAGE



Images above are just a representation of the package family, actual package may vary.
Refer to the product data sheet for package details.

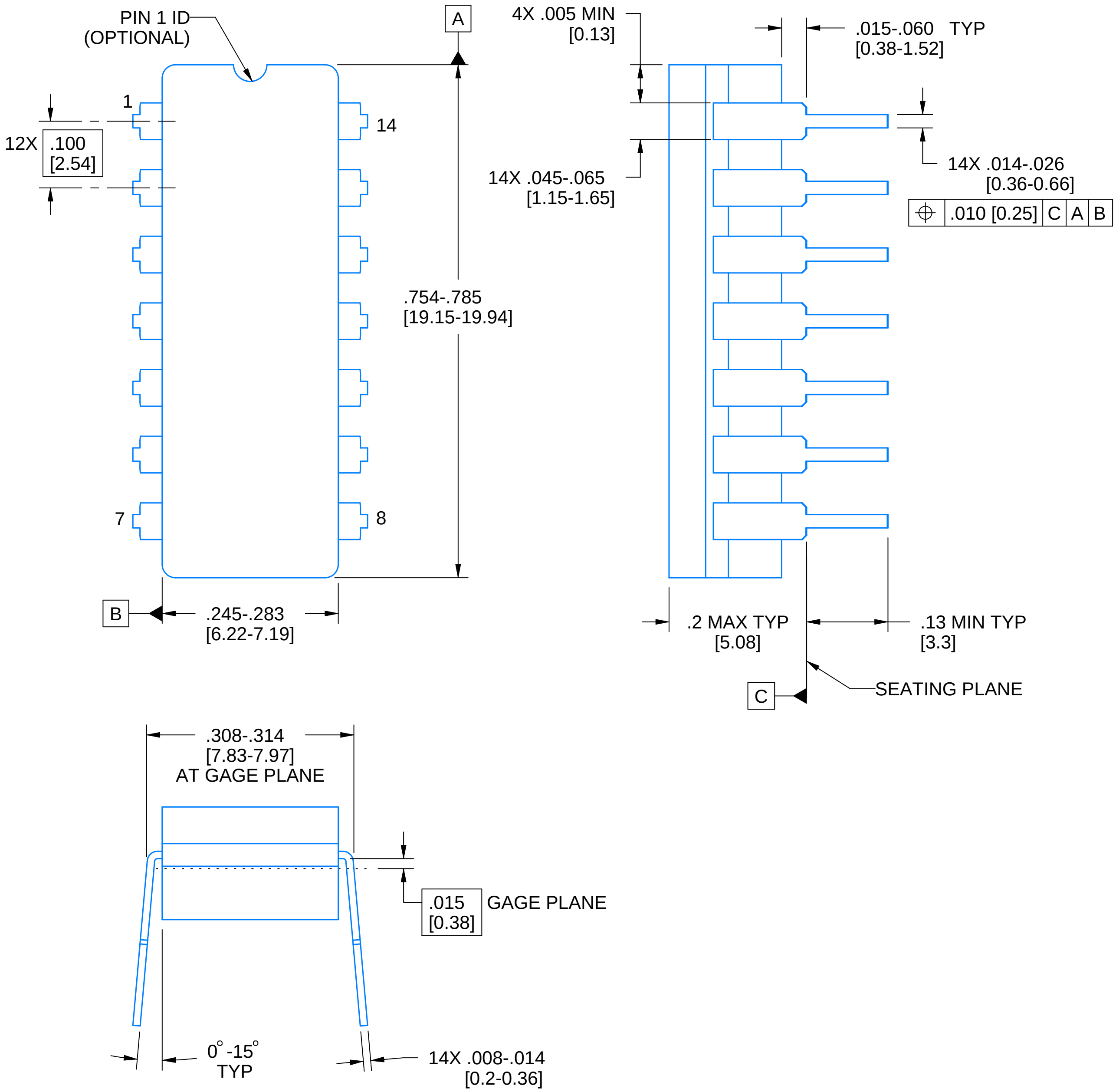
4040083-5/G

J0014A



CDIP - 5.08 mm max height

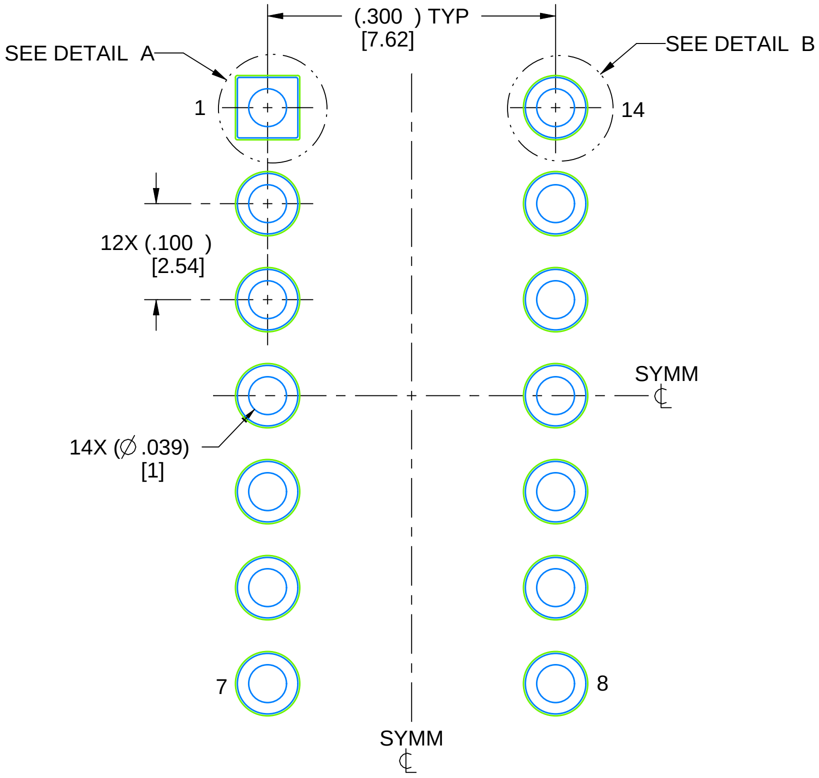
CERAMIC DUAL IN LINE PACKAGE



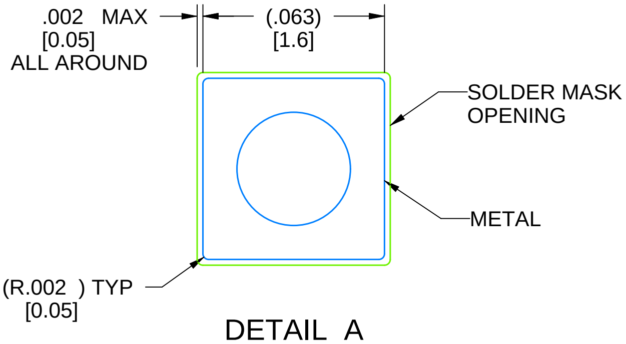
4214771/A 05/2017

NOTES:

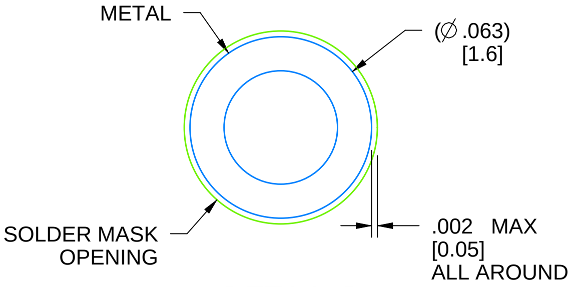
1. All controlling linear dimensions are in inches. Dimensions in brackets are in millimeters. Any dimension in brackets or parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This package is hermitically sealed with a ceramic lid using glass frit.
4. Index point is provided on cap for terminal identification only and on press ceramic glass frit seal only.
5. Falls within MIL-STD-1835 and GDIP1-T14.



LAND PATTERN EXAMPLE
NON-SOLDER MASK DEFINED
SCALE: 5X



DETAIL A
SCALE: 15X



DETAIL B
13X, SCALE: 15X

IMPORTANT NOTICE AND DISCLAIMER

TI PROVIDES TECHNICAL AND RELIABILITY DATA (INCLUDING DATA SHEETS), DESIGN RESOURCES (INCLUDING REFERENCE DESIGNS), APPLICATION OR OTHER DESIGN ADVICE, WEB TOOLS, SAFETY INFORMATION, AND OTHER RESOURCES “AS IS” AND WITH ALL FAULTS, AND DISCLAIMS ALL WARRANTIES, EXPRESS AND IMPLIED, INCLUDING WITHOUT LIMITATION ANY IMPLIED WARRANTIES OF MERCHANTABILITY, FITNESS FOR A PARTICULAR PURPOSE OR NON-INFRINGEMENT OF THIRD PARTY INTELLECTUAL PROPERTY RIGHTS.

These resources are intended for skilled developers designing with TI products. You are solely responsible for (1) selecting the appropriate TI products for your application, (2) designing, validating and testing your application, and (3) ensuring your application meets applicable standards, and any other safety, security, regulatory or other requirements.

These resources are subject to change without notice. TI grants you permission to use these resources only for development of an application that uses the TI products described in the resource. Other reproduction and display of these resources is prohibited. No license is granted to any other TI intellectual property right or to any third party intellectual property right. TI disclaims responsibility for, and you will fully indemnify TI and its representatives against, any claims, damages, costs, losses, and liabilities arising out of your use of these resources.

TI’s products are provided subject to TI’s Terms of Sale or other applicable terms available either on ti.com or provided in conjunction with such TI products. TI’s provision of these resources does not expand or otherwise alter TI’s applicable warranties or warranty disclaimers for TI products.

TI objects to and rejects any additional or different terms you may have proposed.

Mailing Address: Texas Instruments, Post Office Box 655303, Dallas, Texas 75265
Copyright © 2025, Texas Instruments Incorporated