TEXAS INSTRUMENTS

application INFO available

UC1706
UC2706
UC3706

Dual Output Driver

FEATURES

- Dual, 1.5A Totem Pole Outputs
- 40nsec Rise and Fall into 1000pF
- Parallel or Push-Pull Operation
- Single-Ended to Push-Pull Conversion
- High-Speed, Power MOSFET Compatible
- Low Cross-Conduction Current Spike
- Analog, Latched Shutdown
- Internal Deadband Inhibit Circuit
- Low Quiescent Current
- 5 to 40V Operation
- Thermal Shutdown Protection
- 16-Pin Dual-In-Line Package
- 20-Pin Surface Mount Package

DESCRIPTION

The UC1706 family of output drivers are made with a high-speed Schottky process to interface between low-level control functions and high-power switching devices - particularly power MOSFET's. These devices implement three generalized functions as outlined below.

First: They accept a single-ended, low-current digital input of either polarity and process it to activate a pair of high-current, totem pole outputs which can source or sink up to 1.5A each.

Second: They provide an optional single-ended to push-pull conversion through the use of an internal flip-flop driven by double-pulse-suppression logic. With the flip-flop disabled, the outputs work in parallel for 3.0A capability.

Third: Protection functions are also included for pulse-by-pulse current limiting, automatic deadband control, and thermal shutdown.

These devices are available in a two-watt plastic “bat-wing” DIP for operation over a 0°C to 70°C temperature range and, with reduced power, in a hermetically sealed cerdip for -55°C to +125°C operation. Also available in surface mount Q and L packages.

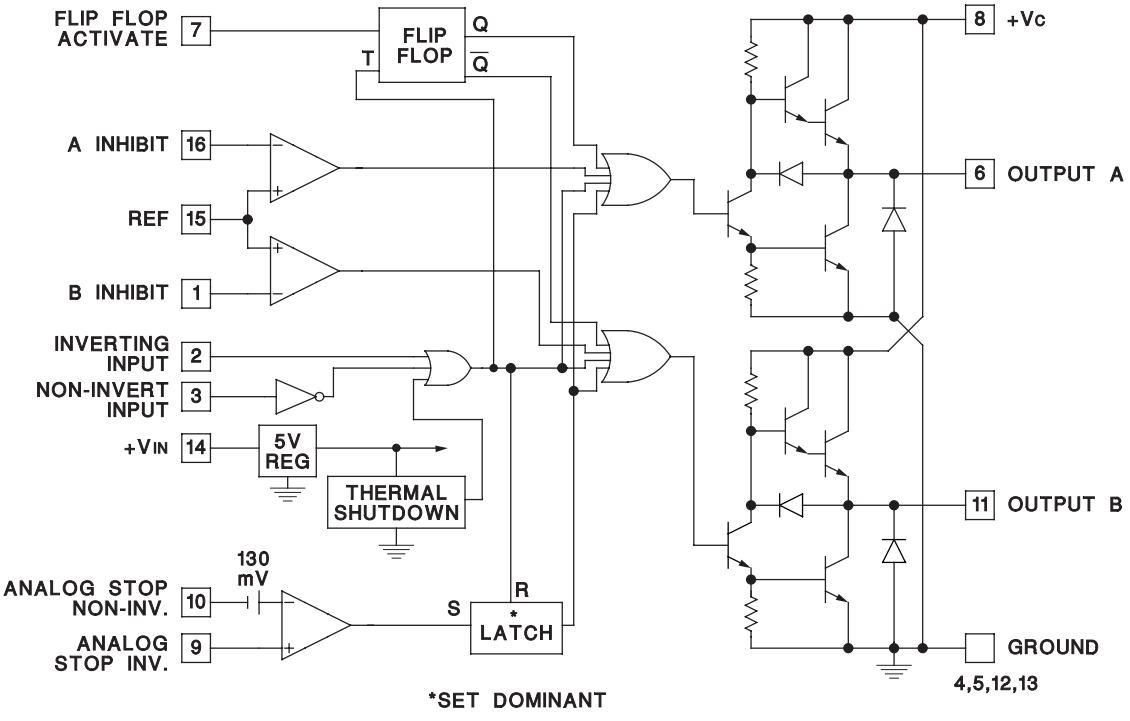
TRUTH TABLE

INV	N.I	OUT
H	H	L
L	H	H
H	L	L
L	L	L

OUT = $\overline{\text{INV}}$ and N.I.

$\overline{\text{OUT}}$ = INV or $\overline{\text{N.I.}}$

BLOCK DIAGRAM



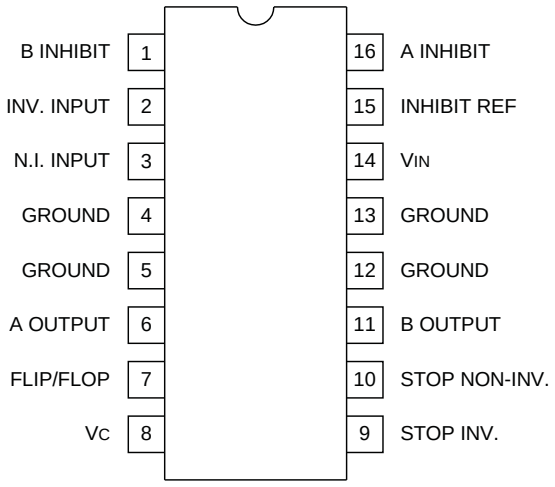
ABSOLUTE MAXIMUM RATINGS

	N--Pkg	J--Pkg
Supply Voltage, V_{IN}	40V	40V
Collector Supply Voltage, V_C	40V	40V
Output Current (Each Output, Source or Sink)		
Steady--State	±500mA	±500mA
Peak Transient	±1.5A	±1.0A
Capacitive Discharge Energy	20µJ	15µJ
Digital Inputs	5.5V	5.5V
Analog Stop Inputs	V_{IN}	V_{IN}
Power Dissipation at T_A = 25°C (See Note)	2W	1W
Power Dissipation at T (Leads/Case) = 25°C (See Note)	5W	2
Operating Temperature Range	--55°C to +125°C	
Storage Temperature Range	--65°C to +150°C	
Lead Temperature (Soldering, 10 Seconds)	300°C	

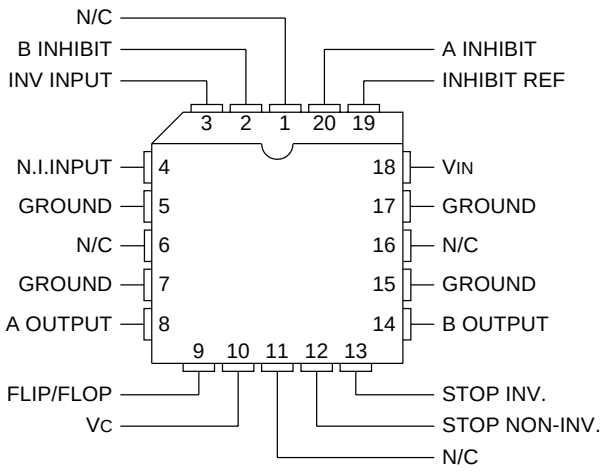
Note: All voltages are with respect to the four ground pins which must be connected together. All currents are positive into, negative out of the specified trerminal. Consult Packaging sections of the Databook for thermal limitations and considerations of package.

CONNECTION DIAGRAMS

DIL-16, SOIC-16 (TOP VIEW)
J or N Package, DW Package



PLCC-20, LCC-20 (TOP VIEW)
Q, L Packages



Note: All four ground pins must be connected to a common ground.

ELECTRICAL CHARACTERISTICS: Unless otherwise stated, these specifications apply for T_A = –55°C to +125°C for the UC1706, –25°C to +85°C for the UC2706 and 0°C to +70°C for the UC3706; V_{IN} = V_C = 20V. T_A = T_J.

PARAMETERS	TEST CONDITIONS	MIN	TYP	MAX	UNITS
V_{IN} Supply Current	V_{IN} = 40V		8	10	mA
V_C Supply Current	V_C = 40V, Outputs Low		4	5	mA
V_C Leakage Current	V_{IN} = 0, V_C = 30V, No Load		.05	0.1	mA
Digital Input Low Level				0.8	V
Digital Input High Level		2.2			V
Input Current	V_I = 0		–0.6	–1.0	mA
Input Leakage	V_I = 5V		.05	0.1	mA

ELECTRICAL CHARACTERISTICS: Unless otherwise stated, these specifications apply for T_A = –55°C to +125°C for the UC1706, –25°C to +85°C for the UC2706 and 0°C to +70°C for the UC3706; V_{IN} = V_C = 20V. T_A = T_J.

PARAMETERS	TEST CONDITIONS	MIN	TYP	MAX	UNITS
Output High Sat., V_C-V_O	I_O = -50mA			2.0	V
Output Low Sat., V_O	I_O = 50mA			0.4	V
	I_O = 500mA			2.5	V
Inhibit Threshold	V_{REF} = 0.5V	0.4		0.6	V
	V_{REF} = 3.5V	3.3		3.7	V
Inhibit Input Current	V_{REF} = 0		–10	–20	µA
Analog Threshold	V_{CM} = 0 to 15V, for the UC2706 and UC3706	100	130	160	mV
	V_{CM} = 0 to 15V, for the UC1706	80	130	160	mV
Input Bias Current	V_{CM} = 0		–10	–20	µA
Thermal Shutdown			155		°C

TYPICAL SWITCHING CHARACTERISTICS: V_{IN} = V_C = 20V, T_A = 25°C. Delays measured to 10% output change.

PARAMETERS	TEST CONDITIONS	OUTPUT C_L =			UNITS
From Inv. Input to Output:		open	1.0	2.2	nF
Rise Time Delay		110	130	140	ns
10% to 90% Rise		20	40	60	ns
Fall Time Delay		80	90	110	ns
90% to 10% Fall		25	30	50	ns
From N. I. Input to Output:					
Rise Time Delay		120	130	140	ns
10% to 90% Rise		20	40	60	ns
Fall Time Delay		100	120	130	ns
90% to 10% Fall		25	30	50	ns
V_C Cross-Conduction Current Spike Duration	Output Rise	25			ns
	Output Fall	0			ns
Inhibit Delay	Inhibit Ref. = 1V, Inhibit Inv. = 0.5 to 1.5V	250			ns
Analog Shutdown Delay	Stop Non-Inv. = 0V, Stop Inv. = 0 to 0.5V	180			ns

CIRCUIT DESCRIPTION

Outputs

The totem-pole outputs have been designed to minimize cross-conduction current spikes while maximizing fast, high-current rise and fall times. Current limiting can be done externally either at the outputs or at the common V_C pin. The output diodes included have slow recovery and should be shunted with high-speed external diodes when driving high-frequency inductive loads.

Flip/Flop

Grounding pin 7 activates the internal flip-flop to alternate the two outputs. With pin 7 open, the two outputs operate simultaneously and can be paralleled for higher current operation. Since the flip-flop is triggered by the digital input, an off-time of at last 200nsec must be provided to allow the flip/flop to change states. Note that the circuit logic is configured such that the “OFF” state is defined as the outputs low.

Digital Inputs

With both an inverting and non-inverting input available, either active-high or active-low signals may be accepted. These are true TTL compatible inputs—the threshold is approximately 1.2V with no hysteresis; and external pull-up resistors are not required.

Inhibit Circuit

Although it may have other uses, this circuit is included to eliminate the need for deadband control when driving relatively slow bipolar power transistors. A diode from each inhibit input to the opposite power switch collector will keep one output from turning-on until the other has turned-off. The threshold is determined by the voltage on pin 15 which can be set from 0.5 to 3.5V. When this circuit is not used, ground pin 15 and leave 1 and 16 open.

CIRCUIT DESCRIPTION (cont.)

Analog Shutdown

This circuit is included to get a latched shutdown as close to the outputs as possible, from a time standpoint. With an internal 130mV threshold, this comparator has a common-mode range from ground to (V_{IN} – 3V). When not used, both inputs should be grounded. The time required for this circuit to latch is inversely proportional to the amount of overdrive but reaches a minimum of 180nsec. As with the flip-flop, an input off-time of at least 200nsec is required to reset the latch between pulses.

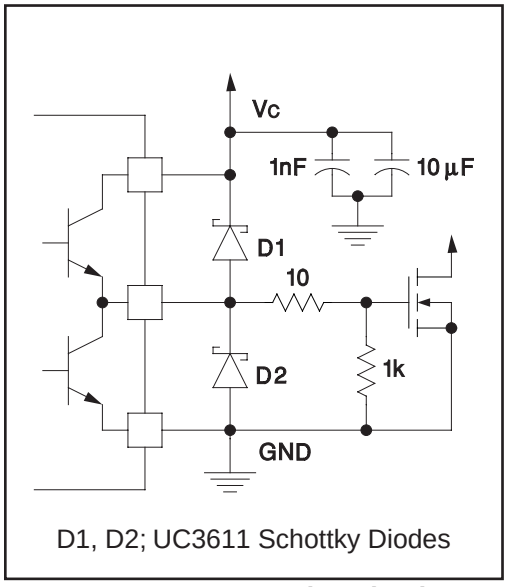
Supply Voltage

With an internal 5V regulator, this circuit is optimized for use with a 7 to 40V supply; however, with some slight response time degradation, it can also be driven from 5V. When V_{IN} is low, the entire circuit is disabled and no current is drawn from V_C. When combined with a UC1840 PWM, the Driver Bias switch can be used to supply V_{IN} to the UC1706. V_{IN} switching should be fast as if V_C is high, undefined operation of the outputs may occur with V_{IN} less than 5V.

Thermal Considerations

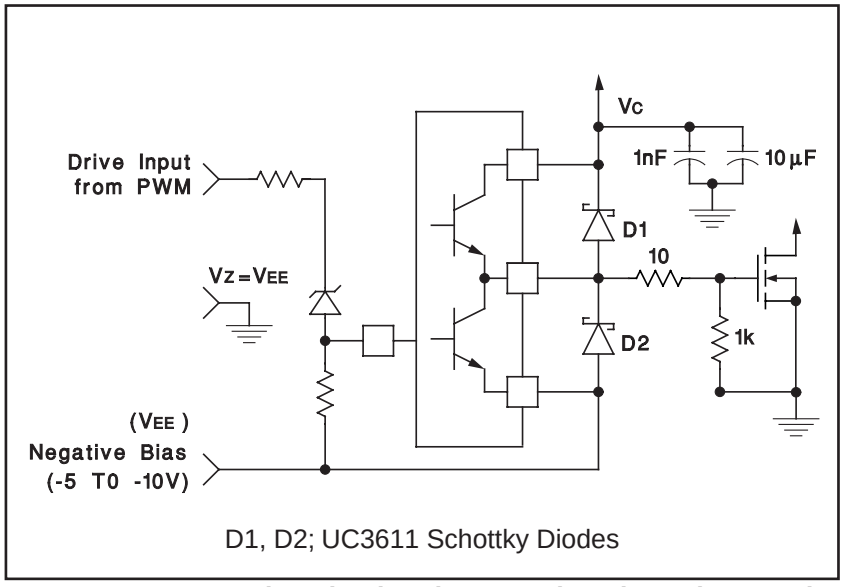
Should the chip temperature reach approximately 155°C, a parallel, non--inverting input is activated driving both outputs to the low state.

APPLICATIONS



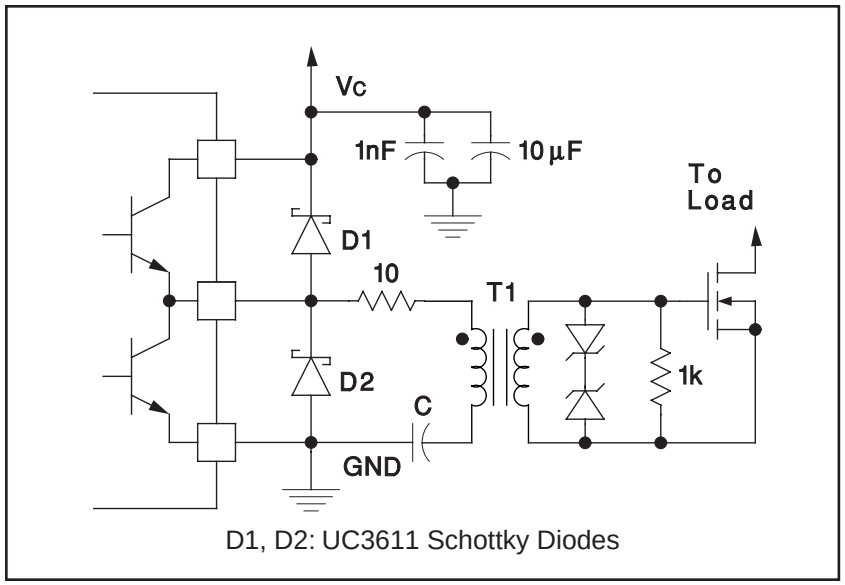
D1, D2; UC3611 Schottky Diodes

Power MOSFET Drive Circuit



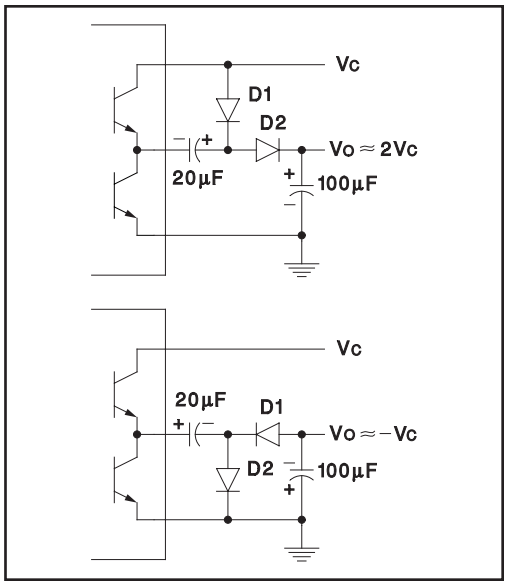
D1, D2; UC3611 Schottky Diodes

Power MOSFET Drive Circuit Using Negative Bias Voltage and Level Shifting to Ground Referenced PWMs



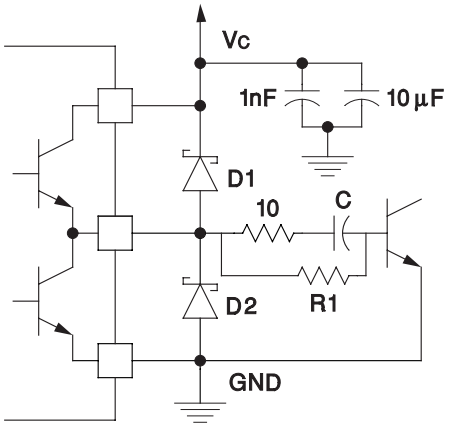
D1, D2: UC3611 Schottky Diodes

Transformer Coupled MOSFET Drive Circuit



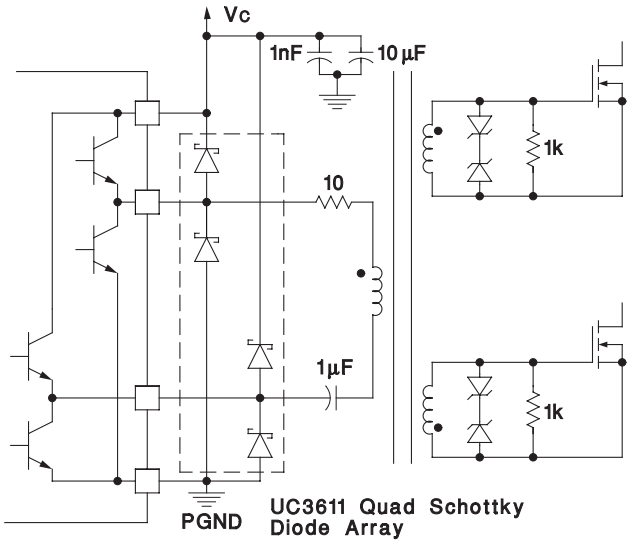
Charge Pump Circuits

APPLICATIONS (cont'd)



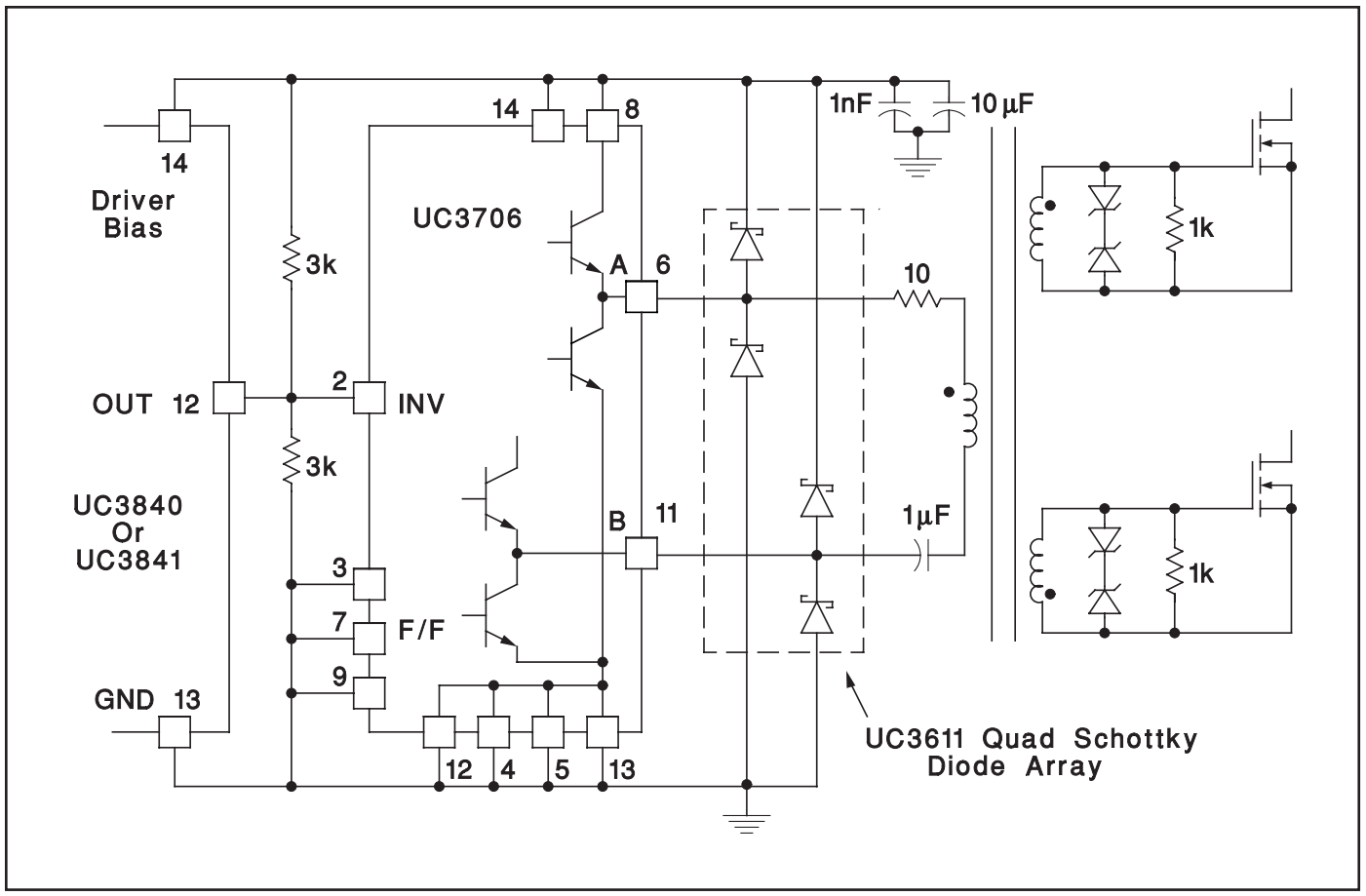
D1, D2: UC3611 Schottky Diodes

Power Bipolar Drive Circuit



D1, D2: UC3611 Schottky Diodes

Transformer Coupled Push-Pull MOSFET Drive Circuit



UC3706 Converts Single Output PWMs to High Current Push-Pull Configuration

UNITRODE CORPORATION
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PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead finish/ Ball material (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
5962-89611012A	ACTIVE	LCCC	FK	20	55	Non-RoHS & Green	SNPB	N / A for Pkg Type	-55 to 125	5962-89611012A	Samples
5962-8961101EA	ACTIVE	CDIP	J	16	25	Non-RoHS & Green	SNPB	N / A for Pkg Type	-55 to 125	5962-8961101EA	Samples
UC1706J	ACTIVE	CDIP	J	16	25	Non-RoHS & Green	SNPB	N / A for Pkg Type	-55 to 125	UC1706J	Samples
UC1706J883B	ACTIVE	CDIP	J	16	25	Non-RoHS & Green	SNPB	N / A for Pkg Type	-55 to 125	UC1706J/883B	Samples
UC1706L	ACTIVE	LCCC	FK	20	55	Non-RoHS & Green	SNPB	N / A for Pkg Type	-55 to 125	UC1706L	Samples
UC2706DW	ACTIVE	SOIC	DW	16	40	RoHS & Green	NIPDAU	Level-2-260C-1 YEAR	-40 to 85	UC2706DW	Samples
UC2706J	ACTIVE	CDIP	J	16	25	Non-RoHS & Green	SNPB	N / A for Pkg Type	-40 to 85	UC2706J	Samples
UC2706N	ACTIVE	PDIP	N	16	25	RoHS & Green	NIPDAU	N / A for Pkg Type	-40 to 85	UC2706N	Samples
UC3706DW	ACTIVE	SOIC	DW	16	40	RoHS & Green	NIPDAU	Level-2-260C-1 YEAR	0 to 70	UC3706DW	Samples
UC3706DWTR	ACTIVE	SOIC	DW	16	2000	RoHS & Green	NIPDAU	Level-2-260C-1 YEAR	0 to 70	UC3706DW	Samples
UC3706N	ACTIVE	PDIP	N	16	25	RoHS & Green	NIPDAU	N / A for Pkg Type	0 to 70	UC3706N	Samples
UC3706NG4	ACTIVE	PDIP	N	16	25	RoHS & Green	NIPDAU	N / A for Pkg Type	0 to 70	UC3706N	Samples

(1) The marketing status values are defined as follows:
ACTIVE: Product device recommended for new designs.
LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
PREVIEW: Device has been announced but is not in production. Samples may or may not be available.
OBSOLETE: TI has discontinued the production of the device.

(2) **RoHS:** TI defines "RoHS" to mean semiconductor products that are compliant with the current EU RoHS requirements for all 10 RoHS substances, including the requirement that RoHS substance do not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, "RoHS" products are suitable for use in specified lead-free processes. TI may reference these types of products as "Pb-Free".
RoHS Exempt: TI defines "RoHS Exempt" to mean products that contain lead but are compliant with EU RoHS pursuant to a specific EU RoHS exemption.

Green: TI defines "Green" to mean the content of Chlorine (Cl) and Bromine (Br) based flame retardants meet JS709B low halogen requirements of <=1000ppm threshold. Antimony trioxide based flame retardants must also meet the <=1000ppm threshold requirement.

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

(6) Lead finish/Ball material - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

OTHER QUALIFIED VERSIONS OF UC1706, UC2706, UC2706M, UC3706 :

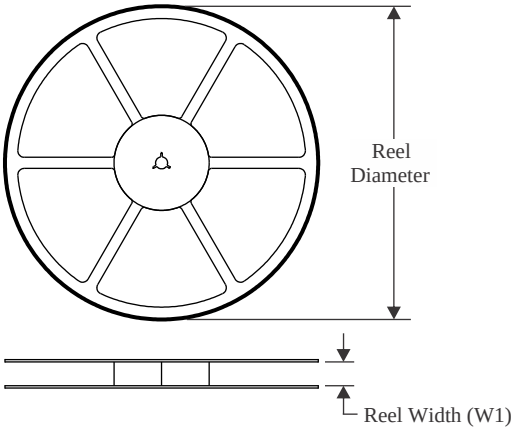
- Catalog : UC3706, UC2706
- Military : UC2706M, UC1706

NOTE: Qualified Version Definitions:

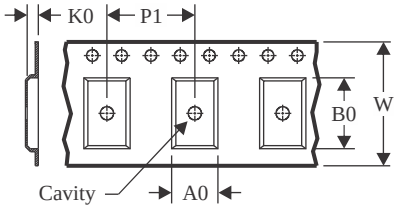
- Catalog - TI's standard catalog product
- Military - QML certified for Military and Defense Applications

TAPE AND REEL INFORMATION

REEL DIMENSIONS

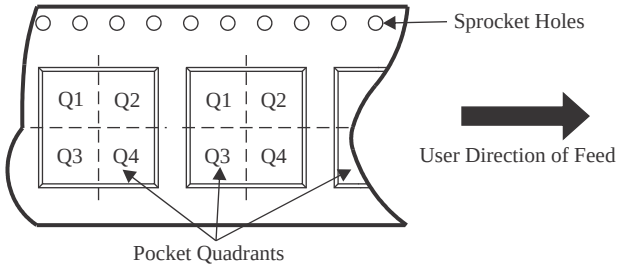


TAPE DIMENSIONS



A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

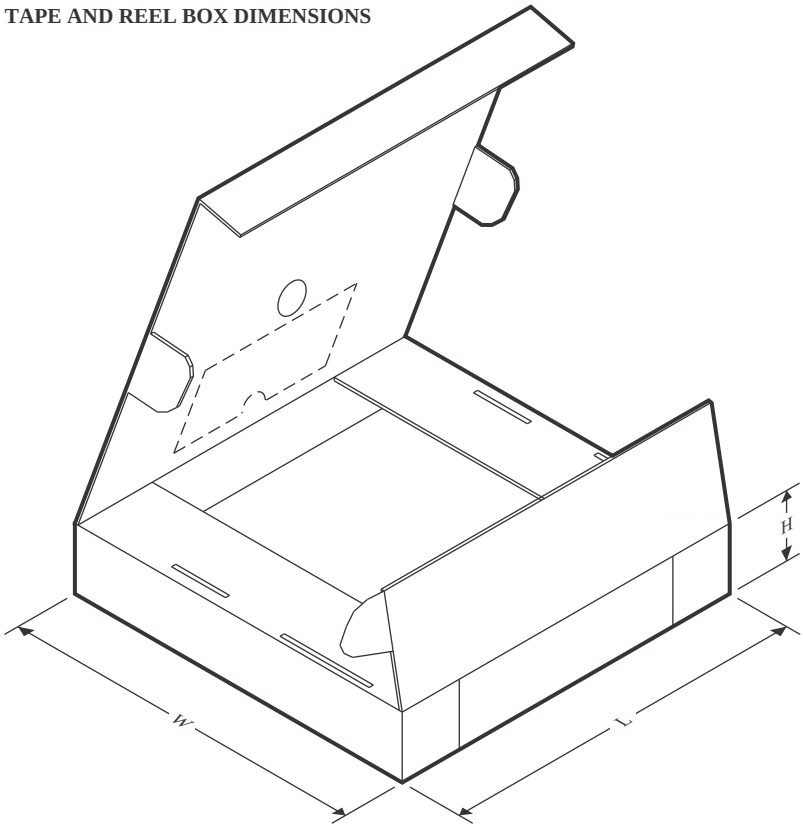
QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
UC3706DWTR	SOIC	DW	16	2000	330.0	16.4	10.75	10.7	2.7	12.0	16.0	Q1

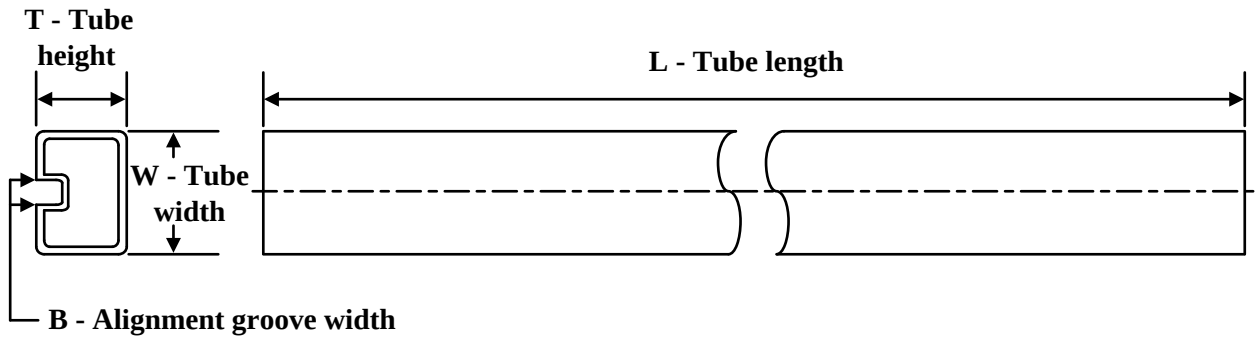
TAPE AND REEL BOX DIMENSIONS



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
UC3706DWTR	SOIC	DW	16	2000	356.0	356.0	35.0

TUBE



*All dimensions are nominal

Device	Package Name	Package Type	Pins	SPQ	L (mm)	W (mm)	T (µm)	B (mm)
5962-89611012A	FK	LCCC	20	55	506.98	12.06	2030	NA
UC1706L	FK	LCCC	20	55	506.98	12.06	2030	NA
UC2706DW	DW	SOIC	16	40	507	12.83	5080	6.6
UC2706N	N	PDIP	16	25	506	13.97	11230	4.32
UC3706DW	DW	SOIC	16	40	507	12.83	5080	6.6
UC3706N	N	PDIP	16	25	506	13.97	11230	4.32
UC3706NG4	N	PDIP	16	25	506	13.97	11230	4.32

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