UC2802x Economy High-Speed PWM Controller

1 Features

- Peak Current Mode, Average Current Mode, or Voltage Mode (With FeedForward) Control Methods
- Practical Operation Up to 1 MHz
- 50-ns Propagation Delay to Output
- ±1.5-A Peak Totem Pole Outputs
- 9-V to 30-V Nominal Operational Voltage
- Wide Bandwidth Error Amplifier
- Fully Latched Logic With Double Pulse Suppression
- Pulse-by-Pulse Current Limiting
- Programmable Maximum Duty Cycle Control
- Undervoltage Lockout With Hysteresis
- Trimmed 5.1-V Reference With UVLO
- Same Functionality as UC3823 and UC3825

2 Applications

- Off-Line and DC-DC Power Supplies
- Converters Using Voltage Mode, Peak Current Mode, or Average Current Mode Control Methods
- Single-Ended or Two-Switch Topology Designs

3 Description

The UC28023 and UC28025 are fixed-frequency PWM controllers optimized for high-frequency switched-mode power-supply applications. The UC28023 is a single output PWM for single-ended topologies while the UC28025 offers dual alternating outputs for double-ended and full bridge topologies.

Targeted for cost-effective solutions with minimal external components. UC2802x devices include an oscillator, a temperature compensated reference, a wide bandwidth error amplifier, a high-speed current-sense comparator, and high-current, active-high, totem-pole outputs to directly drive external MOSFETs.

Protection circuitry includes a current limit comparator with a 1-V threshold, a TTL compatible shutdown port, and a soft-start pin which doubles as a maximum duty-cycle clamp. The logic is fully latched to provide jitter-free operation and prohibit multiple pulses at an output. An undervoltage lockout section with 800 mV of hysteresis assures low start-up current. During undervoltage lockout, the outputs are high impedance. Propagation delays through the comparators and logic circuitry have been minimized while maximizing bandwidth and slew rate of the error amplifier.

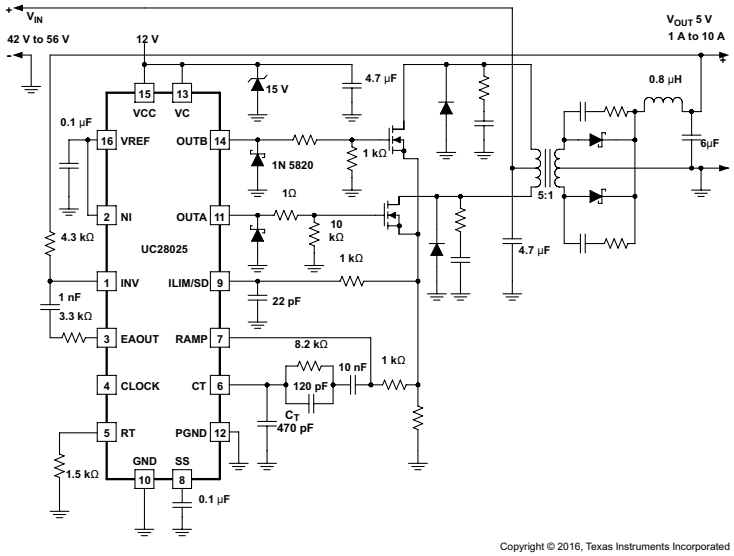
Devices are available in the industrial temperature range of –40°C to 105°C. Package offerings are 16-pin SOIC (DW), or 16-pin PDIP (N) packages.

Device Information(1)

PART NUMBER	PACKAGE	BODY SIZE (NOM)
UC2802x	SOIC (16)	10.30 mm × 7.50 mm
	PDIP (16)	19.30 mm × 6.35 mm

(1) For all available packages, see the orderable addendum at the end of the data sheet.

Typical Application Schematic



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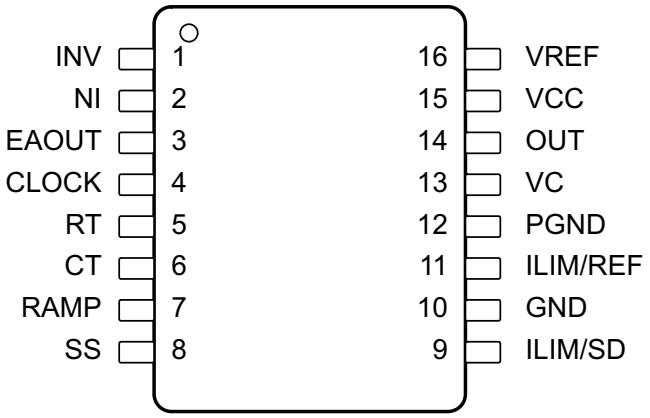
4 Revision History

NOTE: Page numbers for previous revisions may differ from page numbers in the current version.

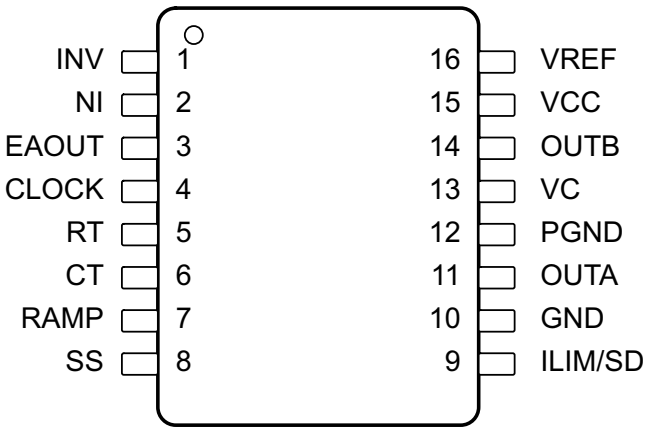
Changes from Revision F (August 2010) to Revision G	Page
• Added *Device Information* table, *Pin Configuration and Functions* section, *Specifications* section, *ESD Ratings* table, *Recommended Operating Conditions* table, *Switching Characteristics* table, *Typical Characteristics* section, *Detailed Description* section, *Application and Implementation* section, *Power Supply Recommendations* section, *Layout* section, *Device and Documentation Support* section, and *Mechanical, Packaging, and Orderable Information* section	1
• Deleted *Ordering Information* table; see POA at the end of the data sheet	1
• Moved Delay to output time parameters from *Electrical Characteristics* to *Switching Characteristics*	1
• Moved rise and fall time parameters from *Electrical Characteristics* to *Switching Characteristics*	1
• Deleted Lead temperature soldering rating in the *Absolute Maximum Ratings* table	4
• Added *Thermal Information* table	4
• Changed $R_{\theta JA}$ values for DW (SOIC) package From: 50°C/W to 100°C/W To: 70.5°C/W and for N (PDIP) package From: 90°C/W To: 44.5°C/W	4
• Changed $R_{\theta JC(top)}$ values for DW (SOIC) package From: 27°C/W To: 31.8°C/W and for N (PDIP) package From: 45°C/W To: 34.3°C/W	4

5 Pin Configuration and Functions

UC28023 DW or N Packages
16-Pin SOIC or PDIP
Top View



UC28025 DW or N Packages
16-Pin SOIC or PDIP
Top View



Pin Functions

PIN			I/O	DESCRIPTION
NAME	UC28023	UC28025		
CLOCK	4	4	O	Output of the internal oscillator
CT	6	6	I	Timing capacitor connection pin for oscillator frequency programming. The timing capacitor must be connected to the device ground using minimal trace length.
EAOUT	3	3	O	Output of the error amplifier for compensation
GND	10	10	—	Analog ground return pin.
ILIM/REF	11	—	I	Pin to set the current limit threshold externally.
ILIM/SD	9	9	I	Input to the current limit comparator and the shutdown comparator.
INV	1	1	I	Inverting input to the error amplifier
NI	2	2	I	Noninverting input to the error amplifier
OUT	14	—	O	High current totem pole output of the on-chip drive stage.
OUTA	—	11	O	High current totem pole output A of the on-chip drive stage.
OUTB	—	14	O	High current totem pole output B of the on-chip drive stage
PGND	12	12	—	Ground return pin for the output driver stage
RAMP	7	7	I	Noninverting input to the PWM comparator with 1.25-V internal input offset. In voltage mode operation this serves as the input voltage feedforward function by using the CT ramp. In peak current mode operation, this serves as the slope compensation input.
RT	5	5	I	Timing resistor connection pin for oscillator frequency programming
SS	8	8	I	Soft-start input pin.
VC	13	13	—	Power supply pin for the output stage. This pin must be bypassed with a 0.1-µF monolithic ceramic low ESL capacitor with minimal trace lengths.
VCC	15	15	—	Power supply pin for the device. This pin must be bypassed with a 0.1-µF monolithic ceramic low ESL capacitor with minimal trace lengths
VREF	16	16	O	5.1-V reference. For stability, the reference must be bypassed with a 0.1-µF monolithic ceramic low ESL capacitor and minimal trace length to the ground plane.

6 Specifications

6.1 Absolute Maximum Ratings

over operating free-air temperature range (unless otherwise noted)(1)(2)

			MIN	MAX	UNIT
	Input voltage	VC, VCC		30	V
	Analog inputs	INV, NI, RAMP	–0.3	7	V
		SS, ILIM/SD	V_{REF} – 0.3	V_{REF} + 0.3	
$I_{OUT(DC)}$	Output current	OUT (UC28023), OUTB (UC28025)		±0.5	A
	Peak output current, pulsed 0.5 ms (I_{OUT} pulsed)	OUT (UC28023), OUTB (UC28025)		±2	A
I_{REF}	Output current	VREF		10	mA
I_{CLOCK}	Output current	CLOCK		–5	mA
I_{SINK_SS}	Soft-start sink current	SS		5	mA
$I_{OUT(EA)}$	Output current	EAOUT		20	mA
I_{OSC_CHG}	Oscillator charging current	RT		–5	mA
C_{LOAD}	Capacitive load			200	pF
	Power Dissipation at T_A = 25°C (all packages)			1	W
T_J	Operating junction temperature		–55	150	°C
T_{stg}	Storage temperature		–65	150	°C

(1) Stresses beyond those listed under *Absolute Maximum Ratings* may cause permanent damage to the device. These are stress ratings only, which do not imply functional operation of the device at these or any other conditions beyond those indicated under *Recommended Operating Conditions*. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
(2) All voltages are with respect to GND. All currents are positive into and negative out of the specified terminal.

6.2 ESD Ratings

			VALUE	UNIT
$V_{(ESD)}$	Electrostatic discharge	Human-body model (HBM), per ANSI/ESDA/JEDEC JS-001(1)	±3000	V
		Charged-device model (CDM), per JEDEC specification JESD22-C101(2)	±1500	

(1) JEDEC document JEP155 states that 500-V HBM allows safe manufacturing with a standard ESD control process.
(2) JEDEC document JEP157 states that 250-V CDM allows safe manufacturing with a standard ESD control process.

6.3 Recommended Operating Conditions

over operating free-air temperature range (unless otherwise noted)

	MIN	NOM	MAX	UNIT
VCC input voltage from a low-impedance source		12		V
Operating temperature	–40		105	°C

6.4 Thermal Information

THERMAL METRIC(1)		UC2802x		UNIT
		DW (SOIC)	N (PDIP)	
		16 PINS	16 PINS	
$R_{\theta JA}$	Junction-to-ambient thermal resistance	70.5	44.5	°C/W
$R_{\theta JC(top)}$	Junction-to-case (top) thermal resistance	31.8	34.3	°C/W
$R_{\theta JB}$	Junction-to-board thermal resistance	35.2	24.6	°C/W
ψ_{JT}	Junction-to-top characterization parameter	7.7	14.7	°C/W
ψ_{JB}	Junction-to-board characterization parameter	34.7	24.4	°C/W

(1) For more information about traditional and new thermal metrics, see the *Semiconductor and IC Package Thermal Metrics* application report.

6.5 Electrical Characteristics

T_A = –40°C to 105°C, $T_J = T_A$, R_T = 3.65 kΩ, C_T = 1 nF, V_{CC} = 15 V (unless otherwise noted)

PARAMETER			TEST CONDITIONS	MIN	TYP	MAX	UNIT
REFERENCE							
V_{REF}	Reference voltage		T_J = 25°C, I_{REF} = 1 mA	5.05	5.1	5.15	V
	Line regulation voltage		V_{CC} = 10 V to 30 V		2	15	mV
	Load regulation voltage		I_{REF} = 1 mA to 10 mA		5	15	mV
	Temperature stability(1)		T_A = –40°C to 105°C		0.2	0.4	mV/°C
	Total output voltage variation(1)		Line and load temperature	4.95		5.25	V
	Output noise voltage(1)		f = 10 Hz to 10 kHz		50		μV
	Long-term stability voltage(1)		T_J = 125°C, 1000 hours		5	25	mV
I_{SS}	Short-circuit current		V_{REF} = 0 V	–20	–50	–100	mA
OSCILLATOR							
f_{OSC}	Initial accuracy(1)		T_J = 25°C	360	400	440	kHz
	Voltage stability(1)		V_{CC} =10 V to 30 V		0.2%	2%	
	Temperature stability(1)		T_A = –40°C to 105°C		5%		
	Total voltage variation(1)		Line temperature	340		460	kHz
V_{CLOCK_H}	High-level clock output voltage			3.9	4.5		V
V_{CLOCK_L}	Low-level clock output voltage				2.3	2.9	V
$V_{RAMP(P)}$	Ramp peak voltage(1)			2.6	2.8	3	V
$V_{RAMP(V)}$	Ramp valley voltage(1)			0.7	1	1.25	V
$V_{RAMP(VP)}$	Ramp valley-to-peak voltage(1)			1.6	1.8	2	V
ERROR AMPLIFIER							
V_{IN}	Input offset voltage					15	mV
I_{BIAS}	Input bias current				0.6	3	μA
I_{IN}	Input offset current				0.1	1	μA
A_{VOL}	Open-loop gain		V_{OUT} = 1 V to 4 V	60	95		dB
CMRR	Common-mode rejection ratio		V_{CM} = 1.5 V to 5.5 V	75	95		dB
PSRR	Power supply rejection ratio		V_{CC} = 10 V to 30 V	85	110		dB
$I_{OUT(SINK)}$	Output sink current		$V_{(EAOUT)}$ = 1 V	1	2.5		mA
$I_{OUT(SRC)}$	Output source current		$V_{(EAOUT)}$ = 4 V	–0.5	–1.3		mA
V_{OH}	High-level output voltage		$I_{(EAOUT)}$ = –0.5 V	4	4.7	5	V
V_{OL}	Low-level output voltage		$I_{(EAOUT)}$ = 1 mA	0	0.5	1	V
	Unity gain bandwidth(1)			3	5.5		MHz
	Slew rate(1)			6	12		V/μs
PWM COMPARATOR							
I_{BIAS_RAMP}	RAMP bias current		V_{RAMP} = 0 V		–1	–5	μA
	Maximum duty cycle	UC28023		80%	90%		
		UC28025	See (2)	40%	45%		
	Minimum duty cycle	UC28023				0%	
		UC28025				0%	
	EAOUT zero DC threshold		V_{RAMP} = 0 V	1.1	1.25	1.4	V
SOFT START							
I_{CHG}	Charge current		V_{SS} = 0.5 V	3	9	20	μA
I_{DISCHG}	Discharge current		V_{SS} = 1 V	1	7.5		mA

(1) Specified by design. Not production tested.
(2) Tested as 80% minimum for the oscillator which is the equivalent of 40% for UC28025.

Electrical Characteristics (continued)

T_A = –40°C to 105°C, $T_J = T_A$, R_T = 3.65 kΩ, C_T = 1 nF, V_{CC} = 15 V (unless otherwise noted)

PARAMETER			TEST CONDITIONS	MIN	TYP	MAX	UNIT
CURRENT LIMIT AND SHUTDOWN							
I_{LIMIT}	Current limit bias current		$V_{ILIM/SD}$ = 0 V to 4 V			±10	µA
I_{LIMIT}	Offset voltage	UC28023				15	mV
$I_{LIMITREF}$	Common mode(1)	UC28023		1		1.25	V
	Current limit threshold voltage	UC28025		0.9	1	1.1	V
	Shutdown threshold voltage			1.25	1.4	1.55	V
OUTPUT							
V_{OL}	Low-level output voltage		I_{OUT} = 20 mA		0.25	0.4	V
			I_{OUT} = 200 mA		1.2	2.2	
V_{OH}	High-level output voltage		I_{OUT} = –20 mA	13	13.5		V
			I_{OUT} = –200 mA	12	13		
	Collector leakage		V_C = 30 V	100	500		µA
UNDERVOLTAGE LOCKOUT (UVLO)							
	Start threshold voltage			8.8	9.2	9.6	V
	Hysteresis			0.4	0.8	1.2	V
SUPPLY CURRENT							
	Start-up current		V_{CC} = 8 V		1.1	2	mA
I_{CC}	Operating current		$V_{INV} = V_{RAMP} = V_{ILIM}$ = 0 V, V_{NI} = 1 V		25	35	mA

6.6 Switching Characteristics

over operating free-air temperature range (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
t_{DELAY}	Delay to output time(1)	PWM comparator		50	100	ns
		Current limit and shutdown		50	80	ns
	Rise time and Fall time(1)	C_{LOAD} = 1 nF	30	60		ns

(1) Specified by design. Not production tested.

6.7 Typical Characteristics

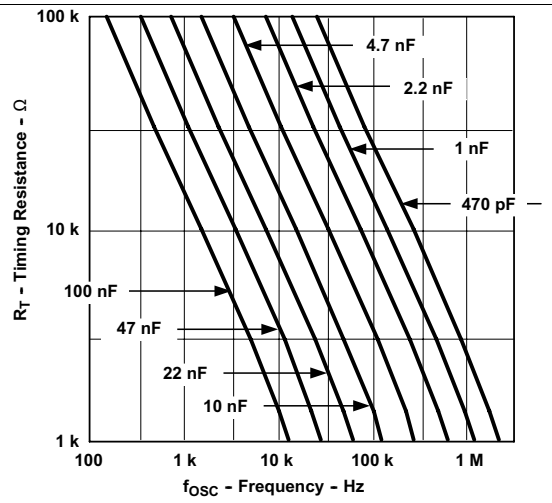


Figure 1. Timing Resistance vs Frequency

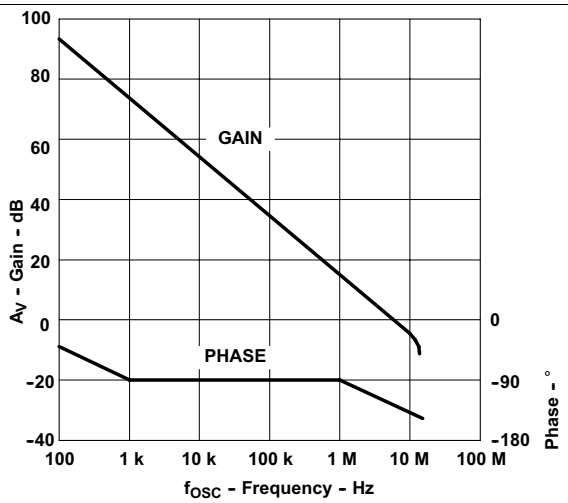


Figure 2. Open-Loop Frequency Response

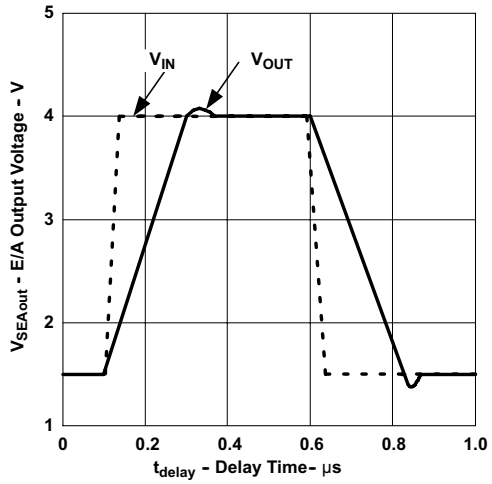


Figure 3. Unity Gain Slew Rate

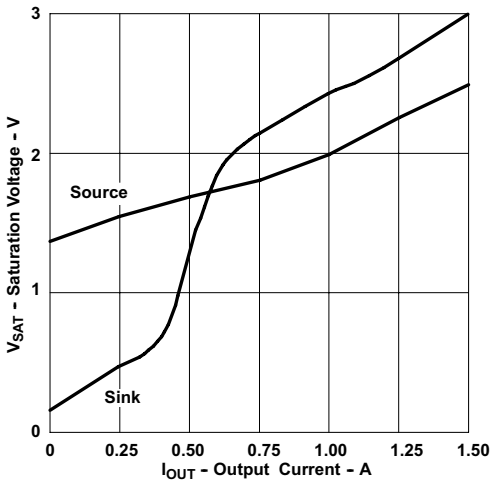


Figure 4. Saturation Voltage vs Output Current

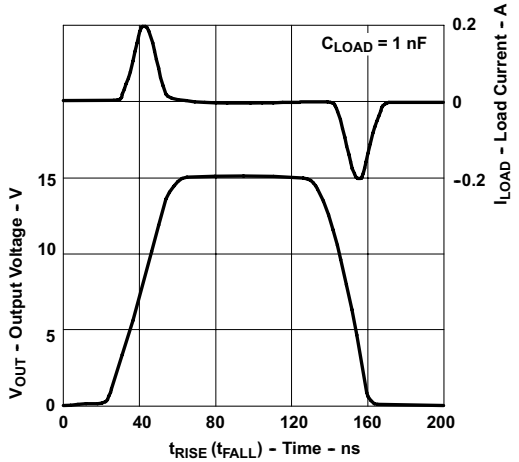


Figure 5. Rise and Fall Time vs Output Voltage and Load Current

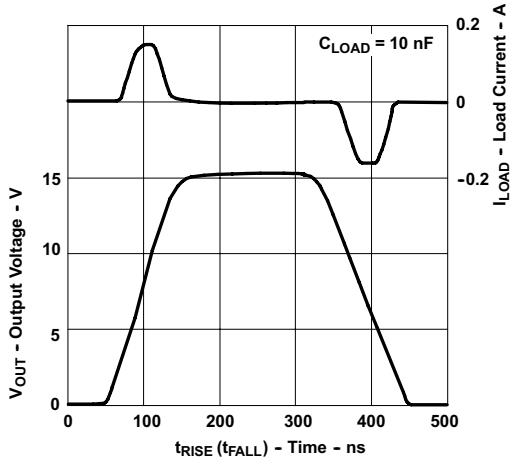


Figure 6. Rise and Fall Time vs Output Voltage and Load Current

7 Parameter Measurement Information

7.1 Control Methods and Test Circuits

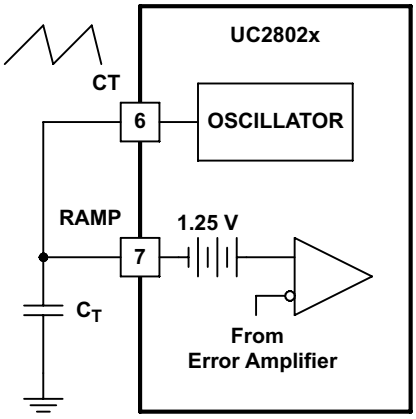
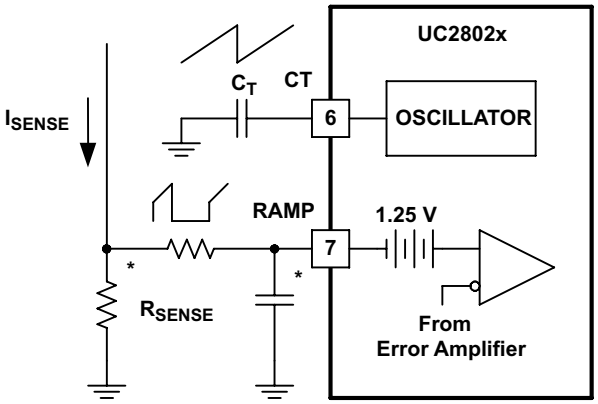


Figure 7. Voltage Mode Control



A small filter may be required to suppress switch noise.

Figure 8. Peak Current Mode Control

Control Methods and Test Circuits (continued)

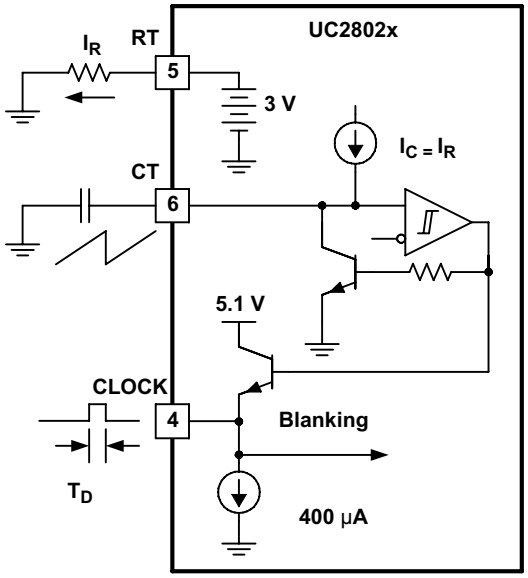


Figure 9. Oscillator Circuit

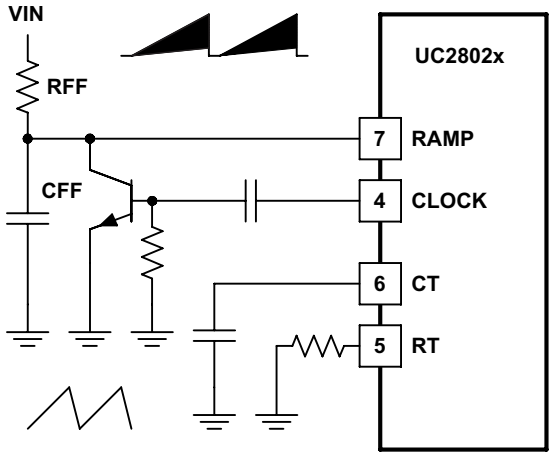


Figure 10. Feedforward Technique for Off-Line Voltage-Mode Applications

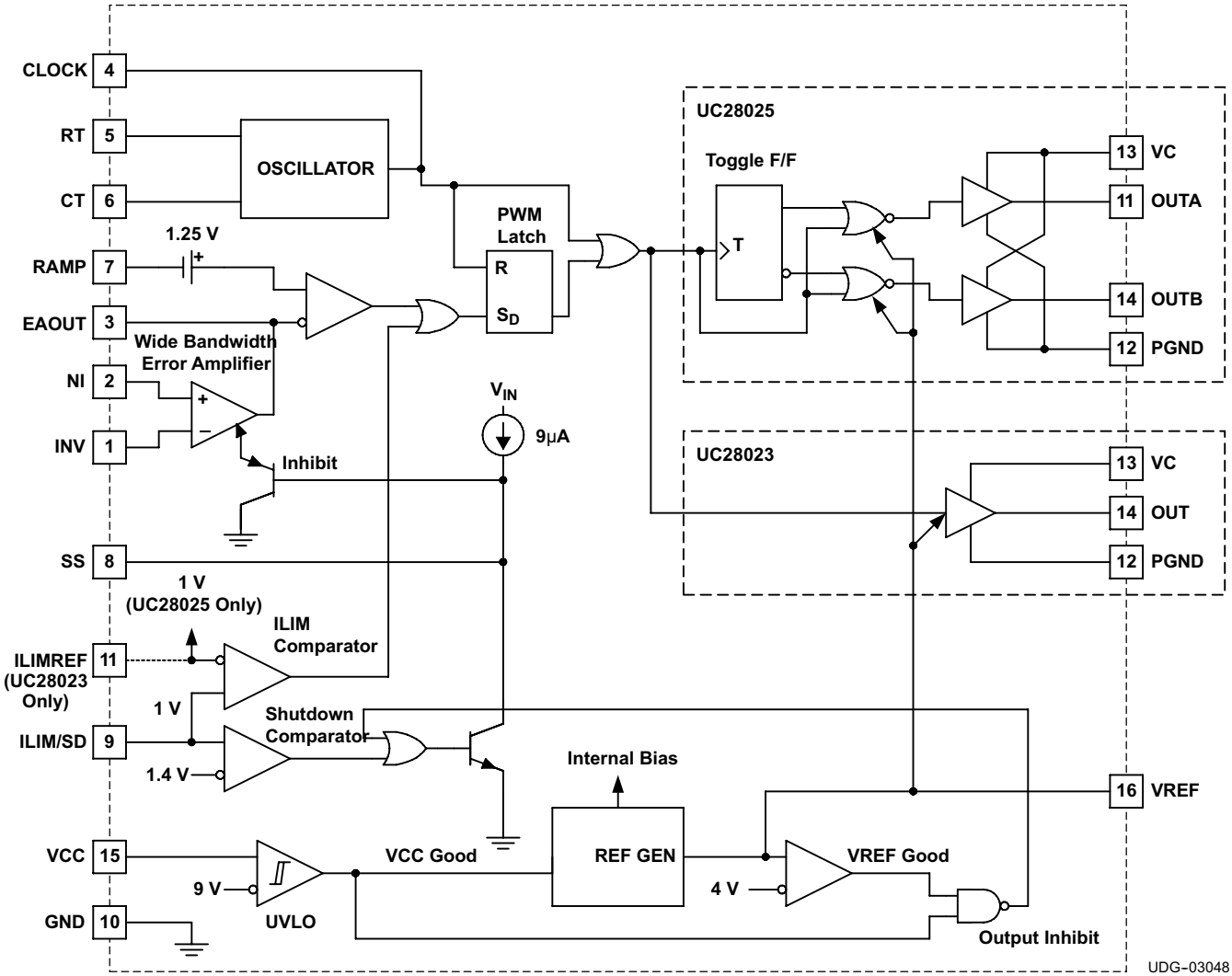
8 Detailed Description

8.1 Overview

The UC28023 and UC28025 (UC2802x) are fixed-frequency PWM controllers optimized for high-frequency switched-mode power-supply applications. Targeted for cost-effective solutions with minimal external components. UC2802x devices include an oscillator, a temperature-compensated reference, a wide band width error amplifier, a high-speed current-sense comparator, and high-current active-high totem-pole outputs to directly drive external MOSFETs.

Protection circuitry includes a current limit comparator with a 1-V threshold, a TTL compatible shutdown port, and a soft-start pin which doubles as a maximum duty cycle clamp. The logic is fully latched to provide jitter free operation and prohibit multiple pulses at an output. An undervoltage lockout section with 800 mV of hysteresis assures low start-up current. During undervoltage lockout, the outputs are high impedance. Propagation delays through the comparators and logic circuitry have been minimized while maximizing bandwidth and slew rate of the error amplifier.

8.2 Functional Block Diagram



8.3 Feature Description

8.3.1 Error Amplifier

Figure 11 shows a simplified schematic of the UC2802x error amplifier and Figure 2 and Figure 3 show its characteristics.

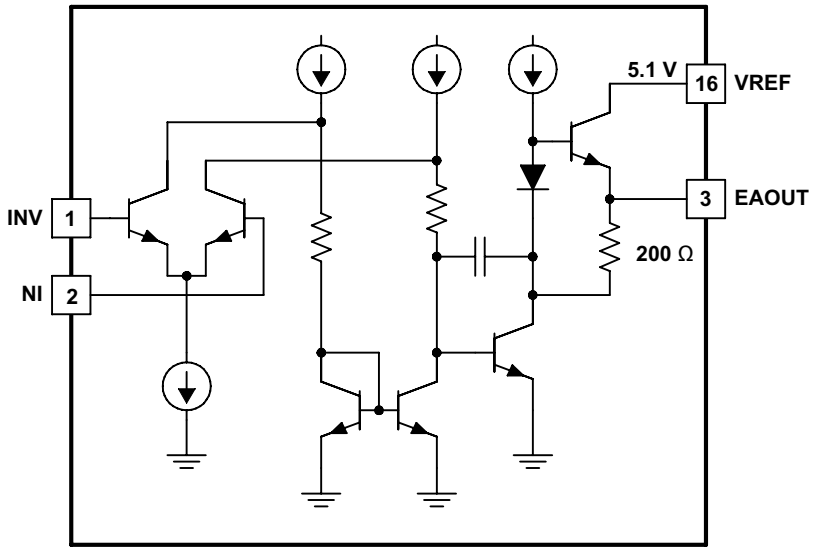


Figure 11. Simplified Error Amplifier Schematic

8.3.2 Synchronization

Figure 12 shows a generalized synchronization. Figure 13 shows a synchronized operation of two units in close proximity.

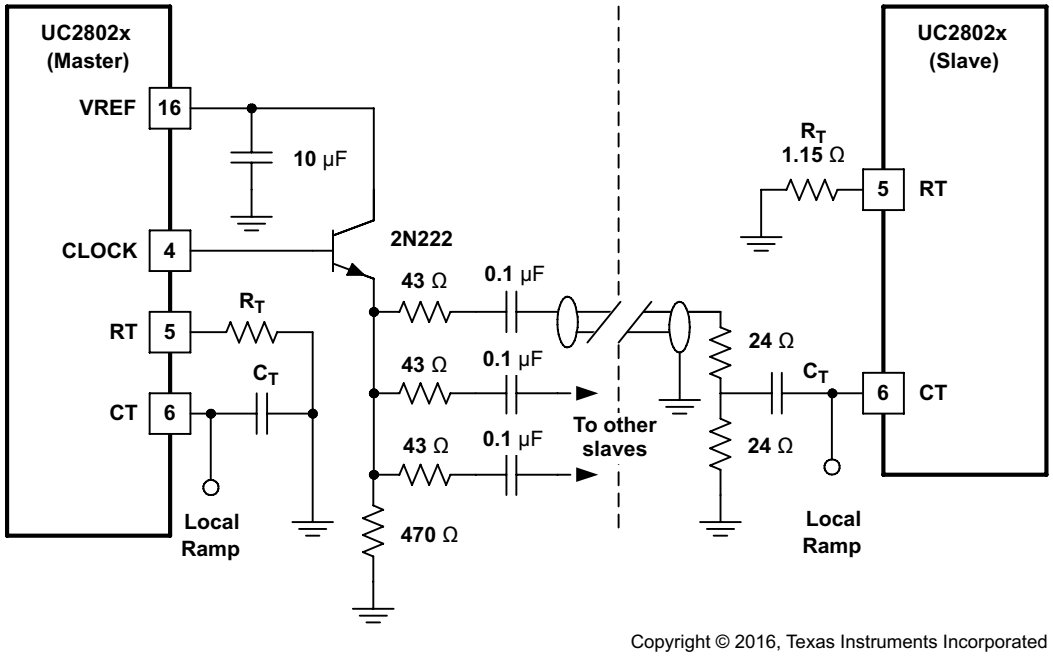


Figure 12. Generalized Synchronization

Feature Description (continued)

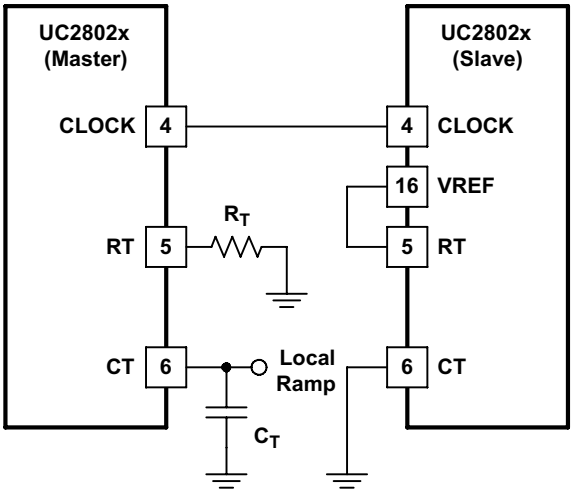


Figure 13. Synchronization of Two Units in Close Proximity

8.3.3 Constant Volt-Second Clamp Circuit

The circuit for the UC28023 shown in Figure 14 describes achievement a constant volt-second product clamp over varying input voltages. The ramp generator components, RT and CR are chosen so that the ramp at Pin 9 (ILIM/SD) crosses the 1-V threshold at the same time the desired maximum volt-second product is reached. The delay through the functional inverter block must be such that the ramp capacitor can be completely discharged during the minimum deadtime.

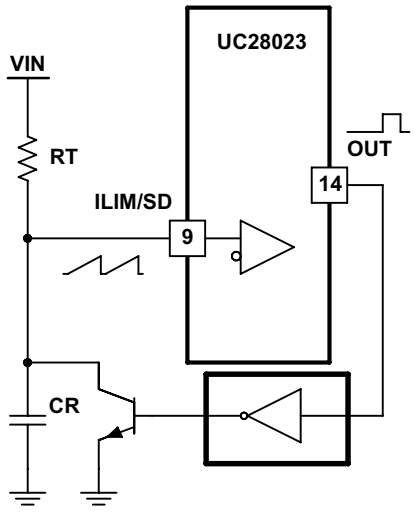


Figure 14. Achieving Constant Volt-Second Product Clamp With the UC28023

The circuit for the UC28025 shown in Figure 15 describes achievement a constant volt-second product clamp over varying input voltages. The ramp generator components, RT and CR are chosen so that the ramp at Pin 9 (ILIM/SD) crosses the 1-V threshold at the same time the desired maximum volt-second product is reached. The delay through the functional inverter block must be such that the ramp capacitor can be completely discharged during the minimum deadtime.

Feature Description (continued)

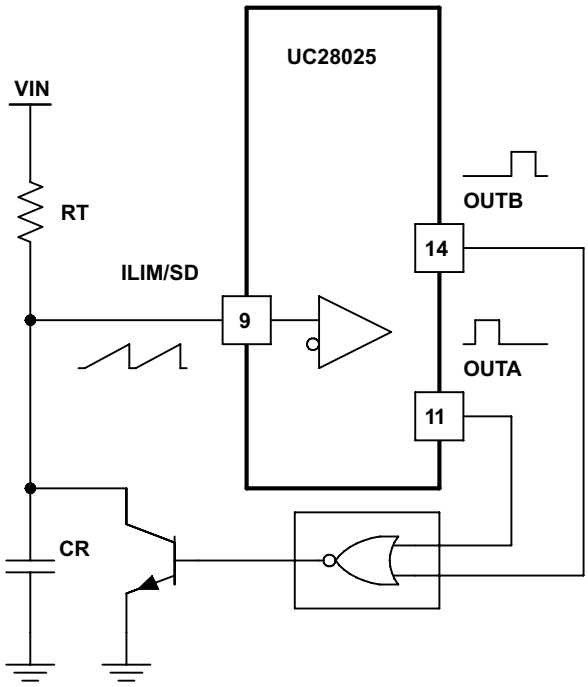


Figure 15. Achieving Constant Volt-Second Product Clamp With the UC28025

8.3.4 Outputs

UC28023 has one output and UC28025 has dual alternating outputs.

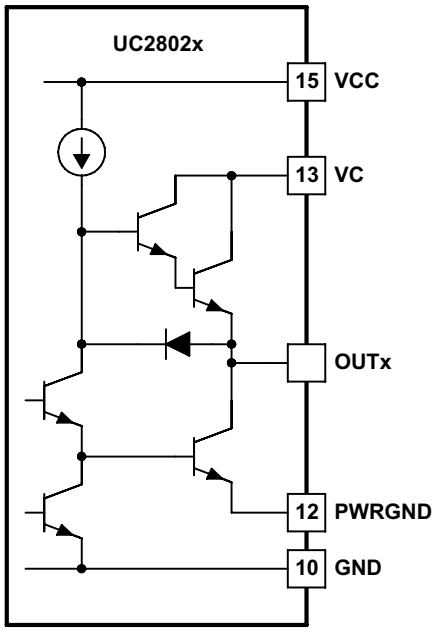


Figure 16. Simplified Schematic

Feature Description (continued)

8.3.5 Open-Loop Laboratory Test Fixture

The following test fixture is useful for exercising many of the UC28025's functions and measuring their specifications. As with any wideband circuit, careful ground and bypass procedures must be followed. TI highly recommends using a ground plane

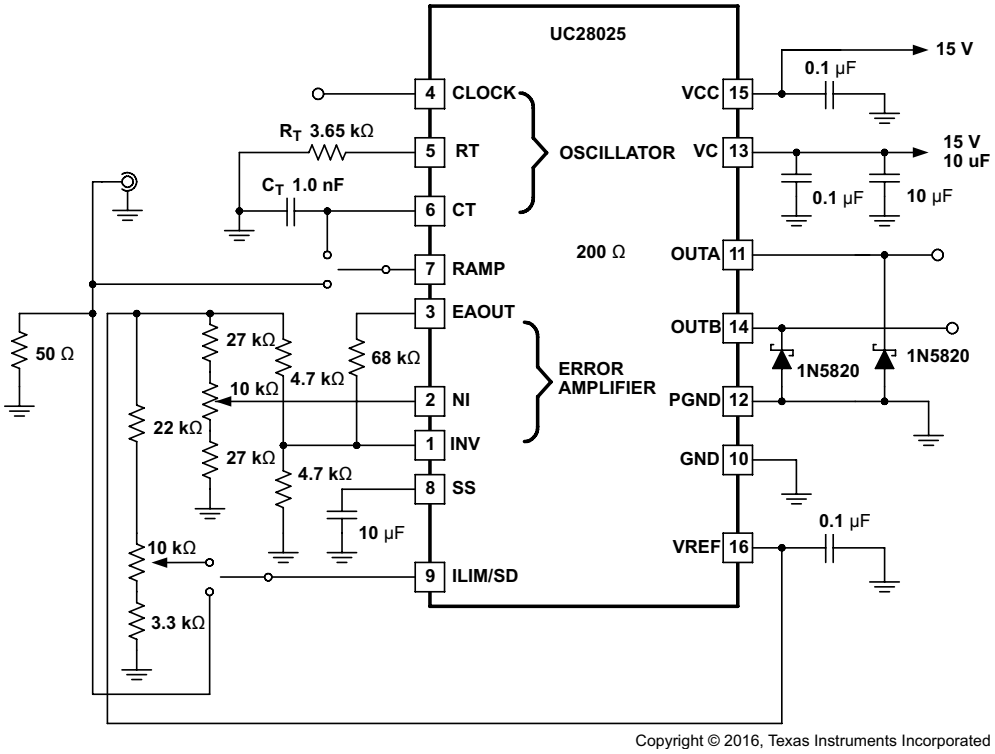


Figure 17. Laboratory Test Fixture

8.4 Device Functional Modes

There are no functional modes for this device.

9 Application and Implementation

NOTE

Information in the following applications sections is not part of the TI component specification, and TI does not warrant its accuracy or completeness. TI's customers are responsible for determining suitability of components for their purposes. Customers should validate and test their design implementation to confirm system functionality.

9.1 Application Information

The UC28023 and UC28025 are fixed-frequency PWM controllers optimized for high-frequency switched-mode power supply applications. The UC28023 is a single output PWM for single-ended topologies while the UC28025 offers dual alternating outputs for double-ended and full bridge topologies.

9.2 Typical Application

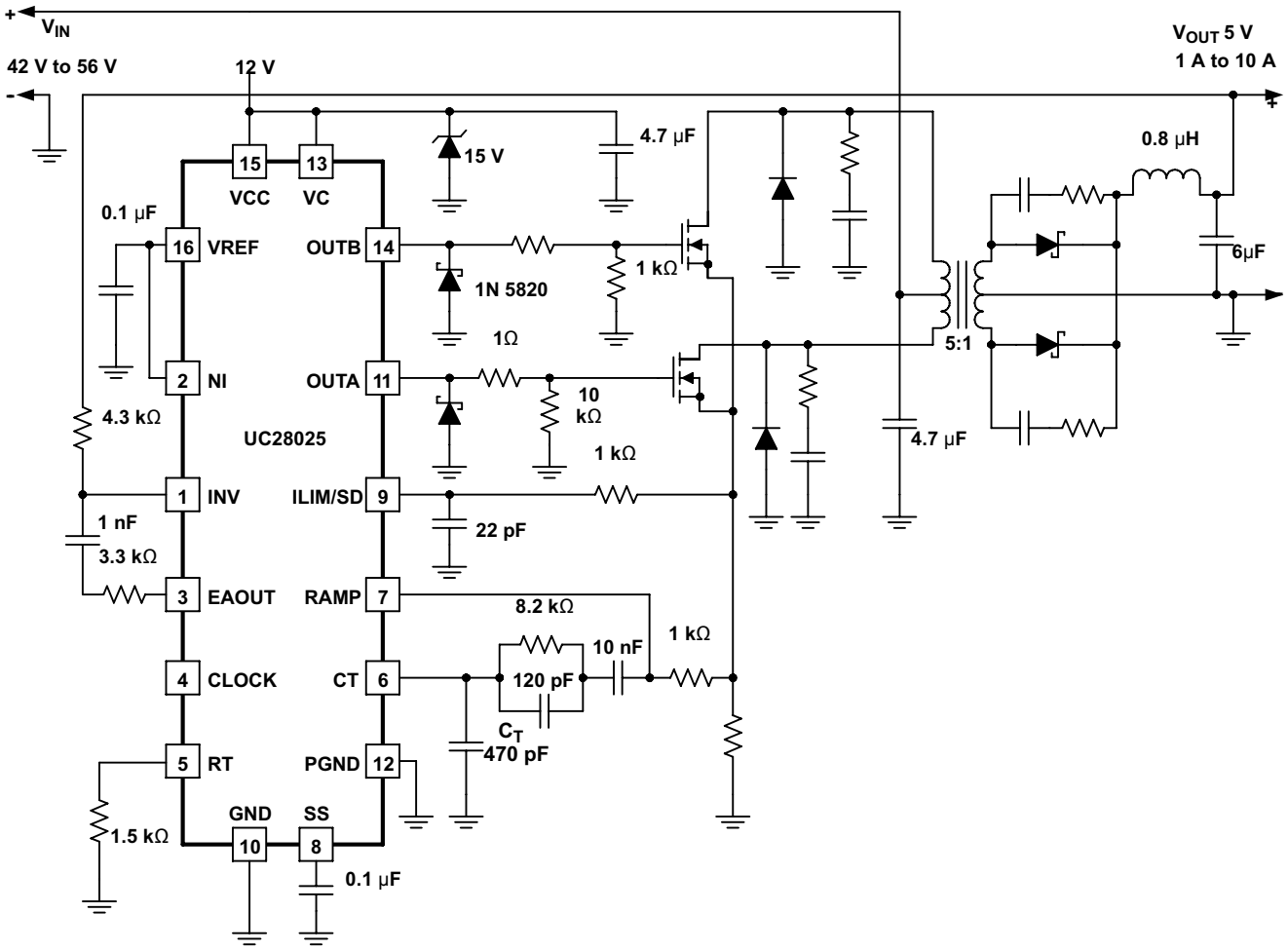


Figure 18. DC-DC Push-Pull Converter Using UC28025

Typical Application (continued)

9.2.1 Design Requirements

For this design example, use the parameters listed in Table 1 as the input parameters.

Table 1. Design Parameters

PARAMETER	EXAMPLE VALUE
Input voltage	42 V to 56 V (48-V typical)
Output voltage	5 V
Output current	1 A to 10 A
Oscillator frequency	1.5 MHz
Switching frequency	750 kHz
Timing resistance	1.5 kΩ
Timing capacitance	470 pF

9.2.2 Detailed Design Procedure

9.2.2.1 Timing Resistor and Capacitor Selection

Generally, a higher switching frequency results in a smaller size but has higher switching losses. Operation at 750 kHz is used in this example as a reasonable compromise between size and efficiency. The values for timing resistance (R_T) and timing capacitance (C_T) are selected for the 1.5-MHz oscillator based on Figure 1.

9.2.2.2 Turns Ratio Selection

The maximum primary-to-secondary turns ratio (N_{MAX}) can be determined with the target output voltage, minimum input voltage, and the estimated maximum duty cycle. D_{LIM} = 0.35 is used for this example. N_{MAX} can be calculated using Equation 1.

$$N_{MAX} = \frac{2 \times D_{LIM} \times V_{INMIN}}{V_{OUT} + V_F} = \frac{2 \times 0.35 \times 42\ V}{5\ V + 0.3\ V} = 5.55 \quad (1)$$

Rounding N_{MAX} down to the next lowest integer results in a turns ratio of N = 5.

9.2.2.3 Inductor Selection

The maximum inductor ripple current occurs at the maximum input voltage. Typically, 20% to 40% of the full load current ripple is a good compromise between core loss and copper loss of the inductor. Higher ripple current allows for smaller inductor size, but places more burden on the output capacitor to smooth the ripple voltage on the output. In this example a ripple current of 25% of 10 A is used. The inductor value can be calculated with Equation 2.

$$L_O = \frac{V_{OUT} + V_F}{\Delta I_L \times f_{SW}} \times \left(\frac{1}{2} - \frac{N \times (V_{OUT} + V_F)}{2 \times V_{INMAX}} \right) = 0.745\ \mu H \quad (2)$$

The closest standard value of 0.8 µH is chosen for L_O, this step is necessary if the chosen L_O differs significantly from the value calculated in Equation 2. The actual ΔI_L is based upon this selected inductor which must be calculated with Equation 3.

$$\Delta I_L = \frac{V_{OUT} + V_F}{L_O \times f_{SW}} \times \left(\frac{1}{2} - \frac{N \times (V_{OUT} + V_F)}{2 \times V_{INMAX}} \right) = 2.327\ A \quad (3)$$

9.2.2.4 Rectifier Diode Selection

A rectifier diode must always possess low-forward voltage drop. When used in high-frequency switching applications, however, the diode must also posses a short recovery time. Schottky diodes meet both requirements and TI recommends their use for push-pull converter designs.

9.2.2.5 Snubber Components Selection

A resistor-capacitor snubber network crossing the low-side MOSFET reduces ringing and spikes at the switching node. Excessive ringing and spikes can cause erratic operation and may couple noise to the output voltage. Selecting the values for the snubber is best accomplished through empirical methods. First, make sure the lead lengths for the snubber connections are very short. Start with a resistor value between 5 Ω and 50 Ω. Increasing the value of the snubber capacitor results in more damping, but higher snubber losses. Select a minimum value for the snubber capacitor that provides adequate damping of the spikes on the switch node waveform at heavy load. A snubber may not be necessary with an optimized layout.

9.2.2.6 VCC and VC Capacitor Selection

The primary purpose of the VCC and VC capacitor is to supply the peak transient currents of the drivers as well as provide stability for the VCC and VC regulator. These peak currents can be several amperes. The value of the VCC and VC capacitor must at least 0.47 µF, and must be a good quality, low ESR, ceramic capacitor. The VCC and VC capacitor must be placed at the pins of the IC to minimize potentially damaging voltage transients caused by trace inductance. A value of 4.7 µF is used in this design.

9.2.2.7 Output Capacitor Selection

The output capacitors smooth the output voltage ripple caused by inductor ripple current and provide a source of charge during load transient conditions. In this design example, a 6-µF capacitor is selected as the main output capacitor.

9.2.2.8 Input Capacitor Selection

The input supply voltage typically has high source impedance at the switching frequency. Good quality input capacitors are necessary to limit the ripple voltage at the VIN pin while supplying most of the switch current during the on-time. The input capacitor must be selected for RMS current rating and minimum ripple voltage. In this example, a 4.7-µF capacitor is used. With ceramic capacitors, the input ripple voltage is triangular.

9.2.3 Application Curves

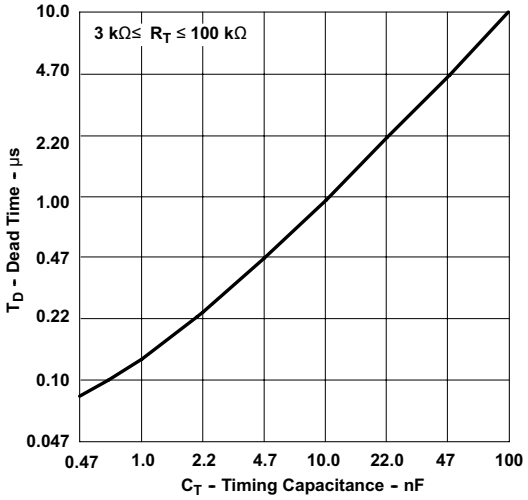


Figure 19. Dead Time vs Timing Capacitance

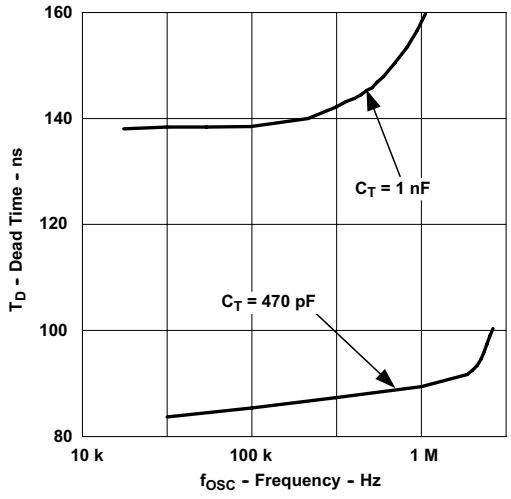


Figure 20. Dead Time vs Frequency

10 Power Supply Recommendations

The UC28023 and UC28025 operate from an external bias supply. TI recommends powering the device from a regulated auxiliary supply. (This device is not intended to be used from a bootstrap bias supply. A bootstrap bias supply is fed from the input high voltage through a resistor with sufficient capacitance on VCC to hold up the voltage on VCC until current can be supplied from a bias winding on the boost inductor. For that reason, the minimal hysteresis on VCC would require an unreasonable value of hold-up capacitance.)

11 Layout

11.1 Layout Guidelines

High speed circuits demand careful attention to layout and component placement. To assure proper performance of the UC2802x follow these rules:

1. Use a ground plane.
2. Damp or clamp parasitic inductive kick energy from the gate of driven MOSFETs. Do not allow the output pins to ring below ground. A series gate resistor or a shunt 1-A Schottky diode at the output pin serves this purpose.
3. Bypass VCC, VC, and VREF. Use 0.1-µF monolithic ceramic capacitors with low equivalent series inductance. Allow less than 1 cm of total lead length for each capacitor between the bypassed pin and the ground plane.
4. Treat the timing capacitor (C_T) as a bypass capacitor.

11.2 Layout Example

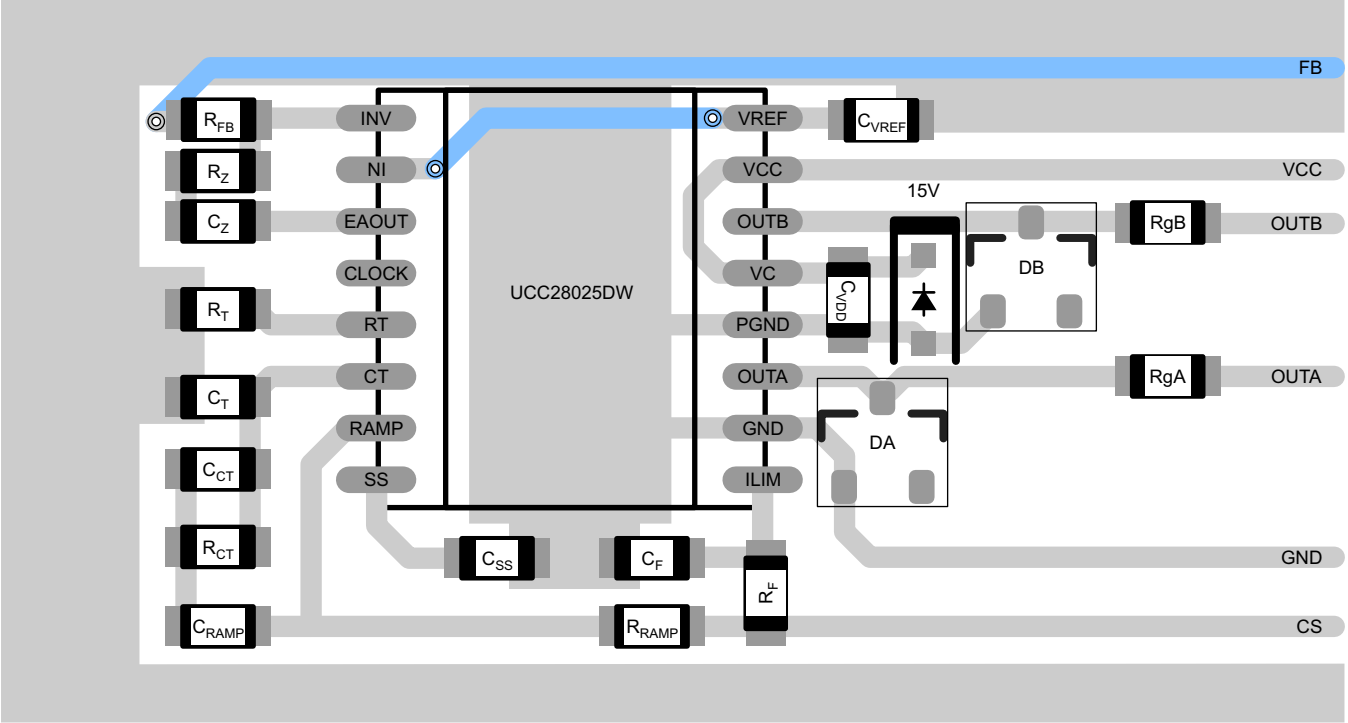


Figure 21. Layout Recommendation

12 Device and Documentation Support

12.1 Documentation Support

12.1.1 Related Documentation

For related documentation see the following:

- *1.5-MHz Current Mode IC Controlled 50--Watt Power Supply* (SLUA053)
- *The UC3823A,B and UC3825A,B Enhanced Generation of PWM Controllers* (SLUA125)

12.2 Related Links

The table below lists quick access links. Categories include technical documents, support and community resources, tools and software, and quick access to sample or buy.

Table 2. Related Links

PARTS	PRODUCT FOLDER	SAMPLE & BUY	TECHNICAL DOCUMENTS	TOOLS & SOFTWARE	SUPPORT & COMMUNITY
UC28023	Click here	Click here	Click here	Click here	Click here
UC28025	Click here	Click here	Click here	Click here	Click here

12.3 Receiving Notification of Documentation Updates

To receive notification of documentation updates, navigate to the device product folder on ti.com. In the upper right corner, click on *Alert me* to register and receive a weekly digest of any product information that has changed. For change details, review the revision history included in any revised document.

12.4 Community Resources

The following links connect to TI community resources. Linked contents are provided "AS IS" by the respective contributors. They do not constitute TI specifications and do not necessarily reflect TI's views; see TI's Terms of Use.

TI E2E™ Online Community ***TI's Engineer-to-Engineer (E2E) Community.*** Created to foster collaboration among engineers. At e2e.ti.com, you can ask questions, share knowledge, explore ideas and help solve problems with fellow engineers.

Design Support ***TI's Design Support*** Quickly find helpful E2E forums along with design support tools and contact information for technical support.

12.5 Trademarks

E2E is a trademark of Texas Instruments.
All other trademarks are the property of their respective owners.

12.6 Electrostatic Discharge Caution

This integrated circuit can be damaged by ESD. Texas Instruments recommends that all integrated circuits be handled with appropriate precautions. Failure to observe proper handling and installation procedures can cause damage.

ESD damage can range from subtle performance degradation to complete device failure. Precision integrated circuits may be more susceptible to damage because very small parametric changes could cause the device not to meet its published specifications.

12.7 Glossary

SLYZ022 — *TI Glossary*.

This glossary lists and explains terms, acronyms, and definitions.

13 Mechanical, Packaging, and Orderable Information

The following pages include mechanical, packaging, and orderable information. This information is the most current data available for the designated devices. This data is subject to change without notice and revision of this document. For browser-based versions of this data sheet, refer to the left-hand navigation.

PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead finish/ Ball material (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
UC28023DW	ACTIVE	SOIC	DW	16	40	RoHS & Green	NIPDAU	Level-2-260C-1 YEAR	-40 to 105	UC28023DW	Samples
UC28023DWR	ACTIVE	SOIC	DW	16	2000	RoHS & Green	NIPDAU	Level-2-260C-1 YEAR	-40 to 105	UC28023DW	Samples
UC28025DW	ACTIVE	SOIC	DW	16	40	RoHS & Green	NIPDAU	Level-2-260C-1 YEAR	-40 to 105	UC28025DW	Samples
UC28025DWG4	ACTIVE	SOIC	DW	16	40	RoHS & Green	NIPDAU	Level-2-260C-1 YEAR	-40 to 105	UC28025DW	Samples
UC28025DWR	ACTIVE	SOIC	DW	16	2000	RoHS & Green	NIPDAU	Level-2-260C-1 YEAR	-40 to 105	UC28025DW	Samples
UC28025N	ACTIVE	PDIP	N	16	25	RoHS & Green	NIPDAU	N / A for Pkg Type	-40 to 105	UC28025N	Samples
UC28025NG4	ACTIVE	PDIP	N	16	25	RoHS & Green	NIPDAU	N / A for Pkg Type	-40 to 105	UC28025N	Samples

(1) The marketing status values are defined as follows:
ACTIVE: Product device recommended for new designs.
LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
PREVIEW: Device has been announced but is not in production. Samples may or may not be available.
OBSOLETE: TI has discontinued the production of the device.

(2) **RoHS:** TI defines "RoHS" to mean semiconductor products that are compliant with the current EU RoHS requirements for all 10 RoHS substances, including the requirement that RoHS substance do not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, "RoHS" products are suitable for use in specified lead-free processes. TI may reference these types of products as "Pb-Free".
RoHS Exempt: TI defines "RoHS Exempt" to mean products that contain lead but are compliant with EU RoHS pursuant to a specific EU RoHS exemption.
Green: TI defines "Green" to mean the content of Chlorine (Cl) and Bromine (Br) based flame retardants meet JS709B low halogen requirements of <=1000ppm threshold. Antimony trioxide based flame retardants must also meet the <=1000ppm threshold requirement.

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

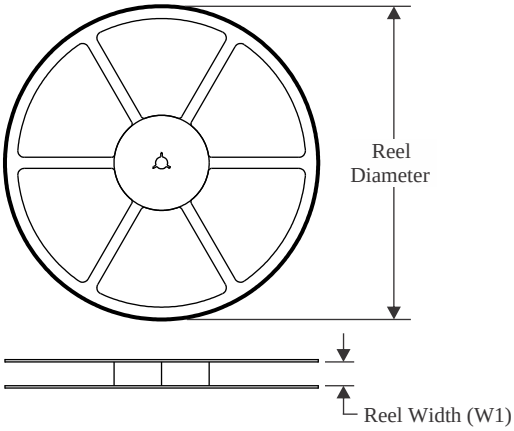
(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

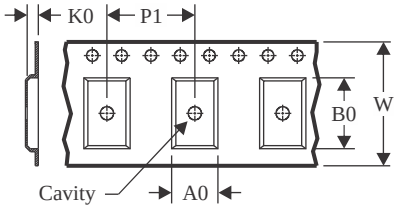
(6) Lead finish/Ball material - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

TAPE AND REEL INFORMATION

REEL DIMENSIONS

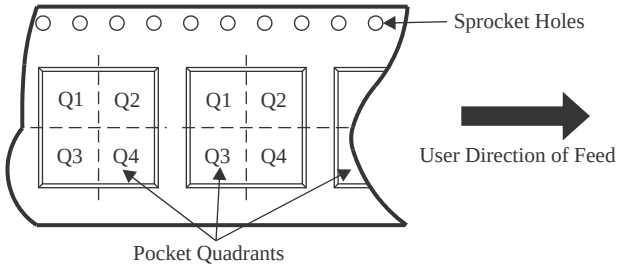


TAPE DIMENSIONS



A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

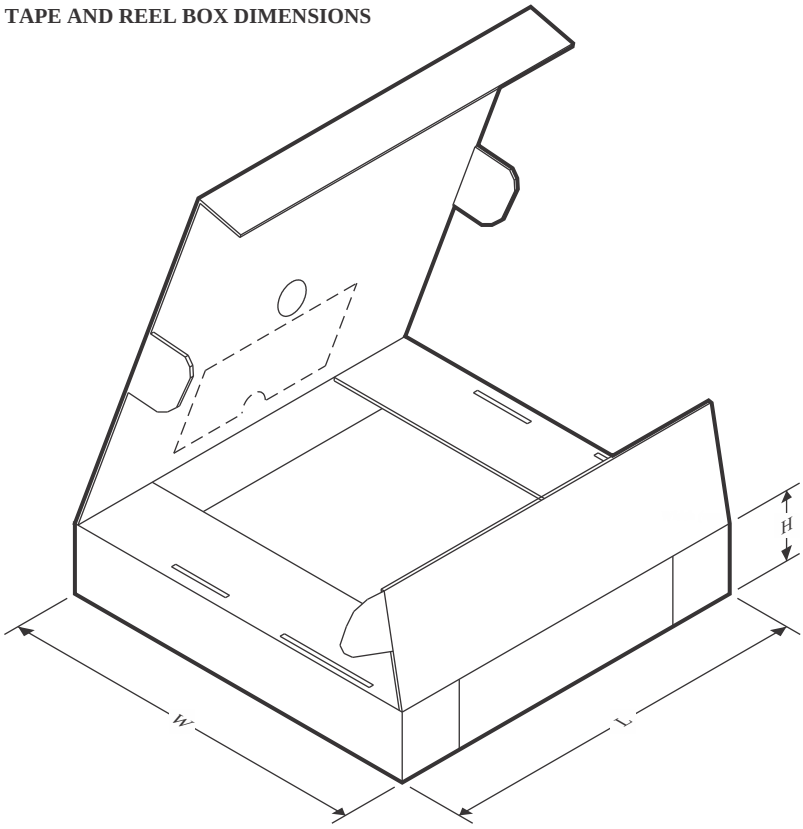
QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
UC28023DWR	SOIC	DW	16	2000	330.0	16.4	10.75	10.7	2.7	12.0	16.0	Q1
UC28025DWR	SOIC	DW	16	2000	330.0	16.4	10.75	10.7	2.7	12.0	16.0	Q1

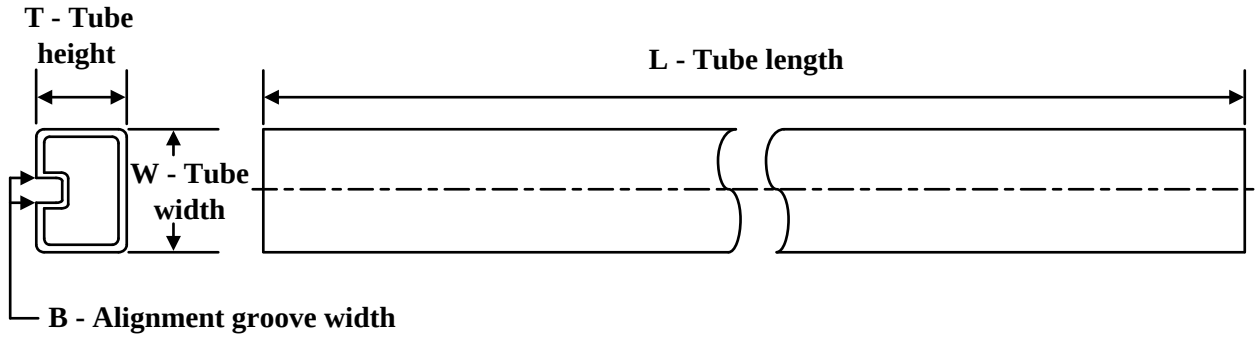
TAPE AND REEL BOX DIMENSIONS



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
UC28023DWR	SOIC	DW	16	2000	356.0	356.0	35.0
UC28025DWR	SOIC	DW	16	2000	356.0	356.0	35.0

TUBE



*All dimensions are nominal

Device	Package Name	Package Type	Pins	SPQ	L (mm)	W (mm)	T (µm)	B (mm)
UC28023DW	DW	SOIC	16	40	507	12.83	5080	6.6
UC28025DW	DW	SOIC	16	40	507	12.83	5080	6.6
UC28025DWG4	DW	SOIC	16	40	507	12.83	5080	6.6
UC28025N	N	PDIP	16	25	506	13.97	11230	4.32
UC28025NG4	N	PDIP	16	25	506	13.97	11230	4.32

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