ULN2003B High-Voltage, High-Current Darlington Transistor Array

1 Features

- Greater Than 4x Reduction in Output Leakage (I_{CEX}) over ULN2003A
- 500-mA Rated Collector Current (Single Output)
- High-Voltage Outputs 50 V
- Output Clamp Diodes
- Inputs Compatible With Various Types of Logic
- Relay-Driver Applications

2 Applications

- Relay Drivers
- Lamp Drivers
- Display Drivers (LED and Gas Discharge)
- Line Drivers
- Logic Buffers

3 Description

The ULN2003B device is a high-voltage, high-current Darlington transistor array. This device consists of seven NPN Darlington pairs that feature high-voltage outputs with common-cathode clamp diodes for switching inductive loads. The collector-current rating of a single Darlington pair is 500 mA. The Darlington pairs can be paralleled for higher current capability.

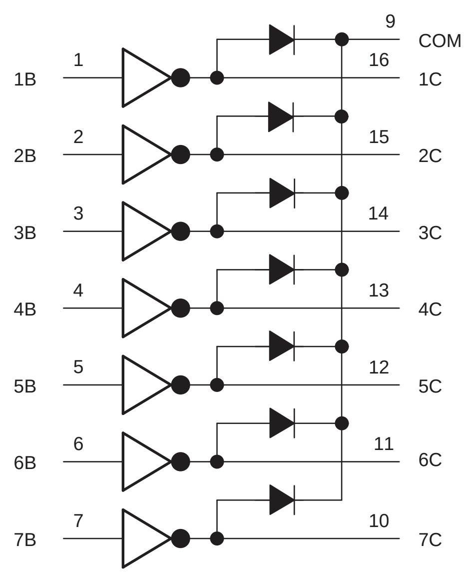
The ULN2003B has a 2.7-kΩ series base resistor for each Darlington pair for operation directly with TTL or CMOS devices.

Device Information(1)

PART NUMBER	PACKAGE	BODY SIZE (NOM)
ULN2003BN	PDIP (16)	19.30 mm × 6.35 mm
ULN2003BD	SOIC (16)	9.90 mm × 3.91 mm
ULN2003BPW	TSSOP (16)	5.00 mm × 4.40 mm

(1) For all available packages, see the orderable addendum at the end of the datasheet.

Simplified Schematic



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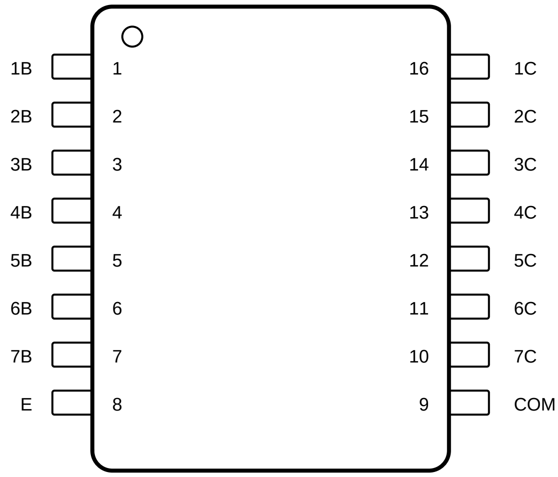
- Deleted Hammer Drivers from *Applications* ... 1
- Updated *Pin Functions* table ... 3
- Deleted Package Themal Information from *Absolute Maximum Ratings* ... 4
- Moved Storage temperature, T_{stg} to *Absolute Maximum Ratings* ... 4
- Deleted V_I from *Recommended Operating Conditions* ... 4
- Updated *Thermal Information* table ... 4
- Moved Operating free-air temperature, T_A to *Recommended Operating Conditions* ... 4
- Deleted *Output Current vs Input Current* graph from *Typical Characteristics* section ... 6
- Added h_{FE} *vs* I_{OUT} to *Typical Characteristics* section ... 6
- Deleted *Thermal Information* graphs section and updated *Typical Characteristics* section with new thermal graphs Figure 6 through Figure 14 ... 6
- Added *Receiving Notification of Documentation Updates* section and *Community Resources* section ... 14

Changes from Original (June 2014) to Revision A — **Page**

- Initial release of full version. ... 1
- Added Pin Functions table ... 3
- Added Thermal Information table. ... 4

5 Pin Configuration and Functions

D, N, or PW Package
16-Pin SOIC, PDIP, or TSSOP
Top View



Not to scale

Pin Functions

PIN		I/O(1)	DESCRIPTION
NAME	NO.		
1B	1	I	Channel 1 through 7 darlington base input
2B	2		
3B	3		
4B	4		
5B	5		
6B	6		
7B	7		
1C	16	O	Channel 1 through 7 darlington collector output
2C	15		
3C	14		
4C	13		
5C	12		
6C	11		
7C	10		
COM	9	—	Common cathode node for flyback diodes (required for inductive loads)
E	8	—	Common Emmitter shared by all channels (typically tied to ground)

(1) I = Input, O = Output

6 Specifications

6.1 Absolute Maximum Ratings

at 25°C free-air temperature (unless otherwise noted)(1)

		MIN	MAX	UNIT
V_{CC}	Collector-emitter voltage		50	V
	Clamp diode reverse voltage(2)		50	V
V_I	Input voltage(2)		30	V
	Peak collector current(3)(4)		500	mA
I_{OK}	Output clamp current		500	mA
	Total emitter-terminal current		–2.5	A
T_J	Operating virtual junction temperature		150	°C
T_{stg}	Storage temperature	–65	150	°C

(1) Stresses beyond those listed under *Absolute Maximum Ratings* may cause permanent damage to the device. These are stress ratings only, which do not imply functional operation of the device at these or any other conditions beyond those indicated under *Recommended Operating Conditions*. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
(2) All voltage values are with respect to the emitter/substrate terminal E, unless otherwise noted.
(3) Maximum power dissipation is a function of T_J(max), θ_{JA}, and T_A. The maximum allowable power dissipation at any allowable ambient temperature is $P_D = (T_J(max) – T_A)/\theta_{JA}$. Operating at the absolute maximum T_J of 150°C can affect reliability.
(4) The package thermal impedance is calculated in accordance with JESD 51-7.

6.2 ESD Ratings

			VALUE	UNIT
$V_{(ESD)}$	Electrostatic discharge	Human body model (HBM), per ANSI/ESDA/JEDEC JS-001(1)	2000	V
		Charged device model (CDM), per JEDEC specification JESD22-C101(2)	500	

(1) JEDEC document JEP155 states that 500-V HBM allows safe manufacturing with a standard ESD control process.
(2) JEDEC document JEP157 states that 250-V CDM allows safe manufacturing with a standard ESD control process.

6.3 Recommended Operating Conditions

over operating free-air temperature range (unless otherwise noted)

		MIN	MAX	UNIT
V_{CC}	Supply Voltage	0	50	V
T_A	Operating free-air temperature	–40	105	°C
T_J	Junction Temperature	–40	125	°C

6.4 Thermal Information

THERMAL METRIC(1)		ULN2003B			UNIT
		PW (TSSOP)	D (SOIC)	N (PDIP)	
		16 PINS	16 PINS	16 PINS	
$R_{\theta JA}$	Junction-to-ambient thermal resistance	105.5	81.2	49.6	°C/W
$R_{\theta JC(top)}$	Junction-to-case (top) thermal resistance	38.3	40	36.2	°C/W
$R_{\theta JB}$	Junction-to-board thermal resistance	50.9	38.6	29.2	°C/W
ψ_{JT}	Junction-to-top characterization parameter	4.1	10.5	20.2	°C/W
ψ_{JB}	Junction-to-board characterization parameter	50.3	38.3	29.5	°C/W

(1) For more information about traditional and new thermal metrics, see the *Semiconductor and IC Package Thermal Metrics* application report.

6.5 Electrical Characteristics, T_A = 25°C

PARAMETER		TEST FIGURE	TEST CONDITIONS		MIN	TYP	MAX	UNIT
$V_{I(on)}$	On-state input voltage	Figure 19	V_{CE} = 2 V	I_C = 200 mA			2.4	V
				I_C = 250 mA			2.7	
				I_C = 300 mA			3	
$V_{CE(sat)}$	Collector-emitter saturation voltage	Figure 18	I_I = 250 µA,	I_C = 100 mA		0.9	1.1	V
			I_I = 350 µA,	I_C = 200 mA		1	1.3	
			I_I = 500 µA,	I_C = 350 mA		1.2	1.6	
I_{CEX}	Collector cutoff current	Figure 15	V_{CE} = 50 V,	I_I = 0			10	µA
V_F	Clamp forward voltage	Figure 21	I_F = 350 mA			1.7	2	V
$I_{I(off)}$	Off-state input current	Figure 16	V_{CE} = 50 V,	I_C = 500 µA	50	65		µA
I_I	Input current	Figure 17	V_I = 3.85 V			0.93	1.35	mA
I_R	Clamp reverse current	Figure 20	V_R = 50 V				50	µA
C_i	Input capacitance		V_I = 0,	f = 1 MHz		15	25	pF

6.6 Electrical Characteristics, T_A = –40°C to +105°C

PARAMETER		TEST FIGURE	TEST CONDITIONS		MIN	TYP	MAX	UNIT
$V_{I(on)}$	On-state input voltage	Figure 19	V_{CE} = 2 V	I_C = 200 mA			2.7	V
				I_C = 250 mA			2.9	
				I_C = 300 mA			3	
$V_{CE(sat)}$	Collector-emitter saturation voltage	Figure 18	I_I = 250 µA,	I_C = 100 mA		0.9	1.2	V
			I_I = 350 µA,	I_C = 200 mA		1	1.4	
			I_I = 500 µA,	I_C = 350 mA		1.2	1.7	
I_{CEX}	Collector cutoff current	Figure 15	V_{CE} = 50 V,	I_I = 0			20	µA
V_F	Clamp forward voltage	Figure 21	I_F = 350 mA			1.7	2.2	V
$I_{I(off)}$	Off-state input current	Figure 16	V_{CE} = 50 V,	I_C = 500 µA	30	65		µA
I_I	Input current	Figure 17	V_I = 3.85 V			0.93	1.35	mA
I_R	Clamp reverse current	Figure 20	V_R = 50 V				100	µA
C_i	Input capacitance		V_I = 0,	f = 1 MHz		15	25	pF

6.7 Switching Characteristics, T_A = 25°C

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
t_{PLH}	Propagation delay time, low- to high-level output			0.25	1	µs
t_{PHL}	Propagation delay time, high- to low-level output			0.25	1	µs
V_{OH}	High-level output voltage after switching	V_S = 50 V, I_O ≈ 300 mA	V_S – 20			mV

6.8 Switching Characteristics, T_A = –40°C to +105°C

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
t_{PLH}	Propagation delay time, low- to high-level output			1	10	µs
t_{PHL}	Propagation delay time, high- to low-level output			1	10	µs
V_{OH}	High-level output voltage after switching	V_S = 50 V, I_O ≈ 300 mA	V_S – 50			mV

6.9 Typical Characteristics

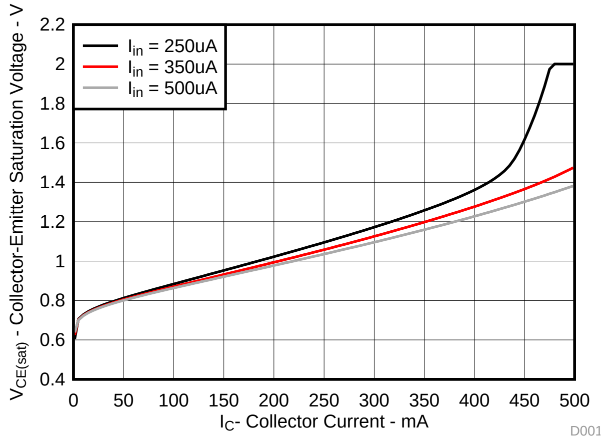


Figure 1. Collector-Emitter Saturation Voltage vs Collector Current (One Darlington)

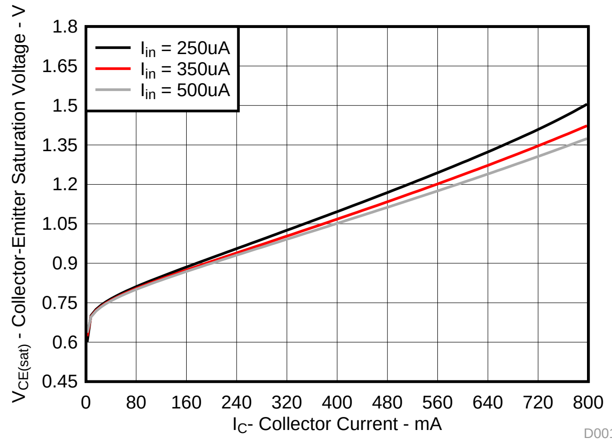


Figure 2. Collector-Emitter Saturation Voltage vs Total Collector Current (Two Darlingtons in Parallel)

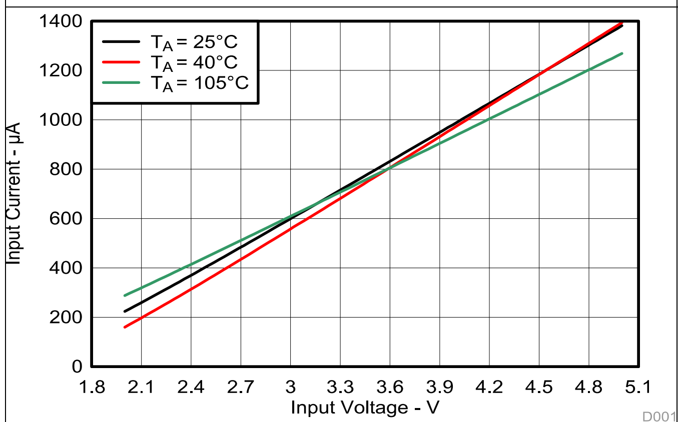


Figure 3. Input Current vs Input Voltage

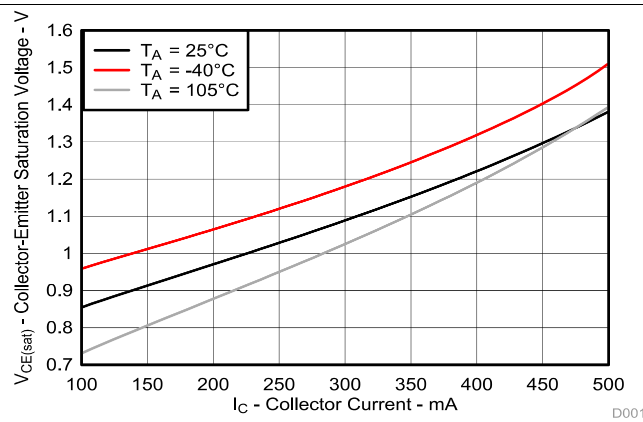


Figure 4. Collector-Emitter Saturation Voltage vs Collector Current

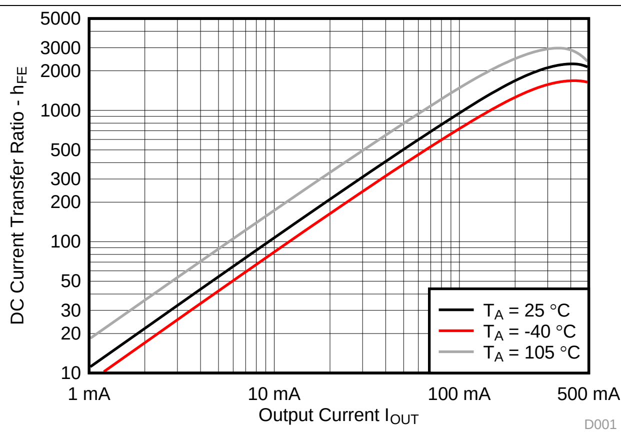


Figure 5. h_{FE} vs I_{OUT}

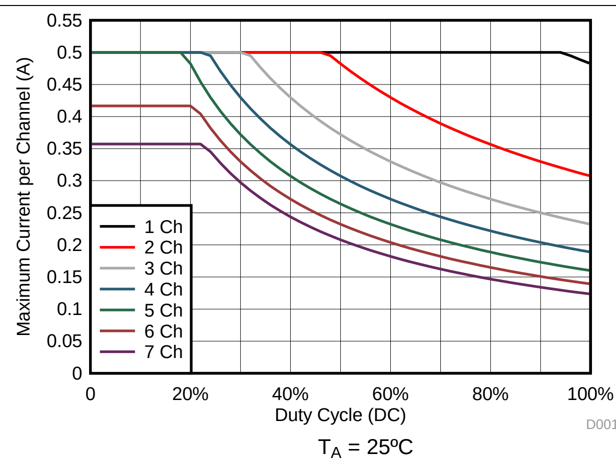


Figure 6. D Package Maximum Collector Current vs Duty Cycle

Typical Characteristics (continued)

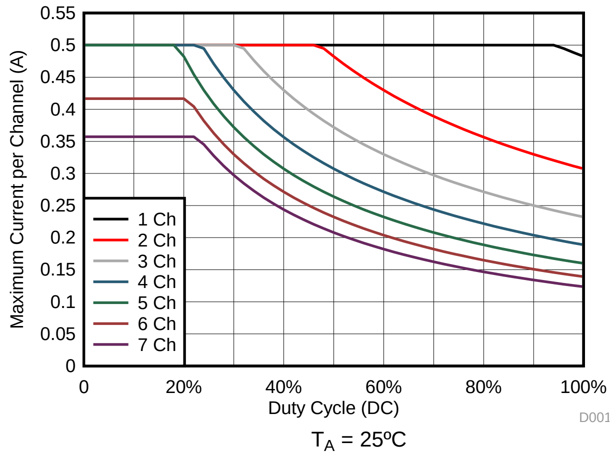


Figure 7. PW Package Maximum Collector Current vs Duty Cycle

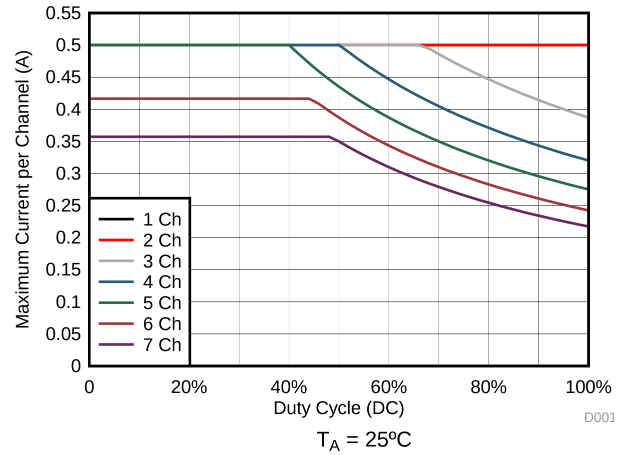


Figure 8. N Package Maximum Collector Current vs Duty Cycle

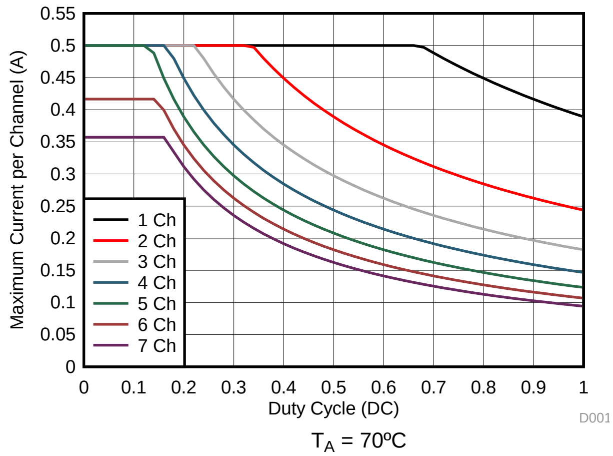


Figure 9. D Package Maximum Collector Current vs Duty Cycle

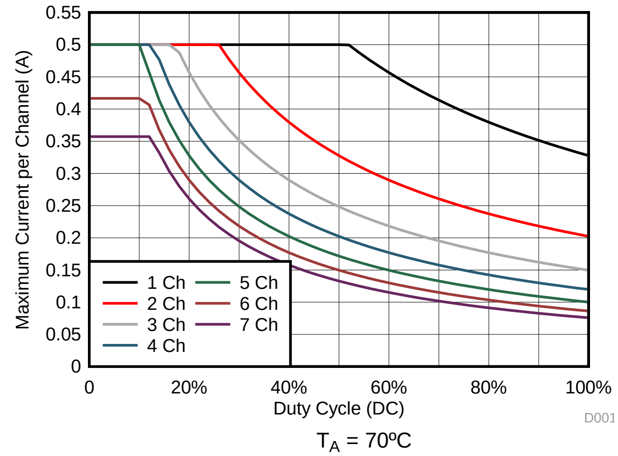


Figure 10. PW Package Maximum Collector Current vs Duty Cycle

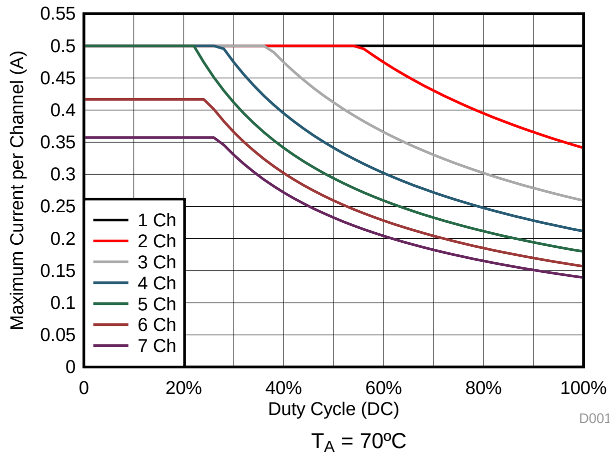


Figure 11. N Package Maximum Collector Current vs Duty Cycle

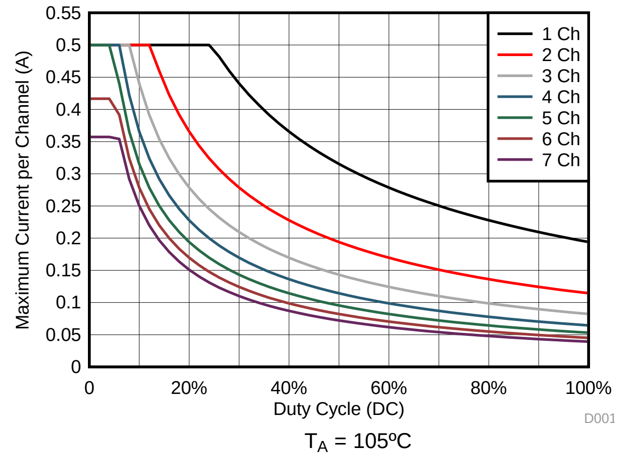
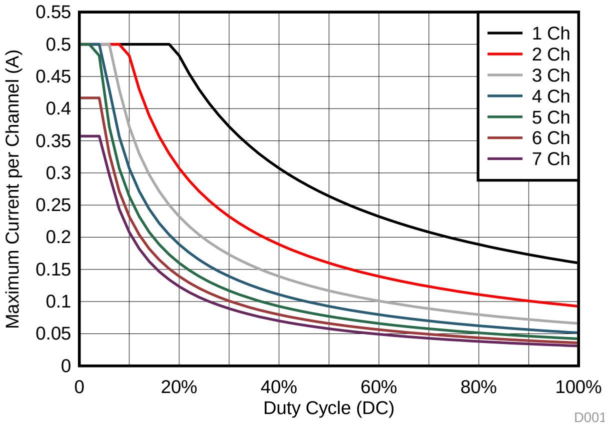


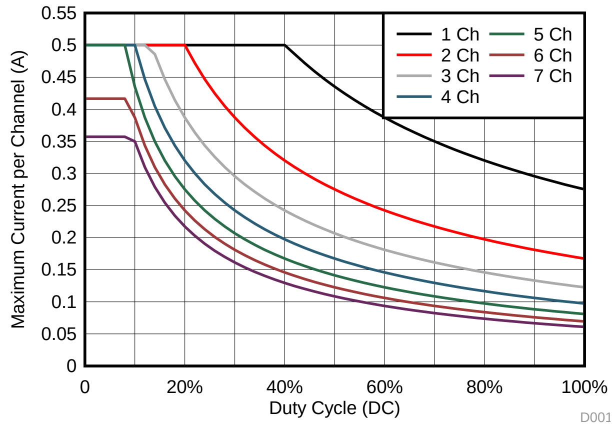
Figure 12. D Package Maximum Collector Current vs Duty Cycle

Typical Characteristics (continued)



T_A = 105ºC

Figure 13. PW Package Maximum Collector Current vs Duty Cycle



T_A = 105ºC

Figure 14. N Package Maximum Collector Current vs Duty Cycle

7 Parameter Measurement Information

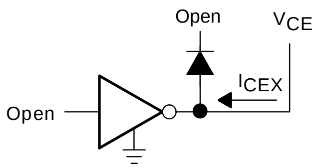


Figure 15. I_{CEX} Test Circuit

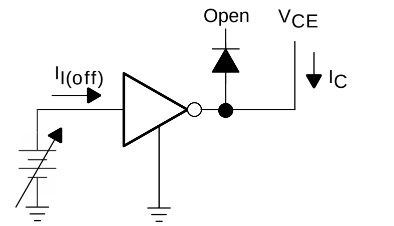


Figure 16. $I_{I(off)}$ Test Circuit

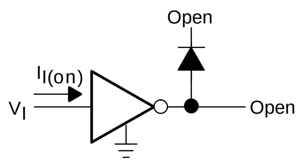


Figure 17. I_I Test Circuit

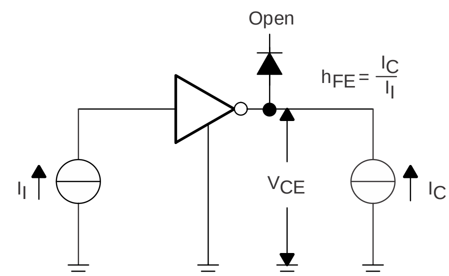


Figure 18. h_{fe} , $V_{CE(sat)}$ Test Circuit

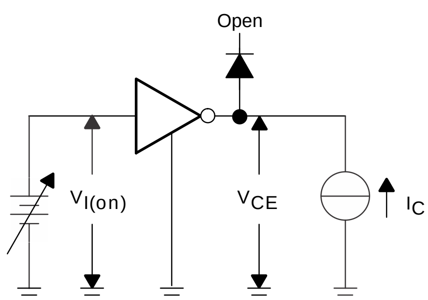


Figure 19. $V_{I(on)}$ Test Circuit

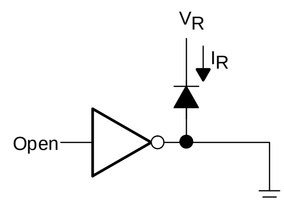


Figure 20. I_R Test Circuit

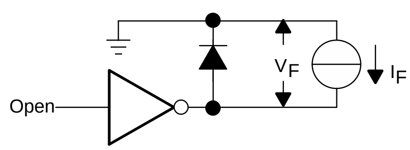


Figure 21. V_F Test Circuit

8 Detailed Description

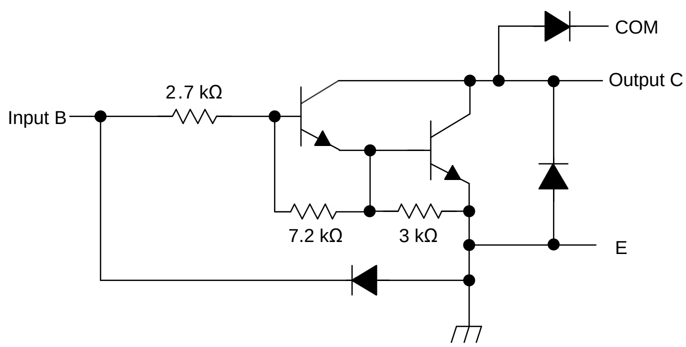
8.1 Overview

This standard device has proven ubiquity and versatility across a wide range of applications. This is due to it's integration of 7 Darlington transistors that are capable of sinking up to 500 mA and wide GPIO range capability.

The ULN2003B comprises seven high voltage, high current NPN Darlington transistor pairs. All units feature a common emitter and open collector outputs. To maximize their effectiveness, these units contain suppression diodes for inductive loads. The ULN2003B has a series base resistor to each Darlington pair, thus allowing operation directly with TTL or CMOS operating at supply voltages of 5 V or 3.3 V. The ULN2003B offers solutions to a great many interface needs, including solenoids, relays, lamps, small motors, and LEDs. Applications requiring sink currents beyond the capability of a single output may be accommodated by paralleling the outputs.

This device can operate over a wide temperature range (–40°C to +105°C).

8.2 Functional Block Diagram



All resistor values shown are nominal.

Figure 22. Schematic (Each Driver)

8.3 Feature Description

Each channel of ULN2003B consists of Darlington connected NPN transistors. This connection creates the effect of a single transistor with a very high current gain. This beta can be high at certain currents see Figure 5.

The GPIO voltage is converted to base current through the 2.7-kΩ resistor connected between the input and base of the pre-driver Darlington NPN. The 7.2-kΩ and 3-kΩ resistors connected between the base and emitter of each respective NPN act as pull-downs and suppress the amount of leakage that may occur from the input.

The diodes connected between the output and COM pin is used to suppress the kick-back voltage from an inductive load that is excited when the NPN drivers are turned off (stop sinking) and the stored energy in the coils causes a reverse current to flow into the coil supply through the kick-back diode.

In normal operation the diodes on base and collector pins to emitter will be reversed biased. If these diode are forward biased, internal parasitic NPN transistors will draw (a nearly equal) current from other (nearby) device pins.

8.4 Device Functional Modes

8.4.1 Inductive Load Drive

When the COM pin is tied to the coil supply voltage, ULN2003B is able to drive inductive loads and suppress the kick-back voltage through the internal free wheeling diodes.

8.4.2 Resistive Load Drive

When driving a resistive load, a pull-up resistor is needed in order for ULN2003B to sink current and for there to be a logic high level. The COM pin can be left floating for these applications.

9 Application and Implementation

NOTE

Information in the following applications sections is not part of the TI component specification, and TI does not warrant its accuracy or completeness. TI's customers are responsible for determining suitability of components for their purposes. Customers should validate and test their design implementation to confirm system functionality.

9.1 Application Information

ULN2003B will typically be used to drive a high voltage and/or current peripheral from an MCU or logic device that cannot tolerate these conditions. The following design is a common application of ULN2003B, driving inductive loads. This includes motors, solenoids and relays. Figure 23 is a typical block diagram representation of this application.

9.2 Typical Application

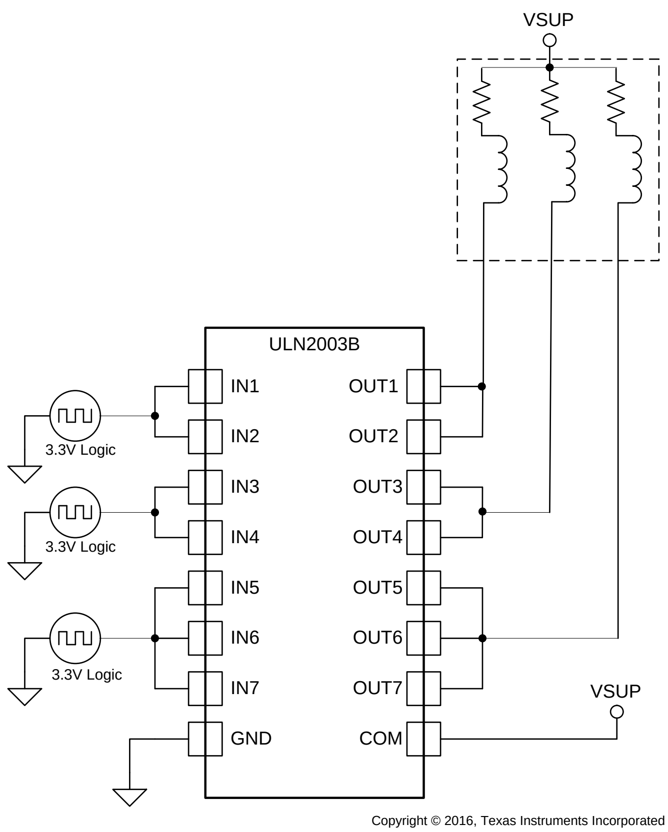


Figure 23. ULN2003B as Inductive Load Driver

Typical Application (continued)

9.2.1 Design Requirements

For this design example, use the parameters listed in Table 1 as the input parameters.

Table 1. Design Parameters

DESIGN PARAMETER (1)	EXAMPLE VALUE
GPIO Voltage	3.3 V or 5 V
Coil Supply Voltage	12 V to 48 V
Number of Channels	7
Output Current (R_{COIL})	20 mA to 300 mA per channel (See Figure 5)
Duty Cycle	See Figure 6 to Figure 14

(1) These test conditions can not be run simultaneously.

9.2.2 Detailed Design Procedure

When using ULN2003B in a coil driving application, determine the following:

- Input Voltage Range
- Temperature Range
- Output and Drive Current
- Power Dissipation

9.2.2.1 Drive Current

The coil current is determined by the coil voltage (VSUP), coil resistance and output low voltage (V_{OL} or $V_{CE(SAT)}$).

$$I_{COIL} = (V_{SUP} – V_{CE(SAT)}) / R_{COIL} \tag{1}$$

9.2.2.2 Output Low Voltage

The output low voltage (V_{OL}) is the same thing as $V_{CE(SAT)}$ and can be determined by, Figure 1, Figure 2, or Figure 4.

9.2.2.3 Power Dissipation and Temperature

The number of coils driven is dependent on the coil current and on-chip power dissipation. The number of coils driven can be determined by Figure 6 or Figure 7.

For a more accurate determination of number of coils possible, use Equation 2 to calculate ULN2003B on-chip power dissipation P_D:

$$P_D = \sum_{i=1}^{N} V_{OLi} \times I_{Li}$$

where

- N is the number of channels active together.
- V_{OLi} is the OUT_i pin voltage for the load current I_{Li}. This is the same as $V_{CE(SAT)}$ (2)

In order to guarantee reliability of ULN2003B and the system the on-chip power dissipation must be lower that or equal to the maximum allowable power dissipation ($PD_{(MAX)}$) dictated by Equation 3.

$$PD_{(MAX)} = \left(T_{J(MAX)} - T_A\right) / \theta_{JA}$$

where

- $T_{J(MAX)}$ is the target maximum junction temperature.
- T_A is the operating ambient temperature.
- θ_{JA} is the package junction to ambient thermal resistance. (3)

TI recommends to limit ULN2003B IC’s die junction temperature to less than 125°C. The IC junction temperature is directly proportional to the on-chip power dissipation.

9.2.3 Application Curves

The following curves were generated with ULN2003B driving an OMRON G5NB relay – V_{in} = 5.0V; V_{sup}= 12 V and R_{COIL}= 2.8 kΩ

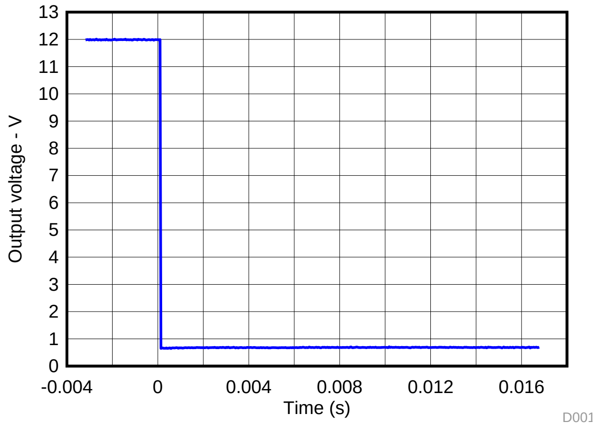


Figure 24. Output Response With Activation of Coil (Turn On)

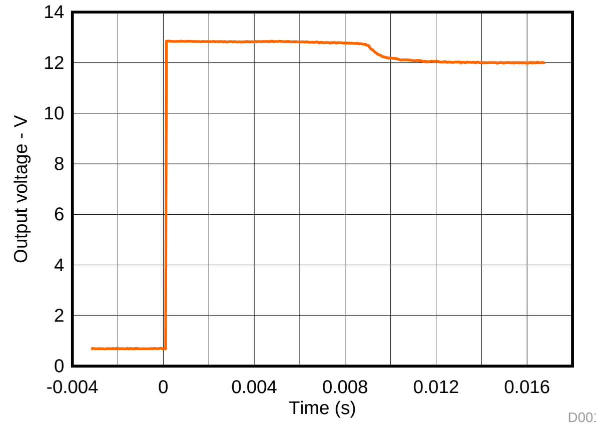


Figure 25. Output Response With De-activation of Coil (Turn Off)

10 Power Supply Recommendations

This part does not need a power supply; however, the COM pin is typically tied to the system power supply. When this is the case, it is very important to make sure that the output voltage does not exceed the COM pin voltage. This will heavily forward bias the fly-back diodes and cause a large current to flow into COM, potentially damaging the on-chip metal or over-heating the part.

11 Layout

11.1 Layout Guidelines

Thin traces can be used on the input due to the low current logic that is typically used to drive UNL2003B. Care must be taken to separate the input channels as much as possible, as to eliminate cross-talk. Thick traces are recommended for the output, in order to drive whatever high currents that may be needed. Wire thickness can be determined by the trace material's current density and desired drive current.

Since all of the channels currents return to a common emitter, it is best to size that trace width to be very wide. Some applications require up to 2.5 A.

11.2 Layout Example

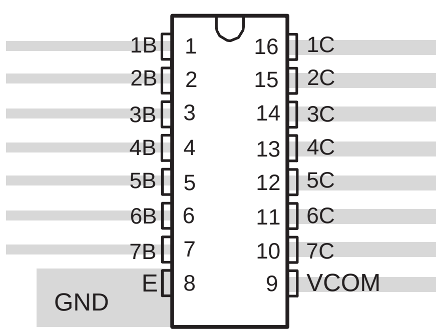


Figure 26. Package Layout

12 Device and Documentation Support

12.1 Receiving Notification of Documentation Updates

To receive notification of documentation updates, navigate to the device product folder on ti.com. In the upper right corner, click on *Alert me* to register and receive a weekly digest of any product information that has changed. For change details, review the revision history included in any revised document.

12.2 Community Resources

The following links connect to TI community resources. Linked contents are provided "AS IS" by the respective contributors. They do not constitute TI specifications and do not necessarily reflect TI's views; see TI's Terms of Use.

TI E2E™ Online Community ***TI's Engineer-to-Engineer (E2E) Community.*** Created to foster collaboration among engineers. At e2e.ti.com, you can ask questions, share knowledge, explore ideas and help solve problems with fellow engineers.

Design Support ***TI's Design Support*** Quickly find helpful E2E forums along with design support tools and contact information for technical support.

12.3 Trademarks

E2E is a trademark of Texas Instruments.
All other trademarks are the property of their respective owners.

12.4 Electrostatic Discharge Caution

This integrated circuit can be damaged by ESD. Texas Instruments recommends that all integrated circuits be handled with appropriate precautions. Failure to observe proper handling and installation procedures can cause damage.

ESD damage can range from subtle performance degradation to complete device failure. Precision integrated circuits may be more susceptible to damage because very small parametric changes could cause the device not to meet its published specifications.

12.5 Glossary

SLYZ022 — *TI Glossary*.
This glossary lists and explains terms, acronyms, and definitions.

13 Mechanical, Packaging, and Orderable Information

The following pages include mechanical, packaging, and orderable information. This information is the most current data available for the designated devices. This data is subject to change without notice and revision of this document. For browser-based versions of this data sheet, refer to the left-hand navigation.

PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead finish/ Ball material (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
ULN2003BDR	OBSOLETE	SOIC	D	16		TBD	Call TI	Call TI	-40 to 105	ULN2003B	
ULN2003BN	OBSOLETE	PDIP	N	16		TBD	Call TI	Call TI	-40 to 105	ULN2003BN	
ULN2003BPWR	OBSOLETE	TSSOP	PW	16		TBD	Call TI	Call TI	-40 to 105	UN2003B	

(1) The marketing status values are defined as follows:
ACTIVE: Product device recommended for new designs.
LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
PREVIEW: Device has been announced but is not in production. Samples may or may not be available.
OBSOLETE: TI has discontinued the production of the device.

(2) **RoHS:** TI defines "RoHS" to mean semiconductor products that are compliant with the current EU RoHS requirements for all 10 RoHS substances, including the requirement that RoHS substance do not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, "RoHS" products are suitable for use in specified lead-free processes. TI may reference these types of products as "Pb-Free".
RoHS Exempt: TI defines "RoHS Exempt" to mean products that contain lead but are compliant with EU RoHS pursuant to a specific EU RoHS exemption.
Green: TI defines "Green" to mean the content of Chlorine (Cl) and Bromine (Br) based flame retardants meet JS709B low halogen requirements of <=1000ppm threshold. Antimony trioxide based flame retardants must also meet the <=1000ppm threshold requirement.

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

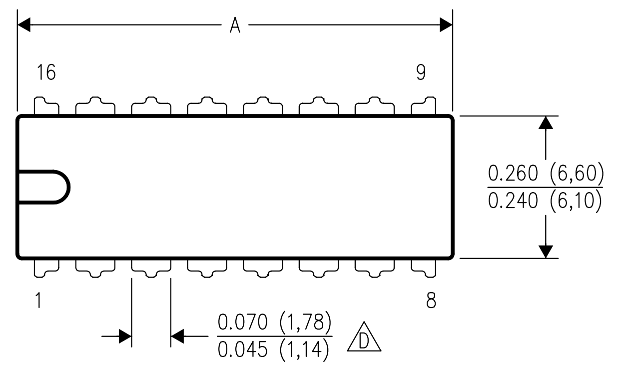
(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

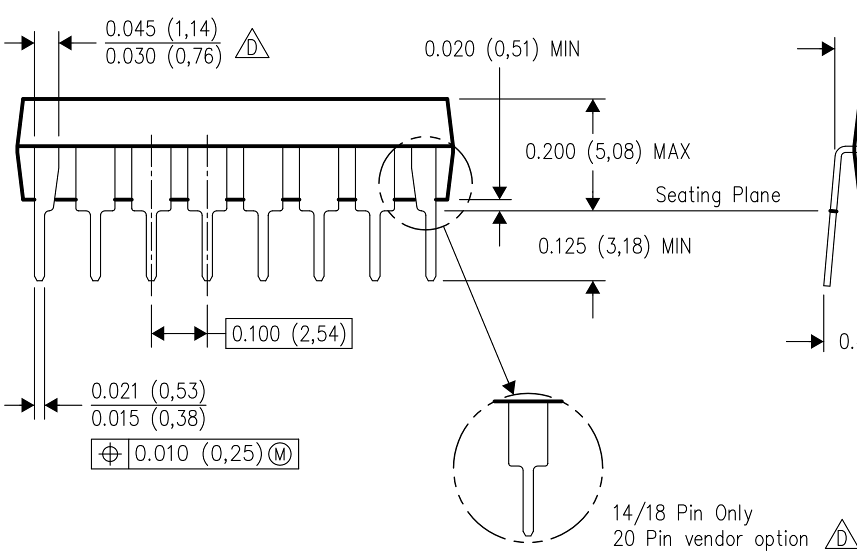
(6) Lead finish/Ball material - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

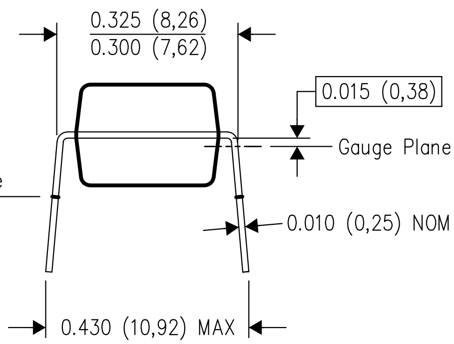
N (R–PDIP–T**) PLASTIC DUAL–IN–LINE PACKAGE

16 PINS SHOWN



PINS ** / DIM	14	16	18	20
A MAX	0.775 (19,69)	0.775 (19,69)	0.920 (23,37)	1.060 (26,92)
A MIN	0.745 (18,92)	0.745 (18,92)	0.850 (21,59)	0.940 (23,88)
C MS–001 VARIATION	AA	BB	AC	AD

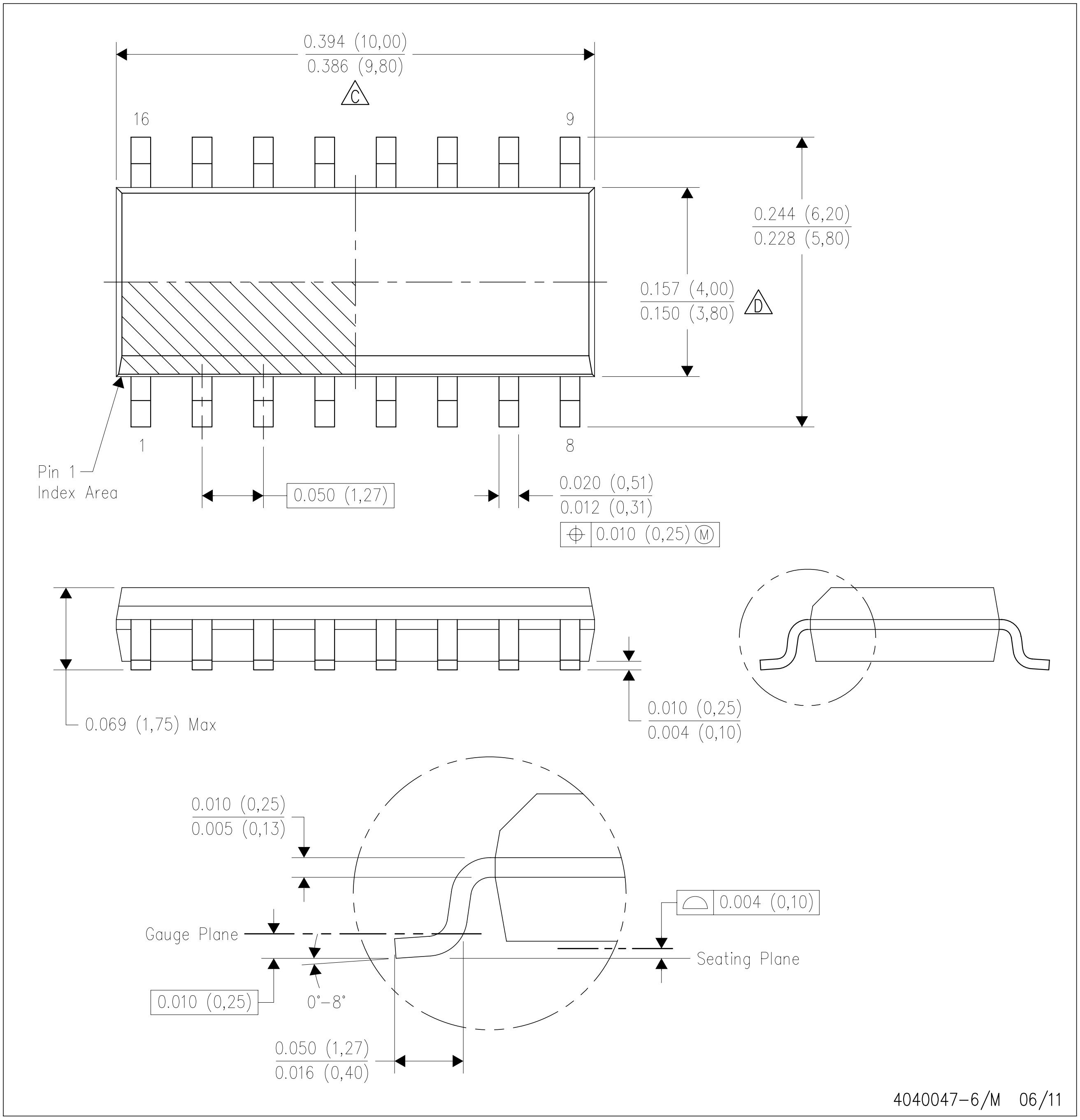




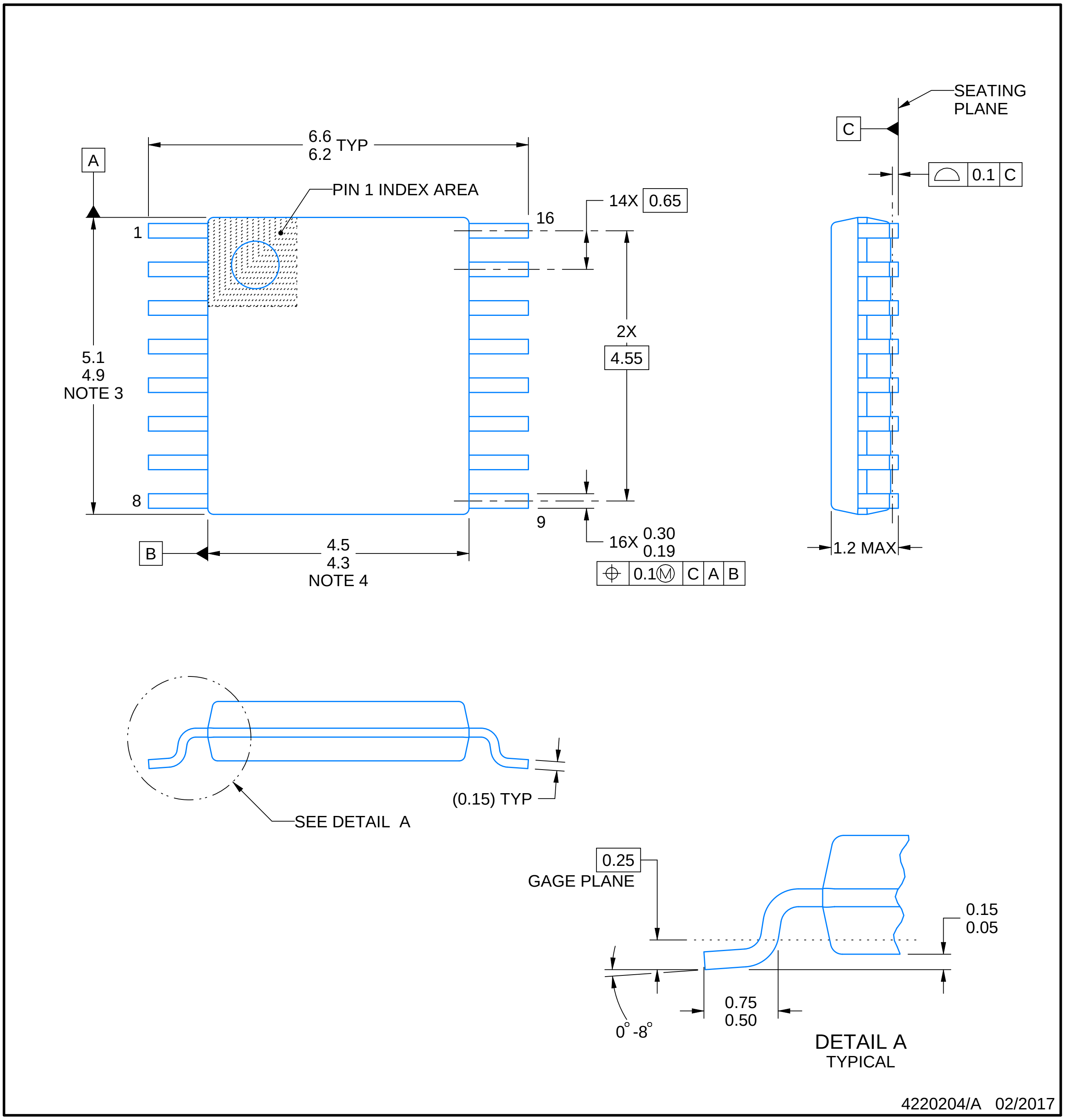
4040049/E 12/2002

NOTES:
A. All linear dimensions are in inches (millimeters).
B. This drawing is subject to change without notice.
C. Falls within JEDEC MS–001, except 18 and 20 pin minimum body length (Dim A).
D. The 20 pin end lead shoulder width is a vendor option, either half or full width.

D (R–PDSO–G16) PLASTIC SMALL OUTLINE



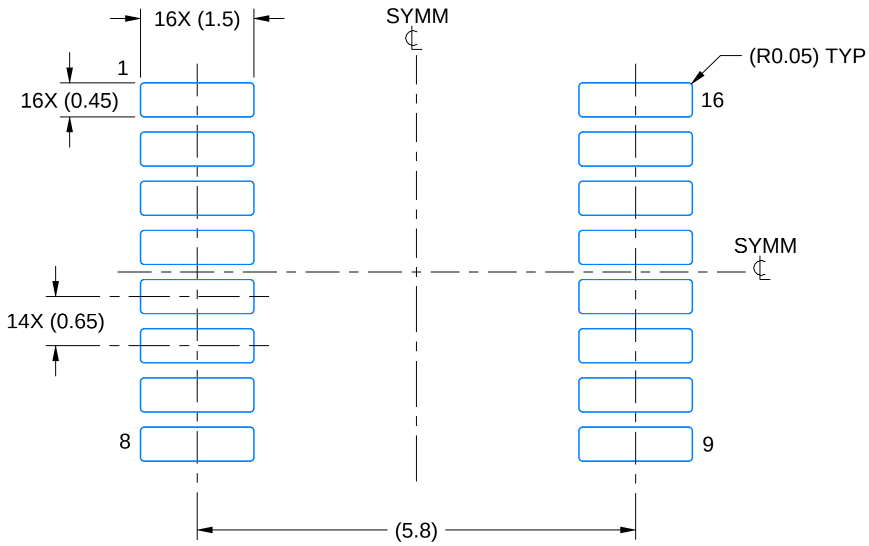
NOTES:
A. All linear dimensions are in inches (millimeters).
B. This drawing is subject to change without notice.
C. Body length does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.006 (0,15) each side.
D. Body width does not include interlead flash. Interlead flash shall not exceed 0.017 (0,43) each side.
E. Reference JEDEC MS–012 variation AC.



4220204/A 02/2017

NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.15 mm per side.
4. This dimension does not include interlead flash. Interlead flash shall not exceed 0.25 mm per side.
5. Reference JEDEC registration MO-153.



LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE: 10X

NON-SOLDER MASK DEFINED (PREFERRED)

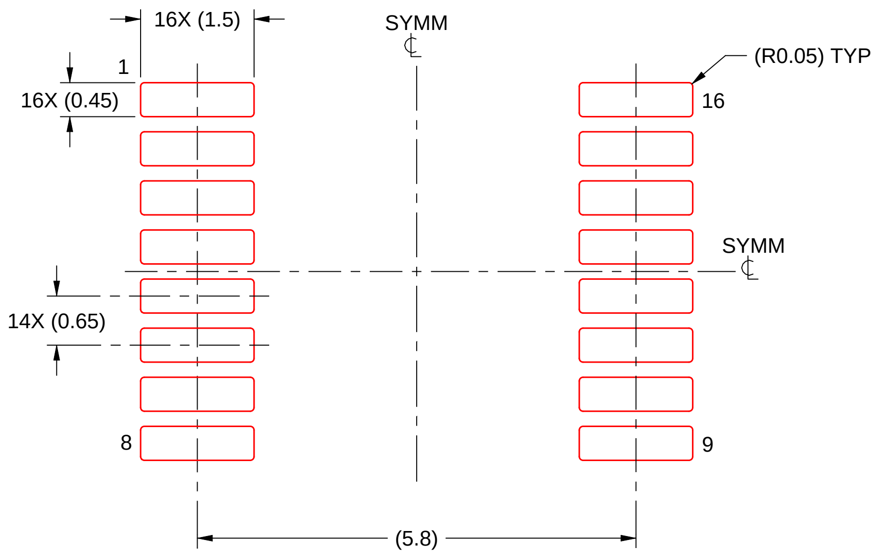
SOLDER MASK DEFINED

SOLDER MASK DETAILS

4220204/A 02/2017

NOTES: (continued)

6. Publication IPC-7351 may have alternate designs.
7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.



SOLDER PASTE EXAMPLE
BASED ON 0.125 mm THICK STENCIL
SCALE: 10X

4220204/A 02/2017

NOTES: (continued)

8. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
9. Board assembly site may have different recommendations for stencil design.

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