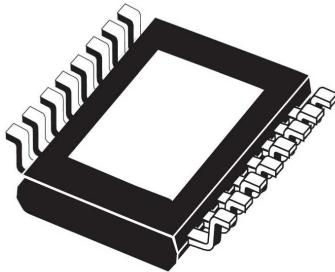


Single channel high-side driver with Current Sense analog feedback for automotive applications



PowerSSO-16

Features

| Description | Parameter | Value |
|----------------------------------------|-------------------|-----------|
| Max. transient supply voltage | V _{CC} | 36 V |
| Operating voltage range | V _{CC} | 4 to 28 V |
| Typ. on-state resistance (per channel) | R _{ON} | 4.2 mΩ |
| Current limitation (typ.) | I _{LIMH} | 108 A |
| Standby current (max.) | I _{STBY} | 0.5 μA |

Product status link

[VN9004AJ](#)

Product summary

| | |
|------------|---------------|
| Order code | VN9004AJTR |
| Package | PowerSSO-16 |
| Packing | Tape and reel |

- AEC-Q100 qualified 
- Extreme low voltage operation for deep cold cranking applications (compliant with LV124, revision 2013)
- General
 - Single channel smart high-side driver with current sense analog feedback
 - Very low standby current
 - Compatible with 3 V and 5 V CMOS outputs
- Current sense diagnostic functions
 - Multiplexed analog feedback of: load current with high precision proportional current mirror
 - Overload and short to ground (power limitation) indication
 - Thermal shutdown indication
 - OFF-state open-load detection (with external pull-up)
 - Output short to V_{CC} detection
 - Sense enable/disable
- Protections
 - Undervoltage shutdown
 - Overvoltage clamp
 - Load current limitation
 - Self limiting of fast thermal transients
 - Configurable latch-off on overtemperature or power limitation with dedicated fault reset pin
 - Loss of ground and loss of V_{CC}
 - Reverse battery through self turn-on
 - Electrostatic discharge protection

Applications

- Specially intended for Automotive smart power distribution
- Glow plugs, heating systems, DC motors, relay replacement and high power resistive and inductive actuators

Description

The VN9004AJ is a single channel high-side driver manufactured using ST proprietary VIPower M0-9 technology and housed in a PowerSSO-16 package. The device is designed to drive 12 V automotive grounded loads through a 3 V and 5 V CMOS-compatible interface, providing protection and diagnostics.

The device integrates advanced protective functions such as load current limitation, overload active management by power limitation and overtemperature shutdown with configurable latch-off.

A FaultRST pin unlatches the output in case of fault or disables the latch-off functionality.

A dedicated multifunction multiplexed analog output pin delivers sophisticated diagnostic functions including high precision proportional load current sense, supply voltage feedback and chip temperature sense, in addition to the detection of overload and short circuit to ground, short to V_{CC} and OFF-state open-load.

1 Block diagram and pin description

Figure 1. Block diagram

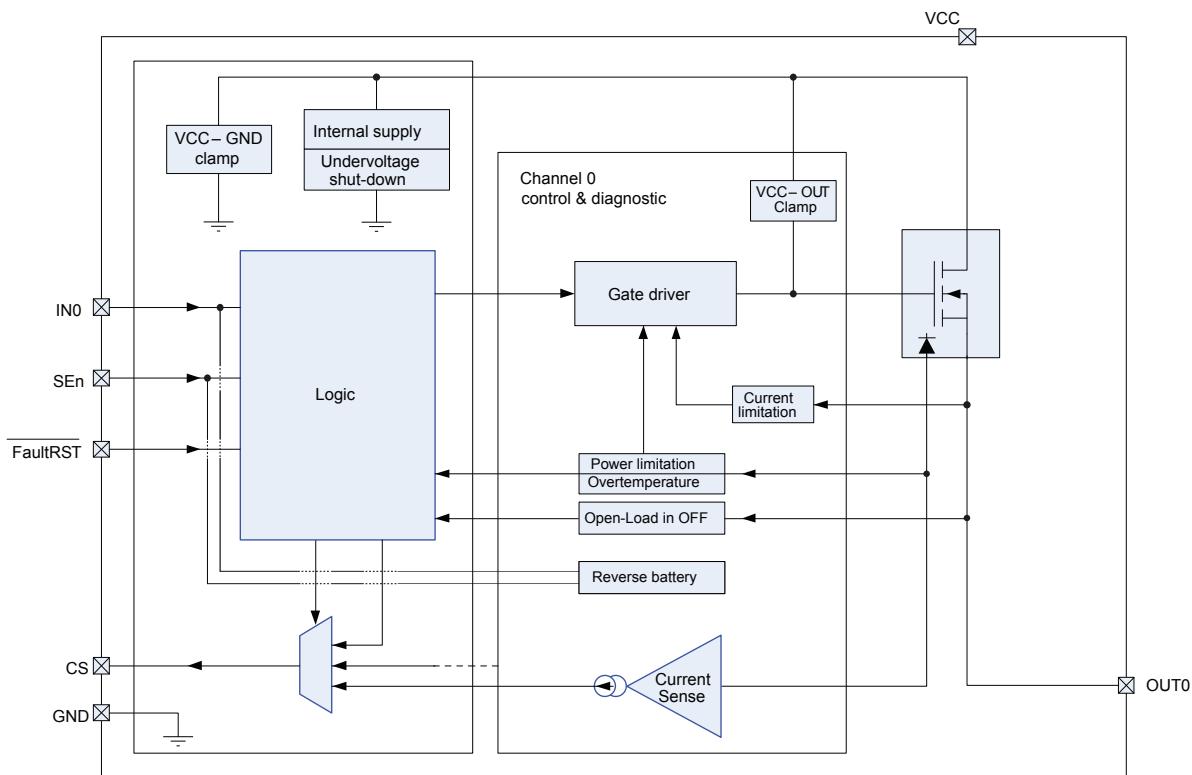
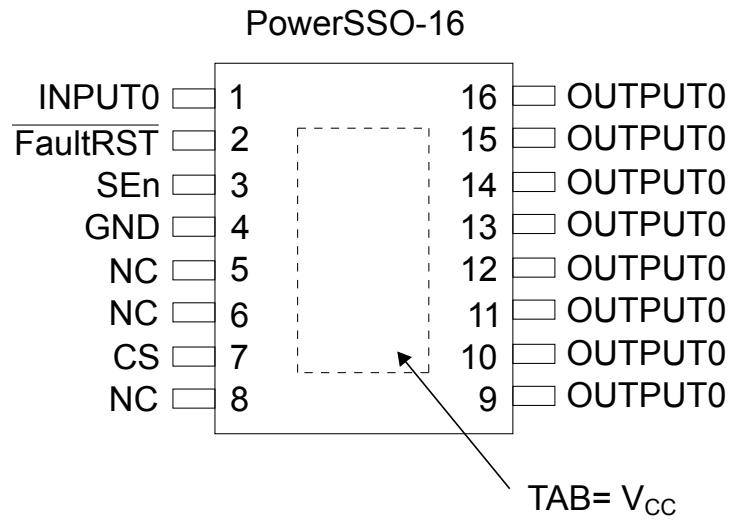


Table 1. Pin functions

| Name | Function |
|---------------------------|--------------------------------------------------------------------------------------------------------------------------------------------------------|
| V_{CC} | Battery connection. |
| OUTPUT₀ | Power outputs. |
| GND | Ground connection. Must be reverse battery protected by an external diode / resistor network. |
| INPUT₀ | Voltage controlled input pin with hysteresis, compatible with 3 V and 5 V CMOS outputs. It controls output switch state. |
| CS | Multiplexed analog sense output pin; it delivers a current proportional to the selected load current. |
| SEn | Active high compatible with 3 V and 5 V CMOS outputs pin; it enables the CS diagnostic pin. |
| FaultRST | Active low compatible with 3 V and 5 V CMOS outputs pin; it unlatches the output in case of fault; If kept low, sets the outputs in auto-restart mode. |

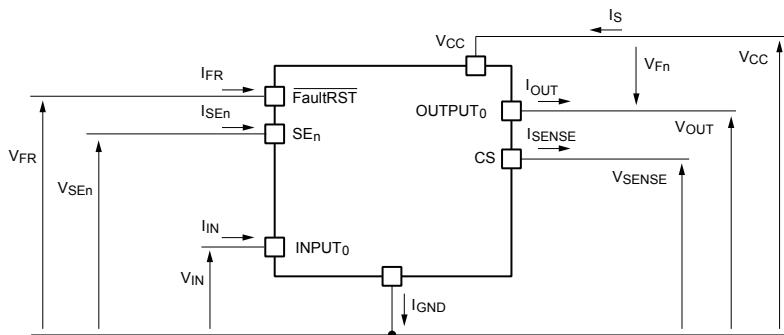
Figure 2. Configuration diagram (top view)**Table 2.** Suggested connections for unused and not connected pins

| Connection / pin | CS | NC | Output | Input | SEn, <u>FaultRST</u> |
|------------------|-----------------------|----|------------------|------------------------|------------------------|
| Floating | Not allowed | X | X ⁽¹⁾ | X | X |
| To ground | Through 1 kΩ resistor | X | Not allowed | Through 15 kΩ resistor | Through 15 kΩ resistor |

1. X: do not care.

2 Electrical specification

Figure 3. Current and voltage conventions



GADG1605171029PS

2.1 Absolute maximum ratings

Stressing the device above the rating listed in Table 3. **Absolute maximum ratings** may cause permanent damage to the device. These are stress ratings only and operation of the device at these or any other conditions above those indicated in the operating sections of this specification is not implied. Exposure to the conditions in table below for extended periods may affect device reliability.

Table 3. Absolute maximum ratings

| Symbol | Parameter | Value | Unit |
|--------------------|----------------------------------------------------------------------|--------------------|------|
| V _{CC} | DC supply voltage | 36 | V |
| -V _{CC} | Reverse DC supply voltage | 0.3 | |
| V _{CCJS} | Maximum jump start voltage for single pulse short circuit protection | 28 | V |
| -I _{GND} | DC reverse ground pin current | 200 | mA |
| I _{OUT} | OUTPUT ₀ DC output current | Internally limited | A |
| -I _{OUT} | Reverse DC output current | 31 | |
| I _{IN} | INPUT ₀ DC input current | -1 to 10 | mA |
| I _{SEN} | SEn DC input current | -1 to 3 | mA |
| I _{FR} | FaultRST DC input current | -1 to 10 | mA |
| I _{SENSE} | CS pin DC output current ($V_{GND} = V_{CC}$ and $V_{SENSE} < 0$ V) | +10 | mA |
| | CS pin DC output current in reverse ($V_{CC} < 0$ V) | -20 | |
| E _{MAX} | Maximum switching energy (single pulse) ($T_{Jstart} = 150$ °C) | 75 | mJ |
| V _{ESD} | Electrostatic discharge (JEDEC 22A-114F) | 2000 | |
| | • INPUT ₀ | 2000 | |
| | • CS | 2000 | V |
| | • SEn, FaultRST | 4000 | |
| | • OUTPUT ₀ | 4000 | |
| V _{ESD} | Charge device model (CDM-AEC-Q100-011) | 750 | V |
| T _J | Junction operating temperature | -40 to 150 | °C |
| T _{stg} | Storage temperature | -55 to 150 | °C |

2.2 Thermal data

Table 4. Thermal data

| Symbol | Parameter | Typ. value | Unit |
|------------|--------------------------------------------------------------------------|------------|------|
| R_{thJB} | Thermal resistance, junction-to-board (JEDEC JESD 51-8) ⁽¹⁾ | 5.9 | °C/W |
| R_{thJA} | Thermal resistance, junction-to-ambient (JEDEC JESD 51-2) ⁽²⁾ | 52.2 | °C/W |
| | Thermal resistance, junction-to-ambient (JEDEC JESD 51-2) ⁽¹⁾ | 19.2 | |

1. Device mounted on four-layers 2s2p PCB.
2. Device mounted on two-layers 2s0p PCB with 2 cm² heatsink copper trace.

2.3 Main electrical characteristics

$7 \text{ V} < V_{CC} < 28 \text{ V}$, $-40^\circ\text{C} < T_J < 150^\circ\text{C}$, unless otherwise specified.

All typical values refer to $V_{CC} = 13 \text{ V}$, $T_J = 25^\circ\text{C}$, unless otherwise specified.

Table 5. Power section

| Symbol | Parameter | Test conditions | Min. | Typ. | Max. | Unit |
|----------------|---------------------------------------------------------------------|-------------------------------------------------------------------------------------------------------------------------------------|------|------|------|------|
| V_{CC} | Operating supply voltage | | 4 | 13 | 28 | V |
| V_{USD} | Undervoltage shutdown | | | 2.1 | 2.7 | V |
| $V_{USDReset}$ | Undervoltage shutdown reset | | | | 4.5 | V |
| $V_{USDhyst}$ | Undervoltage shutdown hysteresis | | | 0.15 | | V |
| R_{ON} | On-state resistance | $I_{OUT} = 15 \text{ A}$, $T_J = 25^\circ\text{C}$ | | 4.2 | | mΩ |
| | | $I_{OUT} = 15 \text{ A}$, $T_J = 150^\circ\text{C}$ | | | 9.2 | |
| | | $I_{OUT} = 15 \text{ A}$, $V_{CC} = 4 \text{ V}$, $T_J = 25^\circ\text{C}$ | | | 7.2 | |
| | | $I_{OUT} = 4 \text{ A}$, $V_{CC} = 2.7 \text{ V}$, V_{CC} decreasing | | | 25.2 | |
| R_{ON_Rev} | R_{DSon} in reverse battery condition | $V_{CC} = -13 \text{ V}$, $I_{OUT} = -15 \text{ A}$, $T_J = 25^\circ\text{C}$ | | 4.2 | | mΩ |
| V_{clamp} | Clamp voltage | $I_S = 20 \text{ mA}$, $25^\circ\text{C} < T_J < 150^\circ\text{C}$ | 36 | 38 | 45 | V |
| | | $I_S = 20 \text{ mA}$, $T_J = -40^\circ\text{C}$ | 36 | | | |
| I_{STBY} | Supply current in standby at $V_{CC} = 13 \text{ V}^{(1)}$ | $V_{CC} = 13 \text{ V}$, $T_J = 25^\circ\text{C}$, $V_{IN} = V_{OUT} = V_{FR} = V_{SEN} = 0 \text{ V}$, | | | 0.5 | μA |
| | | $V_{CC} = 13 \text{ V}$, $T_J = 85^\circ\text{C}^{(2)}$ $V_{IN} = V_{OUT} = V_{FR} = V_{SEN} = 0 \text{ V}$, | | | 0.5 | |
| | | $V_{CC} = 13 \text{ V}$, $T_J = 125^\circ\text{C}$ $V_{IN} = V_{OUT} = V_{FR} = V_{SEN} = 0 \text{ V}$, | | | 3 | |
| t_{D_STBY} | Standby mode blanking time | $V_{CC} = 13 \text{ V}$, $V_{IN} = V_{OUT} = V_{FR} = 0 \text{ V}$, $V_{SEN} = 5 \text{ V}$ to 0 V | 60 | 260 | 550 | μs |
| $I_{S(ON)}$ | Supply current at $V_{CC} = 13 \text{ V}$ | $V_{CC} = 13 \text{ V}$, $V_{SEN} = V_{FR} = 0 \text{ V}$, $V_{IN0} = 5 \text{ V}$, $I_{OUT0} = 0 \text{ A}$ | | 3.5 | 4.5 | mA |
| $I_{GND(ON)}$ | Control stage current consumption in ON-state. All channels active. | $V_{CC} = 13 \text{ V}$, $V_{SEN} = 5 \text{ V}$, $V_{FR} = 0 \text{ V}$, $V_{IN0} = 5 \text{ V}$, $I_{OUT0} = 15 \text{ A}$ | | | 6 | mA |
| $I_{L(off)}$ | Off-state output current at $V_{CC} = 13 \text{ V}^{(1)}$ | $V_{IN} = V_{OUT} = 0 \text{ V}$, $V_{CC} = 13 \text{ V}$, $T_J = 25^\circ\text{C}$ | 0 | 0.01 | 0.5 | μA |

| Symbol | Parameter | Test conditions | Min. | Typ. | Max. | Unit |
|---------------------|--------------------------------------------------------------|----------------------------------------------------------------------------------|------|------|------|---------------|
| $I_{L(\text{off})}$ | Off-state output current at $V_{CC} = 13 \text{ V}^{(1)}$ | $V_{IN} = V_{OUT} = 0 \text{ V}, V_{CC} = 13 \text{ V}, T_J = 125^\circ\text{C}$ | 0 | | 3 | μA |
| V_F | Output - V_{CC} diode voltage at $T_J = 150^\circ\text{C}$ | $I_{OUT} = -15 \text{ A}, T_J = 150^\circ\text{C}$ | | | 0.7 | V |

1. PowerMOS leakage included.
2. Parameter specified by design, not subjected to production test.

Table 6. Switching

| $V_{CC} = 13 \text{ V}, -40^\circ\text{C} < T_J < 150^\circ\text{C}$, unless otherwise specified | | | | | | |
|---------------------------------------------------------------------------------------------------|----------------------------------------------------|---------------------|------|------|--------------------|------------------------|
| Symbol | Parameter | Test conditions | Min. | Typ. | Max. | Unit |
| $t_{d(on)}^{(1)}$ | Turn-on delay time at $T_J = 25^\circ\text{C}$ | $R_L = 0.87 \Omega$ | 10 | 30 | 120 | μs |
| $t_{d(off)}^{(1)}$ | Turn-off delay time at $T_J = 25^\circ\text{C}$ | $R_L = 0.87 \Omega$ | 10 | 30 | 100 | μs |
| $(dV_{OUT}/dt)_{on}^{(1)}$ | Turn-on voltage slope at $T_J = 25^\circ\text{C}$ | $R_L = 0.87 \Omega$ | 0.1 | 0.4 | 0.7 | $\text{V}/\mu\text{s}$ |
| $(dV_{OUT}/dt)_{off}^{(1)}$ | Turn-off voltage slope at $T_J = 25^\circ\text{C}$ | $R_L = 0.87 \Omega$ | 0.1 | 0.4 | 0.7 | $\text{V}/\mu\text{s}$ |
| W_{ON} | Switching energy losses at turn-on (t_{won}) | $R_L = 0.87 \Omega$ | — | 1.9 | 3.7 ⁽²⁾ | mJ |
| W_{OFF} | Switching energy losses at turn-off (t_{woff}) | $R_L = 0.87 \Omega$ | — | 1.8 | 2.5 ⁽²⁾ | mJ |
| $t_{SKew}^{(1)}$ | Differential Pulse skew ($t_{PHL} - t_{PLH}$) | $R_L = 0.87 \Omega$ | -70 | -20 | 30 | μs |

1. See Figure 4. Switching time and pulse skew.
2. Parameter guaranteed by design and characterization, not subjected to production test.

Table 7. Logic inputs

| $7 \text{ V} < V_{CC} < 28 \text{ V}, -40^\circ\text{C} < T_J < 150^\circ\text{C}$ | | | | | | |
|------------------------------------------------------------------------------------|--------------------------|--------------------------|------|------|------|---------------|
| Symbol | Parameter | Test conditions | Min. | Typ. | Max. | Unit |
| INPUT ₀ characteristics | | | | | | |
| V_{IL} | Input low level voltage | | | | 0.9 | V |
| I_{IL} | Low level input current | $V_{IN} = 0.9 \text{ V}$ | 1 | | | μA |
| V_{IH} | Input high level voltage | | 2.1 | | | V |
| I_{IH} | High level input current | $V_{IN} = 2.1 \text{ V}$ | | | 10 | μA |
| $V_{I(hyst)}$ | Input hysteresis voltage | | 0.2 | | | V |
| V_{ICL} | Input clamp voltage | $I_{IN} = 1 \text{ mA}$ | 6 | | 8.5 | V |
| | | $I_{IN} = -1 \text{ mA}$ | | -0.7 | | |
| FaultRST characteristics | | | | | | |
| V_{FRL} | Input low level voltage | | | | 0.9 | V |
| I_{FRL} | Low level input current | $V_{IN} = 0.9 \text{ V}$ | 1 | | | μA |
| V_{FRH} | Input high level voltage | | 2.1 | | | V |
| I_{FRH} | High level input current | $V_{IN} = 2.1 \text{ V}$ | | | 10 | μA |
| $V_{FR(hyst)}$ | Input hysteresis voltage | | 0.2 | | | V |
| V_{FRCL} | Input clamp voltage | $I_{IN} = 1 \text{ mA}$ | 6 | | 8.5 | V |
| | | $I_{IN} = -1 \text{ mA}$ | | -0.7 | | |
| SEn characteristics ($7 \text{ V} < V_{CC} < 18 \text{ V}$) | | | | | | |

| 7 V < V _{CC} < 28 V, -40 °C < T _J < 150 °C | | | | | | |
|----------------------------------------------------------------|--------------------------|--------------------------|------|------|------|------|
| Symbol | Parameter | Test conditions | Min. | Typ. | Max. | Unit |
| V _{SEN} L | Input low level voltage | | | | 0.9 | V |
| I _{SEN} L | Low level input current | V _{IN} = 0.9 V | 1 | | | µA |
| V _{SEN} H | Input high level voltage | | 2.1 | | | V |
| I _{SEN} H | High level input current | V _{IN} = 2.1 V | | | 10 | µA |
| V _{SEN(hyst)} | Input hysteresis voltage | | 0.2 | | | V |
| V _{SEN} CL | Input clamp voltage | I _{SEN} = 1 mA | 9 | | 12 | V |
| | | I _{SEN} = -1 mA | | -0.7 | | |

Table 8. Protections

| 7 V < V _{CC} < 18 V, -40°C < T _J < 150°C | | | | | | |
|--------------------------------------------------------------|-------------------------------------------------------------------------|------------------------------------------------------------------------------|----------------------|----------------------|----------------------|------|
| Symbol | Parameter | Test conditions | Min. | Typ. | Max. | Unit |
| I _{LIMH} ⁽¹⁾ | DC short-circuit current | V _{CC} = 16 V, T _J = -40°C | -15% | 120 | 15% | A |
| | | V _{CC} = 16 V, T _J = 150°C | -15% | 91 | 15% | |
| I _{LIMH2} ⁽²⁾ | | V _{CC} = 19 V, T _J = -40°C | -15% | 90 | 15% | |
| | | V _{CC} = 19 V, T _J = 150°C | -15% | 69 | 15% | |
| I _{LIMH} at 22 V | | V _{CC} = 22 V, T _J = 25°C | | 35 | | |
| T _{TSD} | Shutdown temperature | | 150 | 175 | 210 | °C |
| | Shutdown temperature (V _{CC} decreasing) | V _{CC} = 2.7 V | 140 | | | |
| T _{RS} ⁽³⁾ | Thermal reset of fault diagnostic indication | V _{FR} = 0 V, V _{SEN} = 5 V | 135 | | | °C |
| T _{HYST} | Thermal hysteresis (T _{TSD} - T _{RS}) ⁽³⁾ | | | 7 | | °C |
| ΔT _{J_SD} | Dynamic temperature | V _{CC} = 19 V | | 55 | | K |
| | | V _{CC} = 16 V | | 80 | | |
| t _{LATCH_RST} | Fault reset time for output unlatch ⁽³⁾ | V _{FR} = 5 V to 0 V; V _{SEN} = 5 V, V _{IN0} = 5 V | 3 | 10 | 20 | µs |
| t _{D_Restart} | Latch-OFF delay time before automatic restart | | | 50 | 75 | ms |
| V _{DEMAG} | Turn-off output voltage clamp | I _{OUT} = 2 A; L = 6 mH, T _J = -40°C | V _{CC} - 36 | | | V |
| | | I _{OUT} = 2 A; L = 6 mH, T _J = 25°C to 150°C | V _{CC} - 36 | V _{CC} - 38 | V _{CC} - 45 | |

1. I_{LIMH}, guaranteed between 7 V and 16 V, -40°C < T_J < 150°C.
2. I_{LIMH2}, guaranteed between 16 V and 19 V, -40°C < T_J < 150°C.
3. Specified by design and evaluated by characterization, not tested in production.

Table 9. CurrentSense

| 7 V < V _{CC} < 18 V; -40 °C < T _J < 150 °C | | | | | | |
|----------------------------------------------------------------|------------------|----------------------------------------------------|------|------|------|------|
| Symbol | Parameter | Test conditions | Min. | Typ. | Max. | Unit |
| V _{SENSE_CL} | CS clamp voltage | V _{SEN} = 0 V; I _{SENSE} = 1 mA | -9 | -8 | -7 | V |
| | | V _{SEN} = 0 V; I _{SENSE} = -1 mA | | 7 | | |

| 7 V < V _{CC} < 18 V; -40 °C < T _J < 150 °C | | | | | | |
|-------------------------------------------------------------------|-------------------------------------------------|-----------------------------------------------------------------------------------------------------------------------------------------------------------|------|-------|------|------|
| Symbol | Parameter | Test conditions | Min. | Typ. | Max. | Unit |
| CurrentSense characteristics | | | | | | |
| K _{LED} | I _{OUT} /I _{SENSE} | I _{OUT} = 0.25 A; V _{SENSE} = 0.5 V; V _{SEN} = 5 V | -35% | 19050 | +35% | % |
| dK _{LED} /K _{LED} ⁽¹⁾ ⁽²⁾ | Current sense ratio drift | I _{OUT} = 0.25 A; V _{SENSE} = 0.5 V; V _{SEN} = 5 V | -25 | | 25 | % |
| K ₀ | I _{OUT} /I _{SENSE} | I _{OUT} = 1.8 A; V _{SENSE} = 0.5 V; V _{SEN} = 5 V | -20% | 19050 | 20% | % |
| dK ₀ /K ₀ ⁽¹⁾ ⁽²⁾ | Current sense ratio drift | I _{OUT} = 1.8 A; V _{SENSE} = 0.5 V; V _{SEN} = 5 V | -15 | | 15 | % |
| K ₁ | I _{OUT} /I _{SENSE} | I _{OUT} = 10 A; V _{SENSE} = 3.5 V; V _{SEN} = 5 V | -7% | 19050 | 7% | % |
| dK ₁ /K ₁ ⁽¹⁾ ⁽²⁾ | Current sense ratio drift | I _{OUT} = 10 A; V _{SENSE} = 3.5 V; V _{SEN} = 5 V | -7 | | 7 | % |
| K ₂ | I _{OUT} /I _{SENSE} | I _{OUT} = 15 A; V _{SENSE} = 3.5 V; V _{SEN} = 5 V | -7% | 19050 | 7% | % |
| dK ₂ /K ₂ ⁽¹⁾ ⁽²⁾ | Current sense ratio drift | I _{OUT} = 15 A; V _{SENSE} = 3.5 V; V _{SEN} = 5 V | -7 | | 7 | % |
| K ₃ | I _{OUT} /I _{SENSE} | I _{OUT} = 27 A; V _{SENSE} = 3.5 V; V _{SEN} = 5 V | -6% | 19050 | 6% | % |
| dK ₃ /K ₃ ⁽¹⁾ ⁽²⁾ | Current sense ratio drift | I _{OUT} = 27 A; V _{SENSE} = 3.5 V; V _{SEN} = 5 V | -5 | | 5 | % |
| I _{SENSE0} | CurrentSense leakage current | CS disabled: V _{SEN} = 0 V | 0 | | 0.5 | μA |
| | | CS disabled: -1 V < V _{SENSE} < 5 V ⁽¹⁾ | -0.5 | | 0.5 | |
| | | CS enabled: V _{SEN} = 5 V; Channel ON; V _{IN0} = 5 V; I _{OUT0} = 0 A; | 0 | | 3 | |
| | | CS enabled: V _{SEN} = 5 V; Channel OFF; V _{IN0} = 0 V; I _{OUT0} = 0 A | 0 | | 1 | |
| V _{OUT_MSD} ⁽¹⁾ | Output voltage for CS shutdown | V _{SEN} = 5 V; R _{SENSE} = 2.7 kΩ; V _{IN0} = 5 V; I _{OUT0} = 15 A | | 5 | | V |
| V _{SENSE_SAT} | Multisense saturation voltage | V _{CC} = 7 V; R _{SENSE} = 10 kΩ; V _{SEN} = 5 V; V _{IN0} = 5 V; I _{OUT0} = 27 A; T _J = -40°C | 4.8 | | | V |
| I _{SENSE_SAT} ⁽¹⁾ | CS saturation current | V _{CC} = 7 V; V _{SENSE} = 3.5 V; V _{IN0} = 5 V; V _{SEN} = 5 V; T _J = 150°C | 2 | | | mA |
| I _{OUT_SAT} ⁽¹⁾ | Output saturation current | V _{CC} = 7 V; V _{SENSE} = 3.5 V; V _{IN0} = 5 V; V _{SEN} = 5 V; T _J = 150 °C | 37 | | | A |
| OFF-state diagnostic | | | | | | |
| V _{OL} | OFF-state open-load voltage detection threshold | V _{SEN} = 5 V; Ch OFF; V _{IN0} = 0 V; | 2 | 3 | 4 | V |

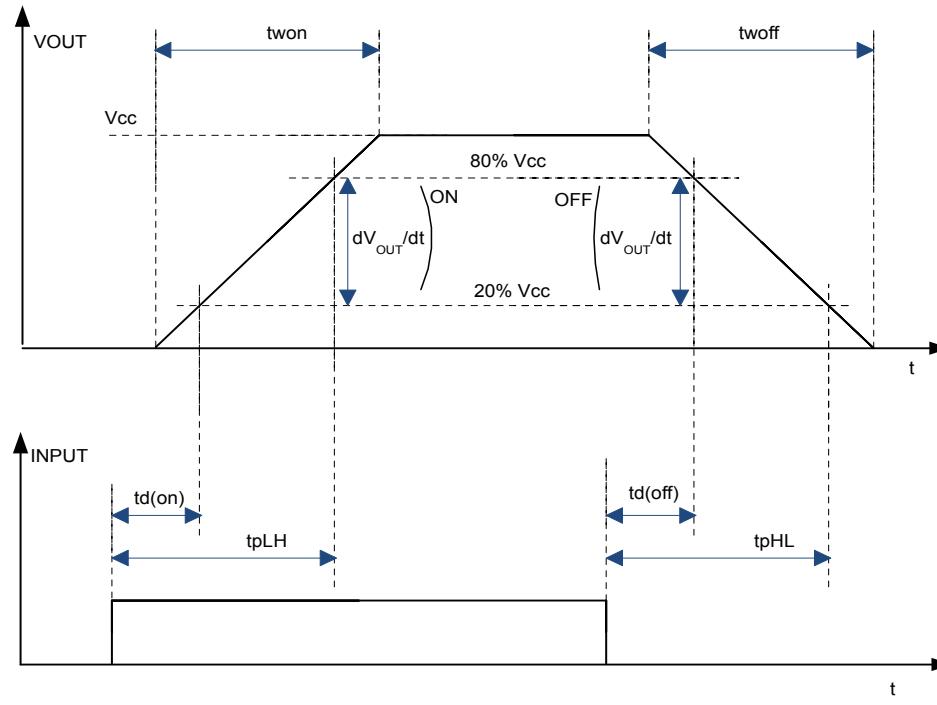
| 7 V < V _{CC} < 18 V; -40 °C < T _J < 150 °C | | | | | | | |
|--------------------------------------------------------------------------------------------------------------------|---------------------------------------------------------------------------------------------------------------------------|--------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|------|------|------|------|----|
| Symbol | Parameter | Test conditions | Min. | Typ. | Max. | Unit | |
| I _{L(off2)} | OFF-state output sink current | V _{IN} = 0 V; V _{OUT} = V _{OL} ; T _J = -40 °C to 125 °C | -150 | -40 | -5 | μA | |
| t _{DSTKON} | OFF-state diagnostic delay time from falling edge of INPUT (see Figure 6. T _{DSTKON}) | V _{SEN} = 5 V; Ch ON to OFF transition; V _{IN0} = 5 V to 0 V; I _{OUT0} = 0 A; V _{OUT} = 4 V | 150 | 260 | 400 | μs | |
| t _{D_OL_V} | Settling time for valid OFF-state open load diagnostic indication from rising edge of SEN | V _{IN} = 0 V; V _{FR} = 0 V; V _{OUT0} = 4 V; V _{SEN} = 0 V to 5 V | | | 60 | μs | |
| t _{D_VOL} | OFF-state diagnostic delay time from rising edge of V _{OUT} | V _{SEN} = 5 V; Ch OFF; V _{IN0} = 0 V; V _{OUT} = 0 V to 4 V | | 5 | 30 | μs | |
| Fault diagnostic feedback (see Table 10. Truth table) | | | | | | | |
| V _{SENSEH} | MultiSense output voltage in fault condition | 13 V < V _{CC} < 18 V; Ch0 in open load; R _{SENSE} = 0.7 kΩ; V _{IN0} = 0 V; V _{SEN} = 5 V; I _{OUT0} = 0 A; V _{OUT0} = 4 V | 5 | | 7.5 | | V |
| | | V _{CC} = 7 V; Ch0 in open load; R _{SENSE} = 0.7 kΩ; V _{IN0} = 0 V; V _{SEN} = 5 V; I _{OUT0} = 0 A; V _{OUT0} = 4 V | 4.3 | | | | |
| I _{SENSEH} | CurrentSense output current in fault condition | 13 V < V _{CC} < 18 V; V _{SENSE} = 5 V; Ch0 in open load; V _{IN0} = 0 V; V _{SEN} = 5 V; I _{OUT0} = 0 A; V _{OUT0} = 4 V | 7 | 8.6 | 12 | | mA |
| | | V _{CC} = 7 V; V _{SENSE} = 5 V; Ch0 in open load; V _{IN0} = 0 V; V _{SEN} = 5 V; I _{OUT0} = 0 A; V _{OUT0} = 4 V | 4.4 | | | | |
| CurrentSense timings (current sense mode - see Figure 5. CurrentSense timings (current sense mode)) ⁽³⁾ | | | | | | | |
| t _{DSENSE1H} | Current sense settling time from rising edge of SEN | V _{IN} = 5 V; V _{SEN} = 0 V to 5 V; R _{SENSE} = 1 kΩ; R _L = 0.87 Ω | | | 60 | μs | |
| t _{DSENSE1L} | Current sense disable delay time from falling edge of SEN | V _{IN} = 5 V; V _{SEN} = 5 V to 0 V; R _{SENSE} = 1 kΩ; R _L = 0.87 Ω | | 5 | 20 | μs | |
| t _{DSENSE2H} | Current sense settling time from rising edge of INPUT | V _{IN} = 0 V to 5 V; V _{SEN} = 5 V; R _{SENSE} = 1 kΩ; R _L = 0.87 Ω | | 100 | 200 | μs | |
| Δt _{DSENSE2H} | Current sense settling time from rising edge of I _{OUT} (dynamic response to a step change of I _{OUT}) | V _{IN} = 5 V; V _{SEN} = 5 V; R _{SENSE} = 1 kΩ; I _{SENSE} = 90 % of I _{SENSEMAX} ; R _L = 0.87 Ω | | | 100 | μs | |
| t _{DSENSE2L} | Current sense turn-off delay time from falling edge of INPUT | V _{IN} = 5 V to 0 V; V _{SEN} = 5 V; R _{SENSE} = 1 kΩ; R _L = 0.87 Ω | | 70 | 250 | μs | |
| t _{DSENSE3H} | Current sense latch-OFF filtering time | | 1.4 | 2.0 | 2.6 | ms | |

1. Specified by design and evaluated by characterization, not tested in production.

2. All values refer to V_{CC} = 13 V; T_J = 25°C, unless otherwise specified.

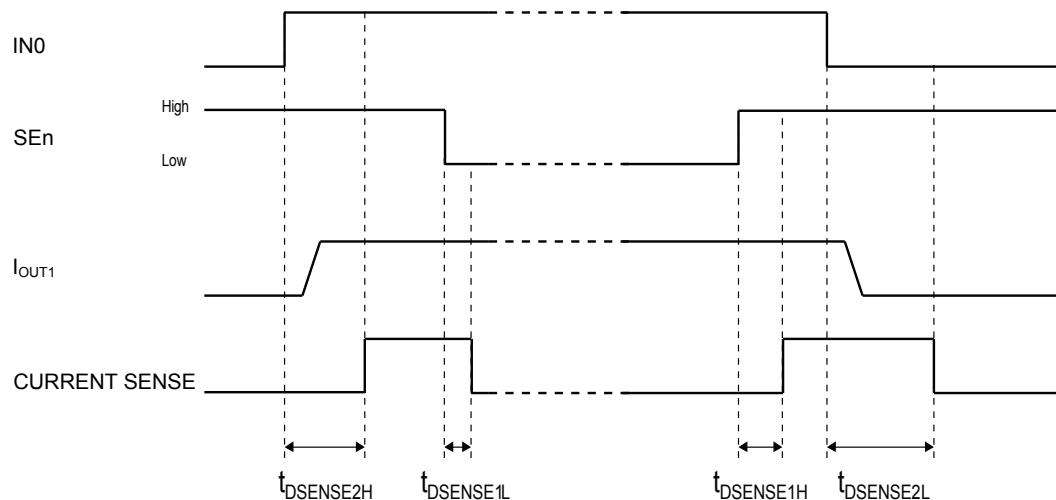
3. Transition delay is measured up to $\pm 10\%$ of final conditions.

Figure 4. Switching time and pulse skew

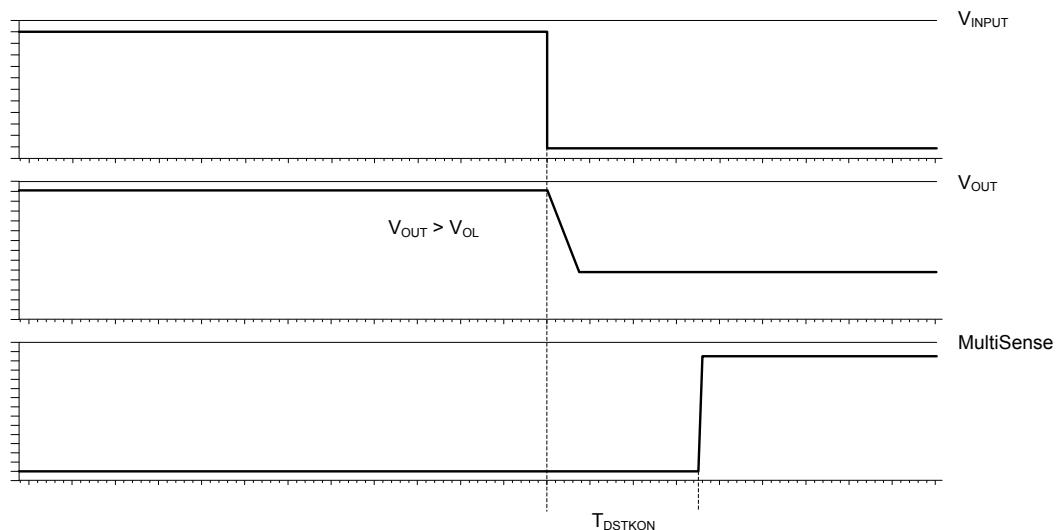


GADG2702181015RI

Figure 5. CurrentSense timings (current sense mode)



GADG2702181020RI

Figure 6. T_{DSTKON}


GAPG2609141140CFT

Table 10. Truth table

| Mode | Conditions | IN_X | FR | SEn | OUT_X | CS | Comments |
|-------------------------|--------------------------------------------------------------------------------------------|--------|----|---------|---------|---------|---------------------------------------------------------|
| Standby | All logic inputs low | L | L | L | L | Hi-Z | Low quiescent current consumption |
| Normal | Nominal load connected; $T_J < 150^\circ C$ | L | X | See (1) | L | See (1) | |
| | | H | L | | H | See (1) | Outputs configured for auto-restart |
| | | H | H | | H | See (1) | Outputs configured for latch-off |
| Overload | Overload or short to GND causing: $T_J > T_{TSD}$ or $\Delta T_J > \Delta T_{J_SD}$ | L | X | See (1) | L | See (1) | |
| | | H | L | | H | See (1) | Output cycles with temperature hysteresis |
| | | H | H | | L | See (1) | Output latches-off |
| Undervoltage | $V_{CC} < V_{USD}$ (falling) | X | X | X | L | Hi-Z | Re-start when $V_{CC} > V_{USD} + V_{USDhyst}$ (rising) |
| OFF-state diagnostics | Short to V_{CC} | L | X | See (1) | H | See (1) | |
| | Open-load | L | X | | H | See (1) | External pull-up |
| Negative output voltage | Inductive loads turn-off | L | X | See (1) | < 0 V | See (1) | |

1. Refer to Table 11. CurrentSense multiplexer addressing

Table 11. CurrentSense multiplexer addressing

| SEn | MUX channel | CS output | | | |
|-------|----------------------|------------------------------|--------------------------|--------------------------|-----------------|
| | | Normal mode | Overload | OFF-state diag. | Negative output |
| L | | Hi-Z | | | |
| H | Channel 0 diagnostic | $I_{SENSE} = 1/K * I_{OUT0}$ | $V_{SENSE} = V_{SENSEH}$ | $V_{SENSE} = V_{SENSEH}$ | Hi-Z |

2.4 Waveforms

Figure 7. Latch-off mode - Intermittent short circuit

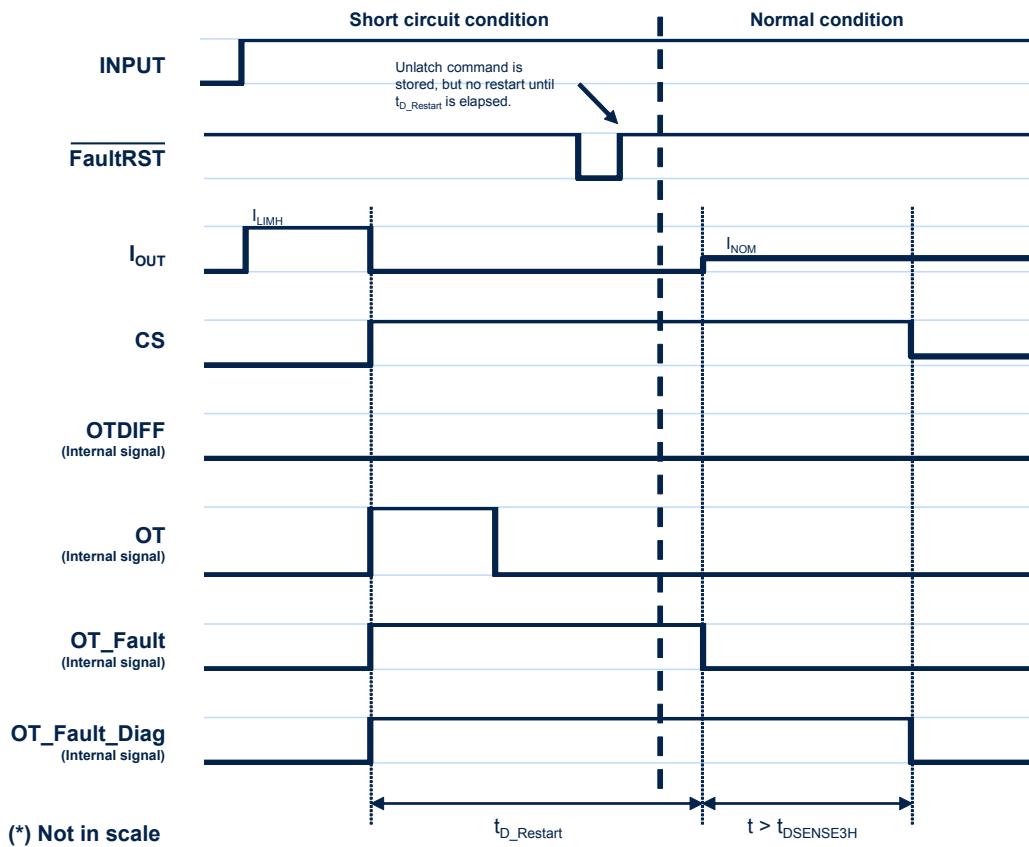


Figure 8. Auto-restart mode - Intermittent short circuit

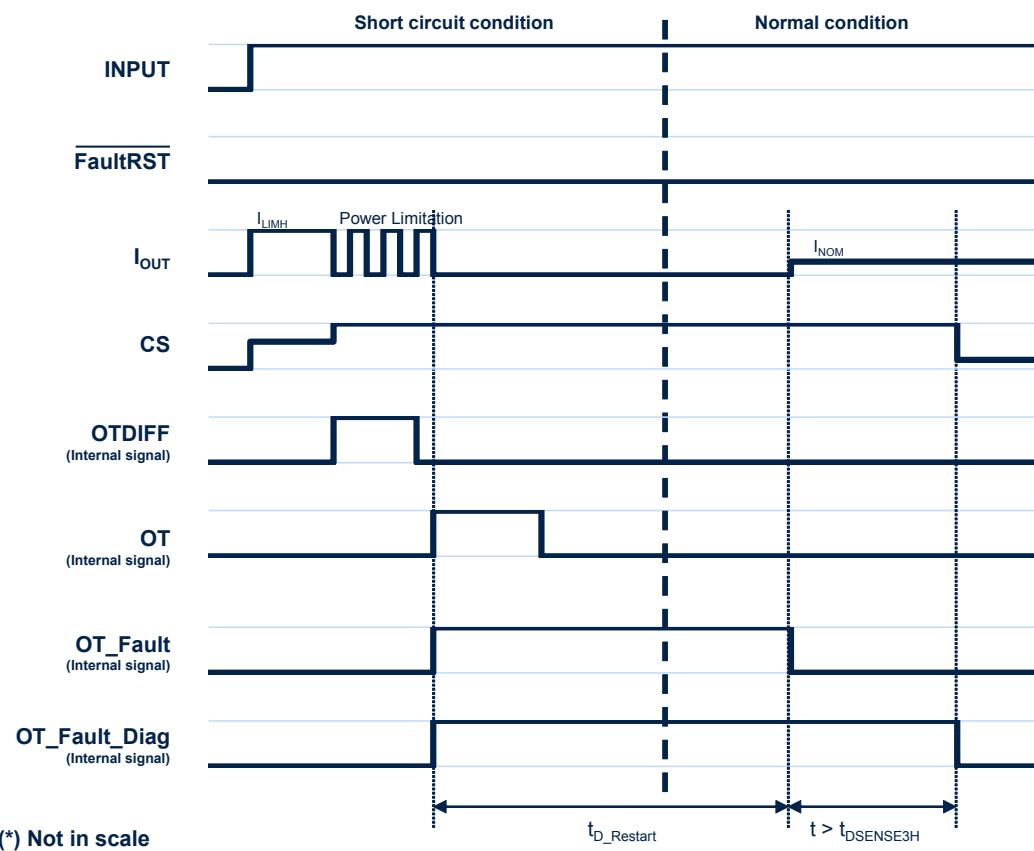
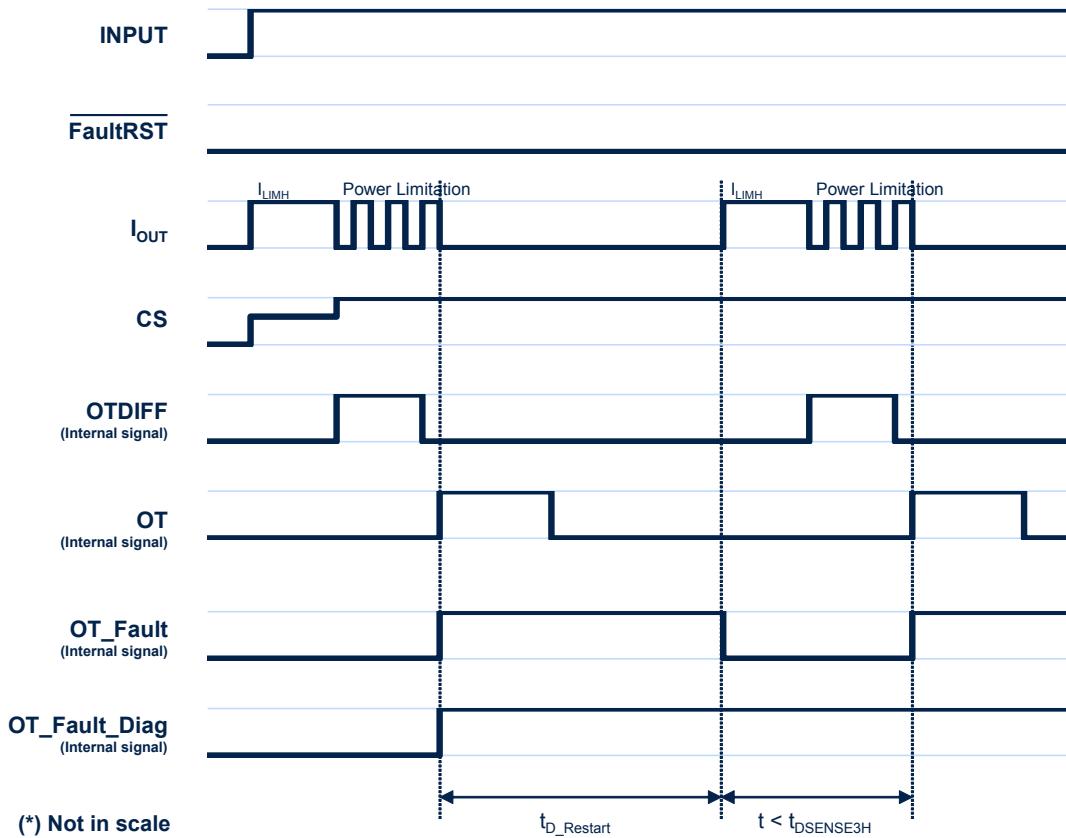
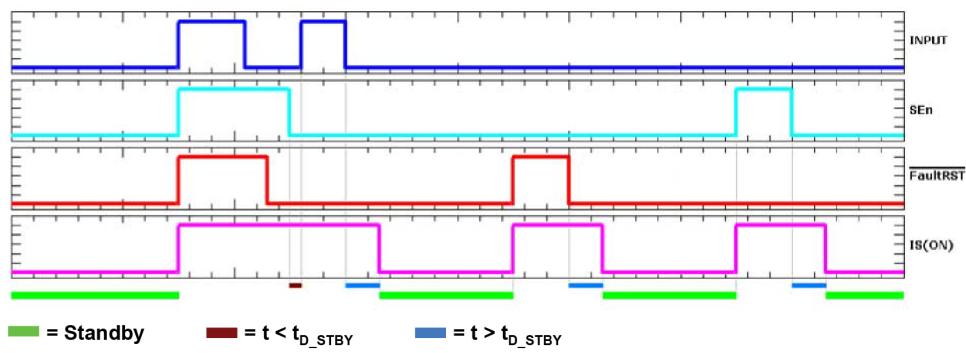
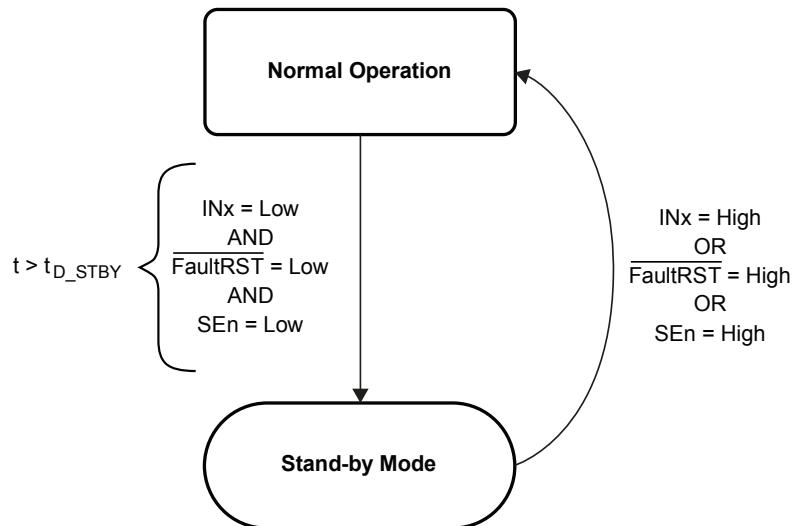


Figure 9. Auto-restart mode - Permanent short circuit

Figure 10. Standby mode activation


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Figure 11. Standby state diagram

GADG2702181047RI

2.5 Electrical characteristics (curves)

Figure 12. OFF-state output current

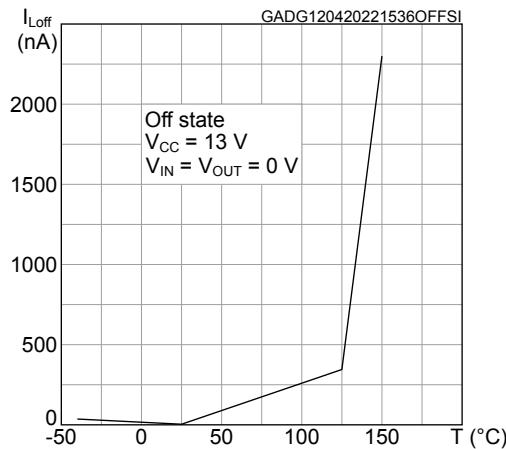


Figure 13. Standby current

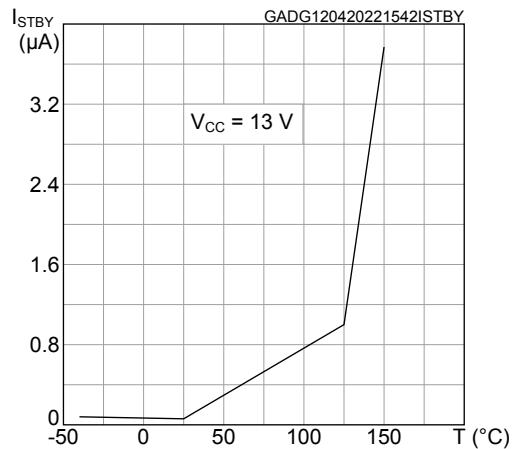


Figure 14. $I_{GND(ON)}$ vs. I_{out}

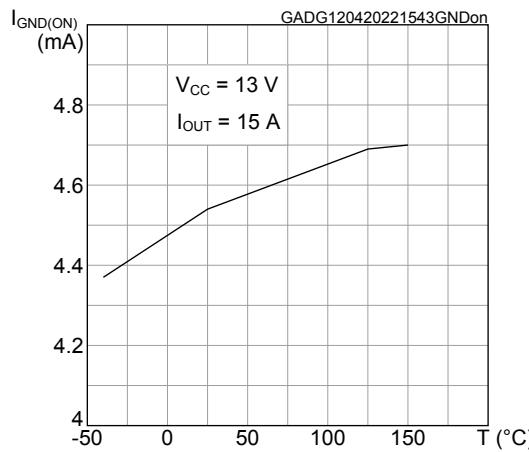


Figure 15. Logic input high level voltage

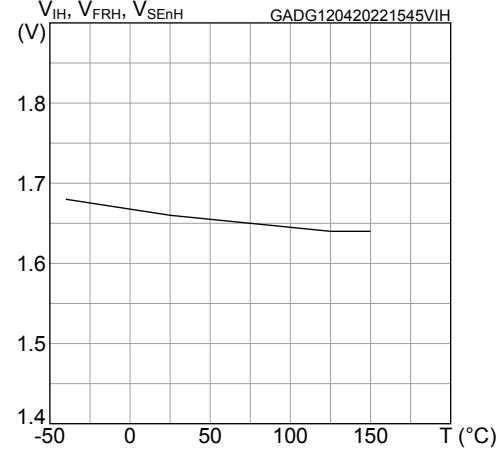


Figure 16. Logic input low level voltage

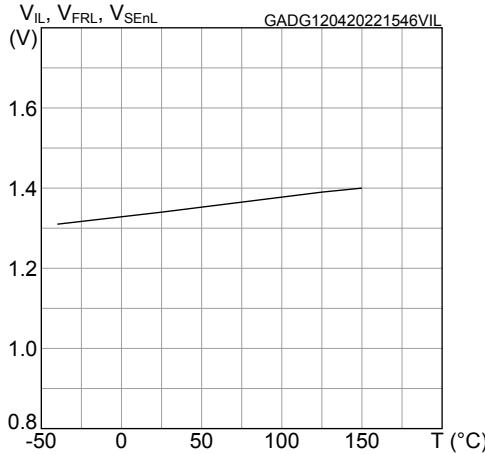


Figure 17. High level logic input current

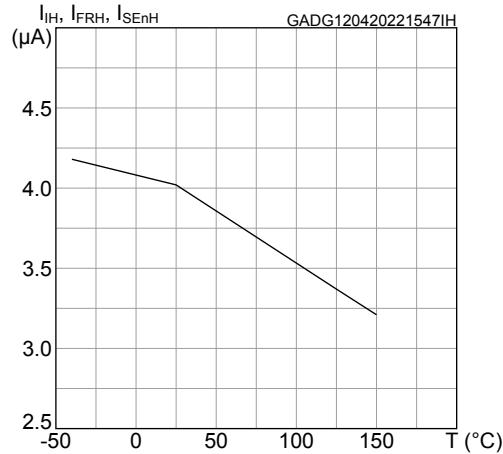


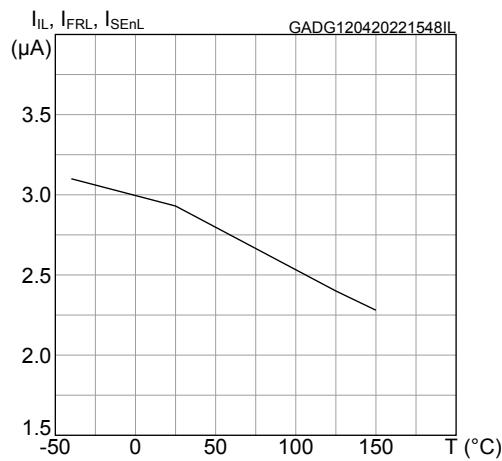
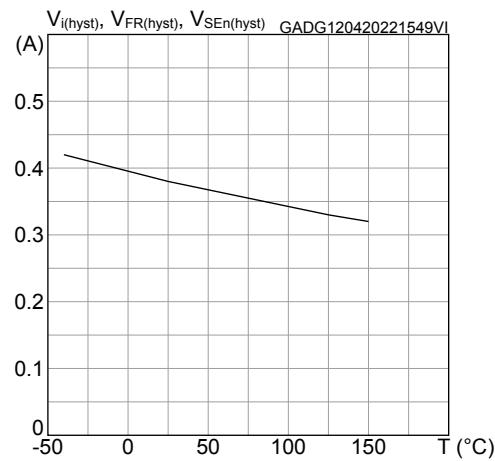
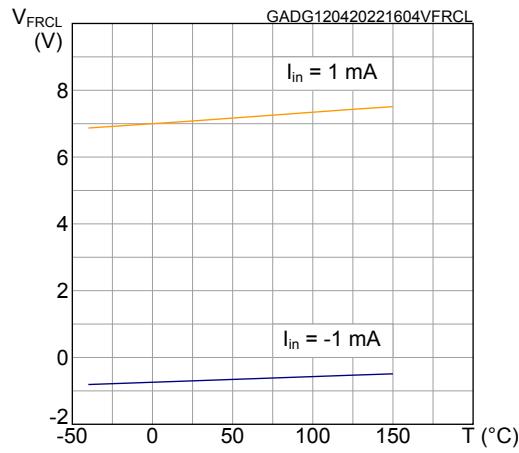
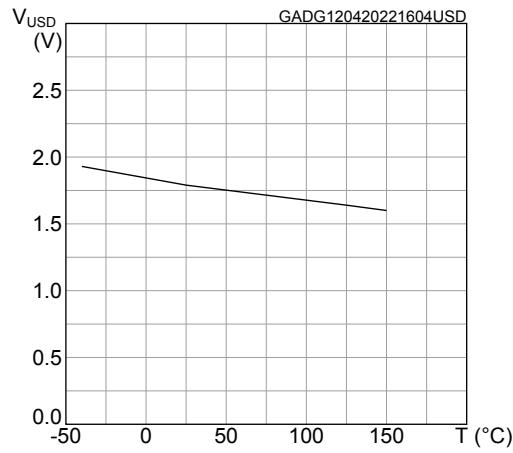
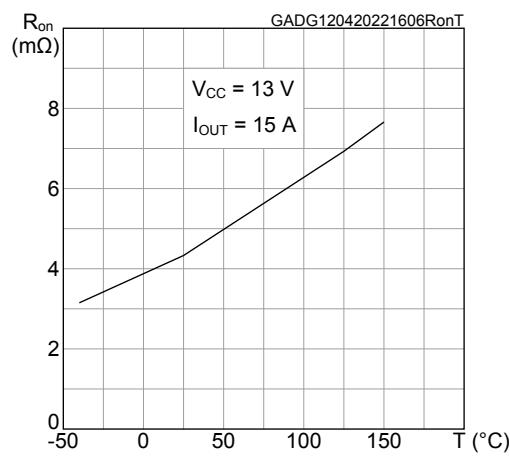
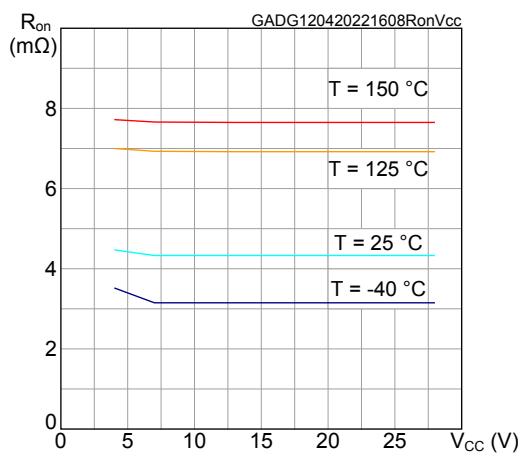
Figure 18. Low level logic input current

Figure 19. Logic input hysteresis voltage

Figure 20. FaultRST input clamp voltage

Figure 21. Undervoltage shutdown

Figure 22. On-state resistance vs. T_C

Figure 23. On-state resistance vs. V_{CC}


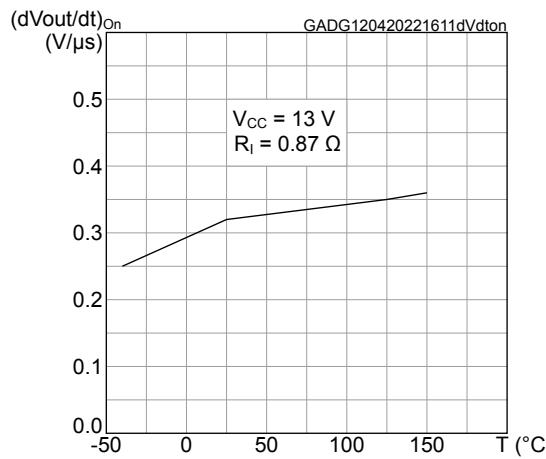
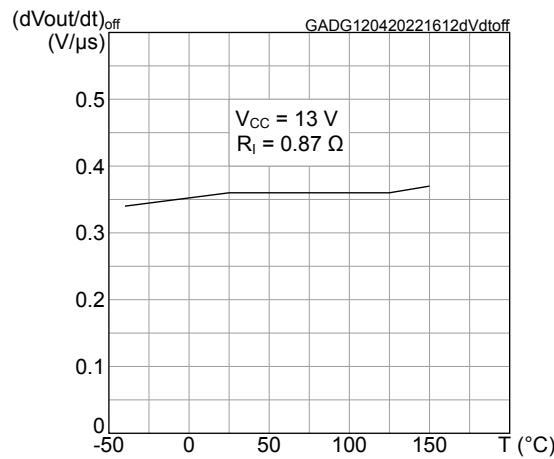
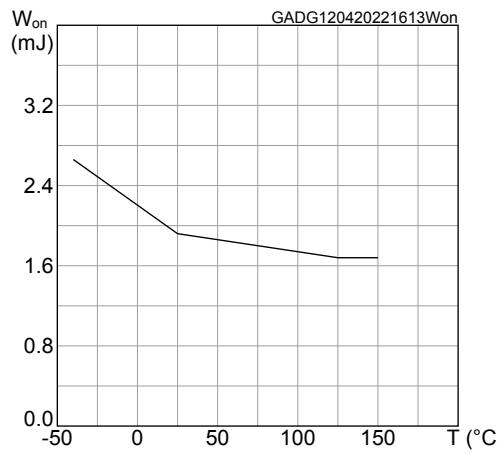
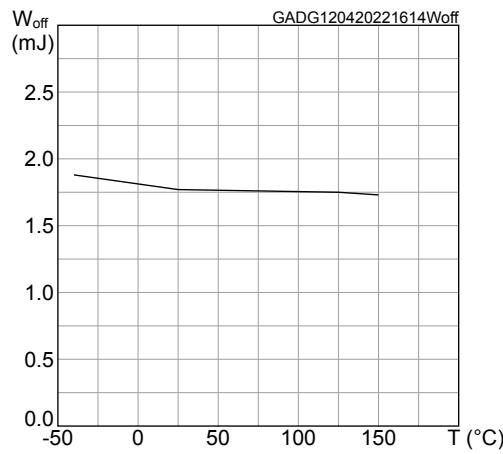
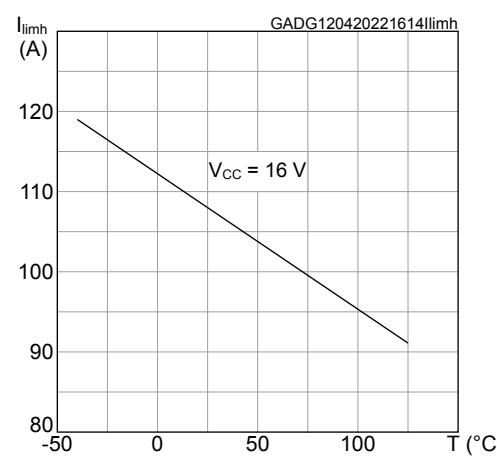
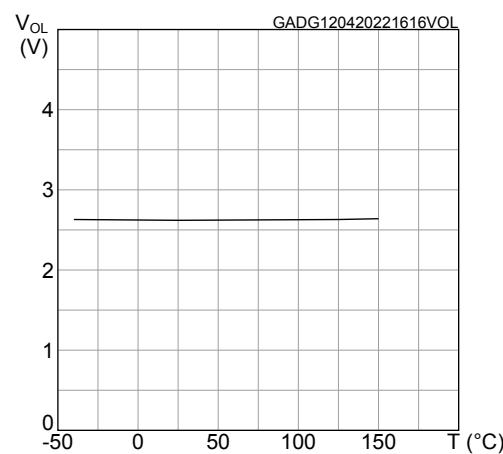
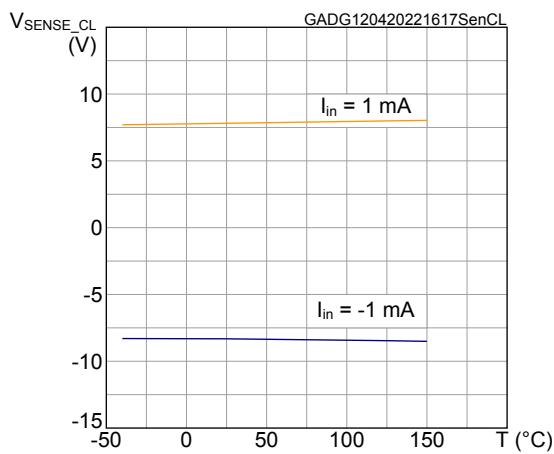
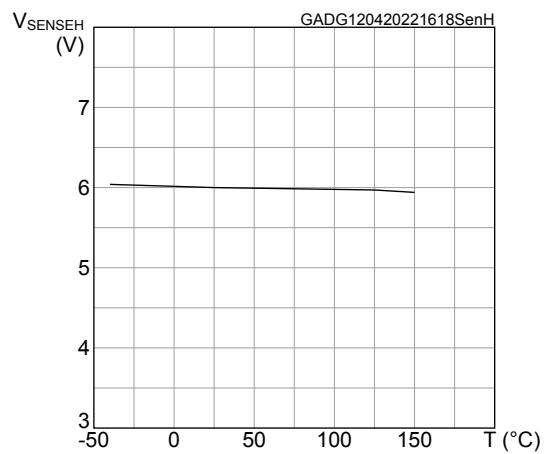
Figure 24. Turn-on voltage slope

Figure 25. Turn-off voltage slope

Figure 26. W_{on} vs T_c

Figure 27. W_{off} vs T_c

Figure 28. I_{LIMH} vs T_c

Figure 29. OFF-state open-load voltage detection threshold


Figure 30. $V_{\text{Sense clamp}}$ vs T_c Figure 31. V_{senseh} vs T_c 

3 Protections

3.1 Power limitation

The basic working principle of this protection consists of an indirect measurement of the junction temperature swing ΔT_J through the direct measurement of the spatial temperature gradient on the device surface in order to automatically shut off the output MOSFET as soon as ΔT_J exceeds the safety level of ΔT_{J_SD} . According to the voltage level on the FaultRST pin, the output MOSFET switches on and cycles with a thermal hysteresis according to the maximum instantaneous power which can be handled (FaultRST = Low) or remain off (FaultRST = High). The protection prevents fast thermal transient effects and, consequently, reduces thermo-mechanical fatigue.

3.2 Thermal shutdown

In case the junction temperature of the device exceeds the maximum allowed threshold (typically 175 °C), it automatically switches off and the diagnostic indication is triggered. According to the voltage level on the FaultRST pin, the device switches on again as soon as its junction temperature drops to T_R (FaultRST = Low) or remains off (FaultRST = High).

3.3 Current limitation

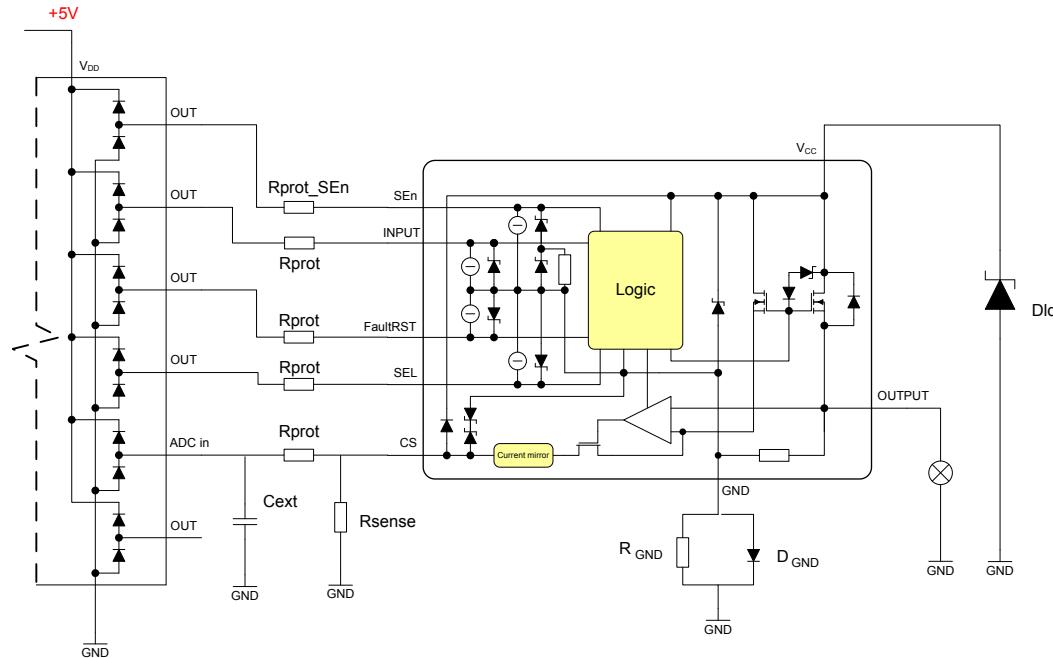
The device is equipped with an output current limiter in order to protect the silicon as well as the other components of the system (for example bonding wires, wiring harness, connectors, loads, etc.) from excessive current flow. Consequently, in case of short-circuit, overload or during load power-up, the output current is clamped to a safety level, I_{LIMH} , by operating the output power MOSFET in the active region.

3.4 Negative voltage clamp

In case the device drives inductive load, the output voltage reaches a negative value during turn off. A negative voltage clamp structure limits the maximum negative voltage to a certain value, V_{DEMAG} , allowing the inductor energy to be dissipated without damaging the device.

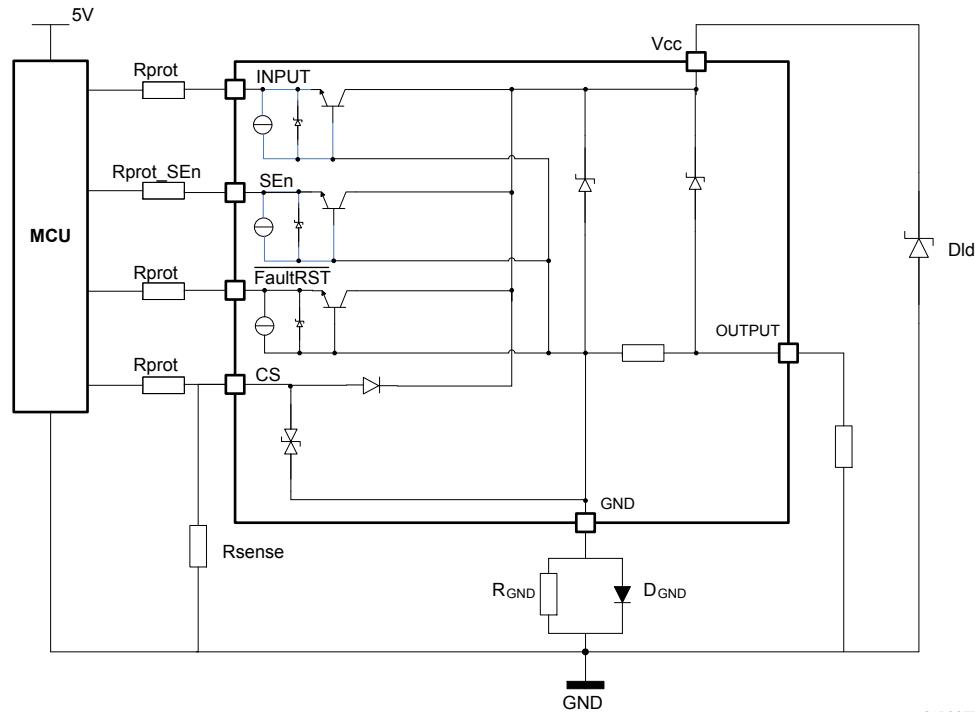
4 Application information

Figure 32. Application diagram



4.1 GND protection network against reverse battery

Figure 33. Simplified internal structure



GAPGCFT00830

4.1.1 Diode (DGND) in the ground line

A resistor (typ. $R_{GND} = 4.7 \text{ k}\Omega$) should be inserted in parallel to D_{GND} if the device drives an inductive load.

This small signal diode can be safely shared amongst several different HSDs. Also in this case, the presence of the ground network produces a shift ($\approx 600 \text{ mV}$) in the input threshold and in the status output values if the microprocessor ground is not common to the device ground. This shift does not vary if more than one HSD shares the same diode/resistor network.

4.2

Immunity against transient electrical disturbances

The immunity of the device against transient electrical emissions, conducted along the supply lines and injected into the V_{CC} pin, is tested in accordance with ISO7637-2:2011 (E) and ISO 16750-2:2010.

The related function performance status classification is shown in [Table 12. ISO 7637-2 - electrical transient conduction along supply line](#).

Test pulses are applied directly to DUT (device under test) both in ON and OFF state and in accordance to ISO 7637-2:2011(E), chapter 4.

The DUT is intended as the current device only, with external components as shown in [Figure 34. M0-9 application schematic](#).

Status II is defined in ISO 7637-1 Function Performance Status Classification (FPSC) as follows: "The function does not perform as designed during the test but returns automatically to normal operation after the test".

Table 12. ISO 7637-2 - electrical transient conduction along supply line

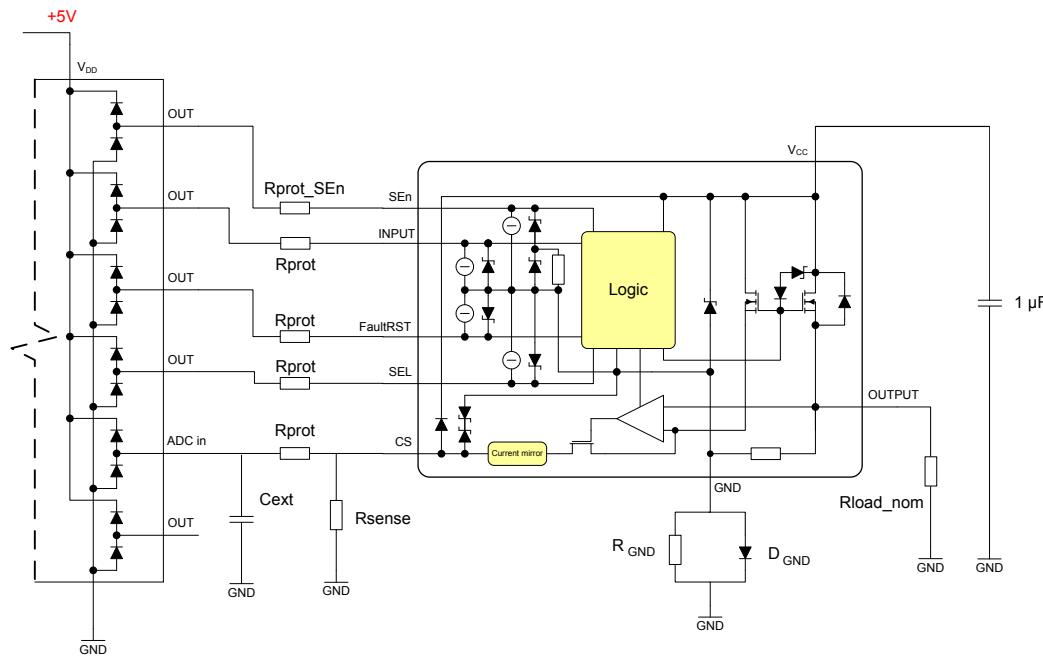
| Test Pulse 2011(E) | Test pulse severity level with Status II functional performance status | | Minimum number of pulses or test time | Burst cycle / pulse repetition time | | Pulse duration and pulse generator internal impedance |
|-----------------------------------------|------------------------------------------------------------------------|-------------|---------------------------------------|-------------------------------------|--------|-------------------------------------------------------|
| | Level | $U_S^{(1)}$ | | min | max | |
| 1 | III | -112 V | 500 pulses | 0.5 s | | 2 ms, 10 Ω |
| 2a | III | +55 V | 500 pulses | 0.2 s | 5 s | 50 μs , 2 Ω |
| 3a | IV | -220 V | 1h | 90 ms | 100 ms | 0.1 μs , 50 Ω |
| 3b | IV | +150 V | 1h | 90 ms | 100 ms | 0.1 μs , 50 Ω |
| 4 ⁽²⁾ | IV | -7 V | 1 pulse | | | 100 ms, 0.01 Ω |
| Load dump according to ISO 16750-2:2010 | | | | | | |
| Test B ⁽³⁾ | | 35 V | 5 pulses | 1 min | | 400 ms, 2 Ω |

1. U_S is the peak amplitude as defined for each test pulse in ISO 7637-2:2011(E), chapter 5.6.

2. Test pulse from ISO 7637-2:2004(E).

3. With 35 V external suppressor referred to ground ($-40^\circ\text{C} < T_j < 150^\circ\text{C}$).

Figure 34. M0-9 application schematic



4.3

MCU I/Os protection

If a ground protection network is used and negative transients are present on the V_{CC} line, the control pins will be pulled negative. ST suggests to insert a resistor (R_{prot}) in line both to prevent the microcontroller I/O pins from latching-up and to protect the HSD inputs.

The value of these resistors is a compromise between the leakage current of microcontroller and the current required by the HSD I/Os (Input levels compatibility) with the latch-up limit of microcontroller I/Os.

Equation

$$V_{CCpeak}/I_{latchup} \leq R_{prot} \leq (V_{OH\mu C} - V_{IH} - V_{GND}) / I_{IHmax}$$

Calculation example:

For $V_{CCpeak} = -150$ V; $I_{latchup} \geq 20$ mA; $V_{OH\mu C} \geq 4.5$ V

$$7.5 \text{ k}\Omega \leq R_{prot} \leq 140 \text{ k}\Omega$$

Recommended values: $R_{prot} = 15 \text{ k}\Omega$

A different value of the resistor has to be used for SEn pin, Rprot_SEn, as reported in Figure 32. Application diagram.

4.4

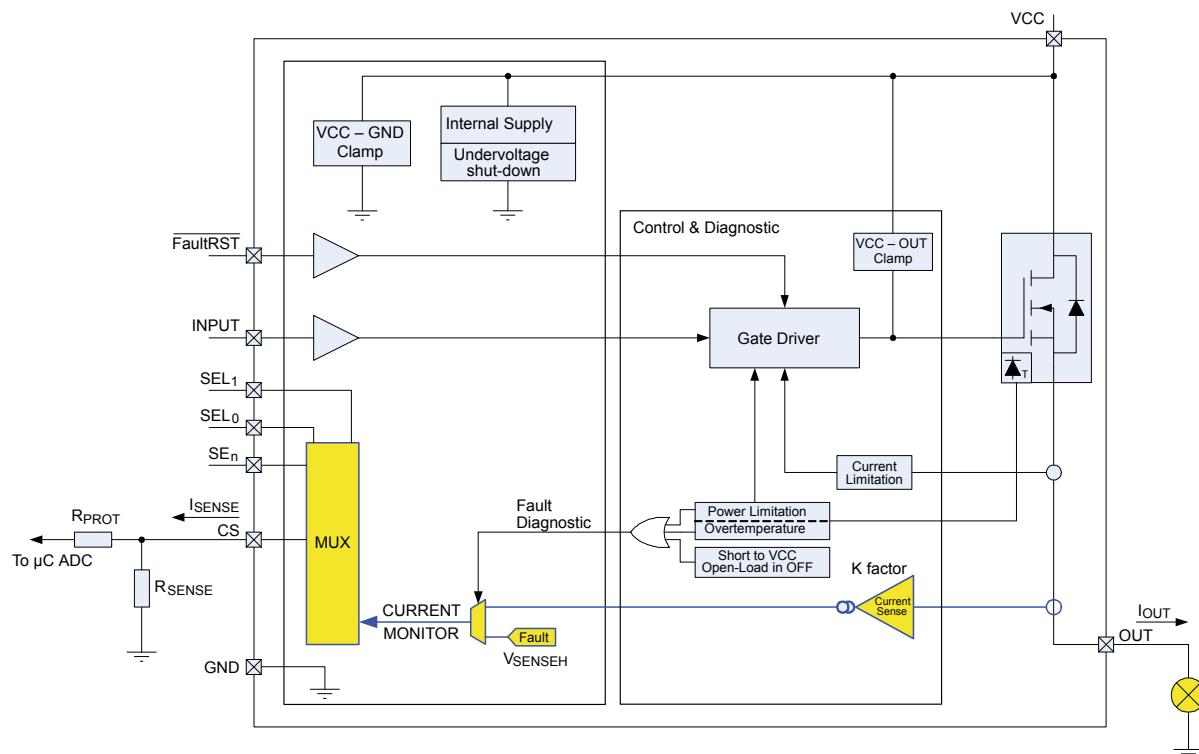
CS - analog current sense

Diagnostic information on device and load status are provided by an analog output pin (CS) delivering the following signals:

- Current monitor: current mirror of channel output current

Those signals are routed through an analog multiplexer which is configured and controlled by means of SELx and SEn pins, according to the address map in Table 7.

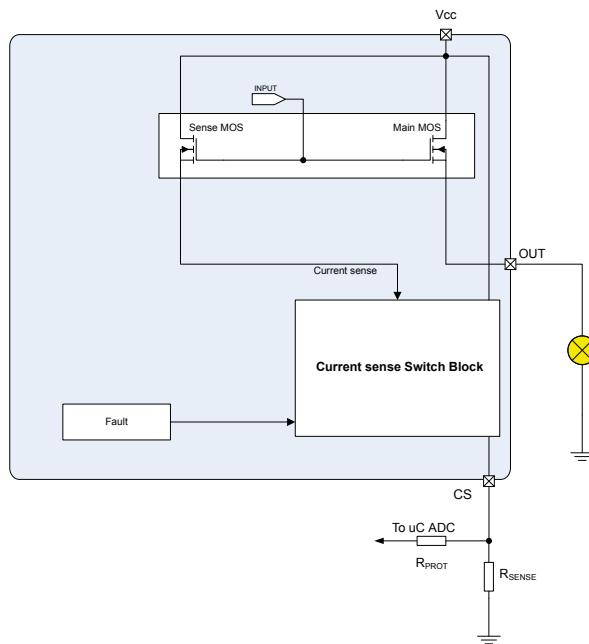
Figure 35. CurrentSense and diagnostic – block diagram



GADG2004171456PS

4.4.1 Principle of current sense signal generation

Figure 36. CurrentSense block diagram



GAPG2307131200CFT

Current sense

The output is capable of providing:

- Current mirror proportional to the load current in normal operation, delivering current proportional to the load according to known ratio named K
- Diagnostics flag in fault conditions delivering fixed voltage V_{SENSEH}

The current delivered by the current sense circuit, I_{SENSE} , can be easily converted into a voltage V_{SENSE} by using an external sense resistor, R_{SENSE} , allowing continuous load monitoring and abnormal condition detection.

Normal operation (channel ON, no fault, SEn active)

While device is operating in normal conditions (no fault intervention), V_{SENSE} calculation can be done using simple equations

Current provided by MultiSense output: $I_{SENSE} = I_{OUT}/K$

Voltage on R_{SENSE} : $V_{SENSE} = R_{SENSE} \cdot I_{SENSE} = R_{SENSE} \cdot I_{OUT}/K$

Where:

- V_{SENSE} is voltage measurable on R_{SENSE} resistor
- I_{SENSE} is current provided from CurrentSense pin in current output mode
- I_{OUT} is current flowing through output
- K factor represents the ratio between PowerMOS cells and SenseMOS cells; its spread includes geometric factor spread, current sense amplifier offset and process parameters spread of overall circuitry specifying the ratio between I_{OUT} and I_{SENSE} .

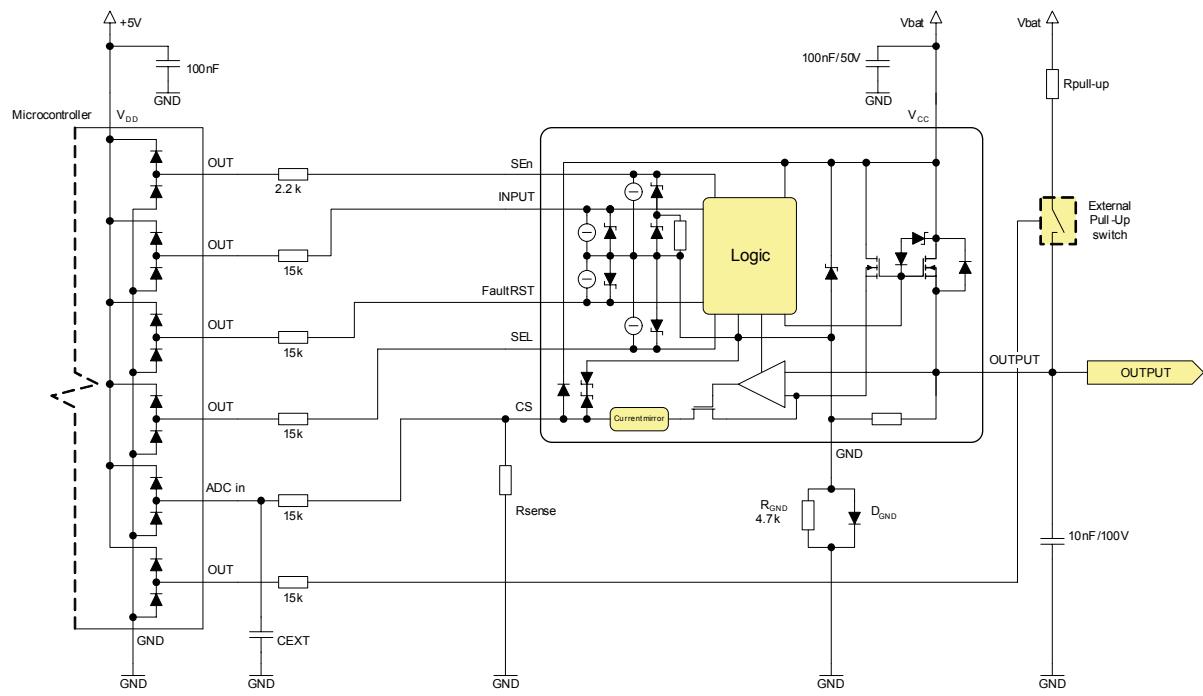
Failure flag indication

In case of power limitation/overtemperature, the fault is indicated by the CurrentSense pin which is switched to a "current limited" voltage source, V_{SENSEH} .

In any case, the current sourced by the CurrentSense in this condition is limited to I_{SENSEH} .

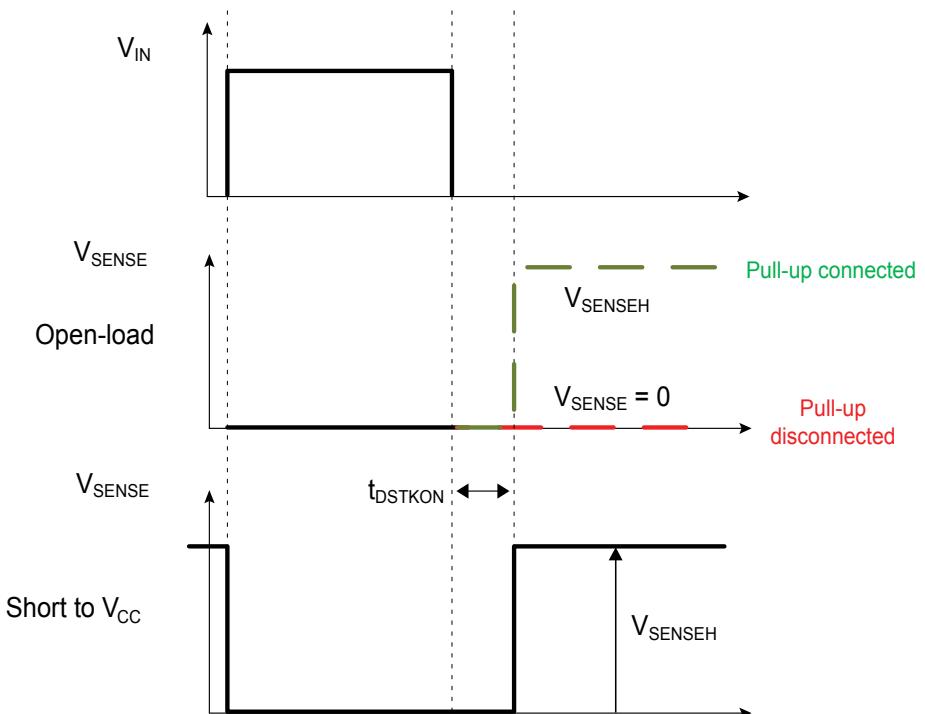
The typical behavior in case of overload or hard short circuit is shown in [Section 2.4: Waveforms](#).

Figure 37. Analog HSD – open-load detection in off-state



GAPG1201151432CFT

Figure 38. Open-load / short to V_{CC} condition



GADG2702181218RI

Table 13. CS pin levels in off-state

| Condition | Output | CS | SEn |
|-------------------|--------------------|--------------|-----|
| Open-load | $V_{OUT} > V_{OL}$ | Hi-Z | L |
| | | V_{SENSEH} | H |
| | $V_{OUT} < V_{OL}$ | Hi-Z | L |
| | | 0 | H |
| Short to V_{CC} | $V_{OUT} > V_{OL}$ | Hi-Z | L |
| | | V_{SENSEH} | H |
| Nominal | $V_{OUT} < V_{OL}$ | Hi-Z | L |
| | | 0 | H |

4.4.2 Short to V_{CC} and OFF-state open-load detection

Short to V_{CC}

A short circuit between V_{CC} and output is indicated by the relevant current sense pin set to V_{SENSEH} during the device off-state. Small or no current is delivered by the current sense during the on-state depending on the nature of the short-circuit.

OFF-state open-load with external circuitry

Detection of an open-load in off mode requires an external pull-up resistor R_{PU} connecting the output to a positive supply voltage V_{PU} .

It is preferable that V_{PU} is switched off during the module standby mode in order to avoid the overall standby current consumption to increase in normal conditions, that is when load is connected.

R_{PU} must be selected in order to ensure $V_{OUT} > V_{OLmax}$ in accordance with the following equation:

$$R_{PU} < \frac{V_{PU} - 4}{I_{L(off2)min @ 4V}}$$

5

Maximum demagnetization energy ($V_{CC} = 16$ V)

Figure 39. Maximum turn off current versus inductance

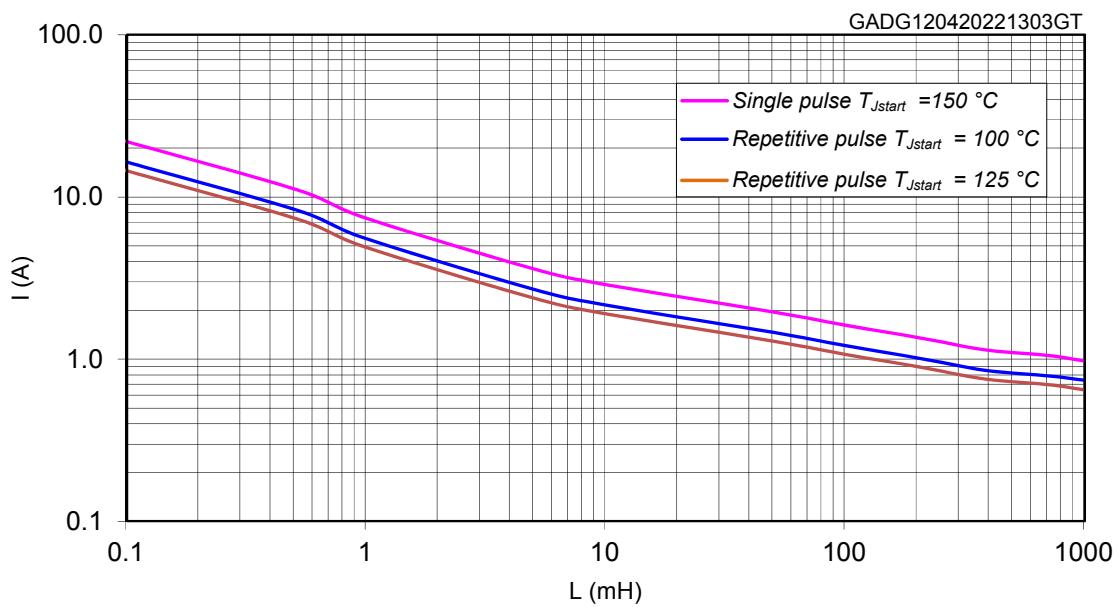
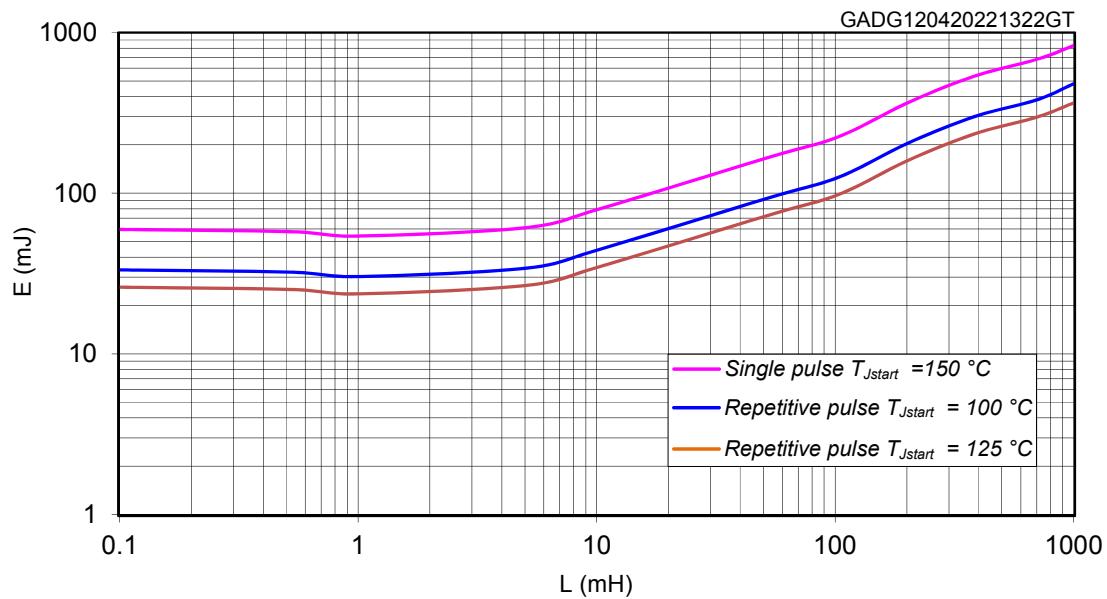


Figure 40. Maximum turn off energy versus inductance



6 Package and PCB thermal data

6.1 PowerSSO-16 thermal data

Figure 41. PowerSSO-16 on two-layer PCB (2s0p to JEDEC JESD 51-5)

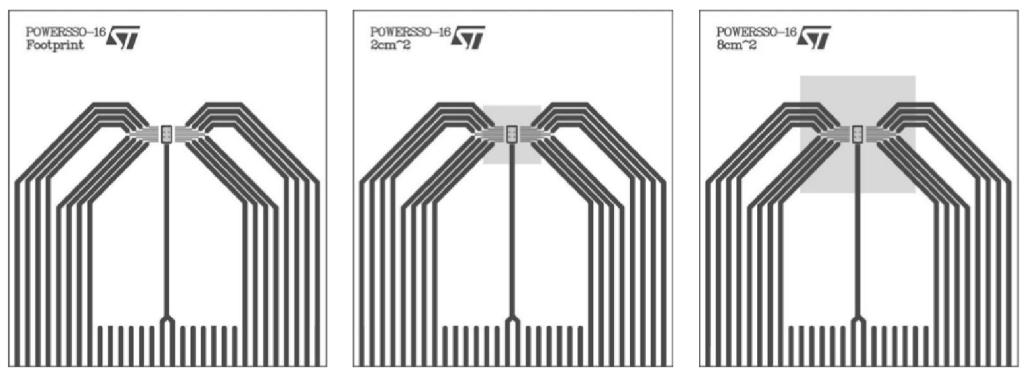


Figure 42. PowerSSO-16 on four-layer PCB (2s2p to JEDEC JESD 51-7)

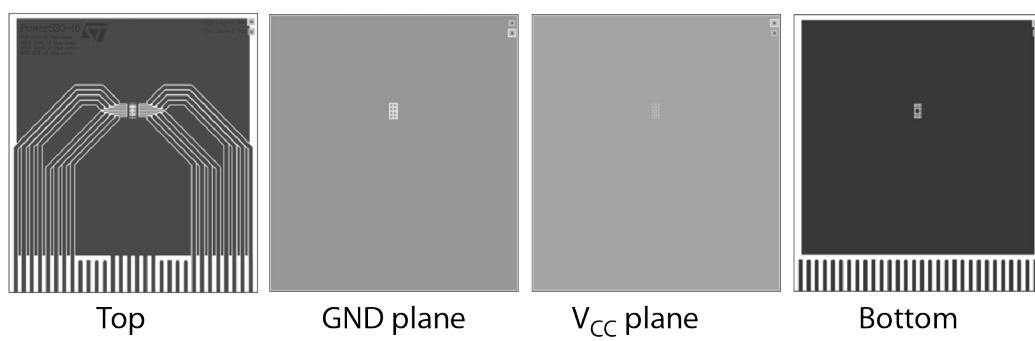


Table 14. PCB properties

| Dimension | Value |
|-----------------------------------------------|---------------------------|
| Board finish thickness | 1.6 mm +/- 10% |
| Board dimension | 77 mm x 86 mm |
| Board Material | FR4 |
| Copper thickness (top and bottom layers) | 0.070 mm |
| Copper thickness (inner layers) | 0.035 mm |
| Thermal vias separation | 1.2 mm |
| Thermal via diameter | 0.3 mm +/- 0.08 mm |
| Copper thickness on vias | 0.025 mm |
| Footprint dimension (top layer) | 2.2 mm x 3.9 mm |
| Heatsink copper area dimension (bottom layer) | Footprint, 2 cm² or 8 cm² |

Figure 43. $R_{thj\text{-amb}}$ vs PCB copper area in open box free air condition (one channel on)

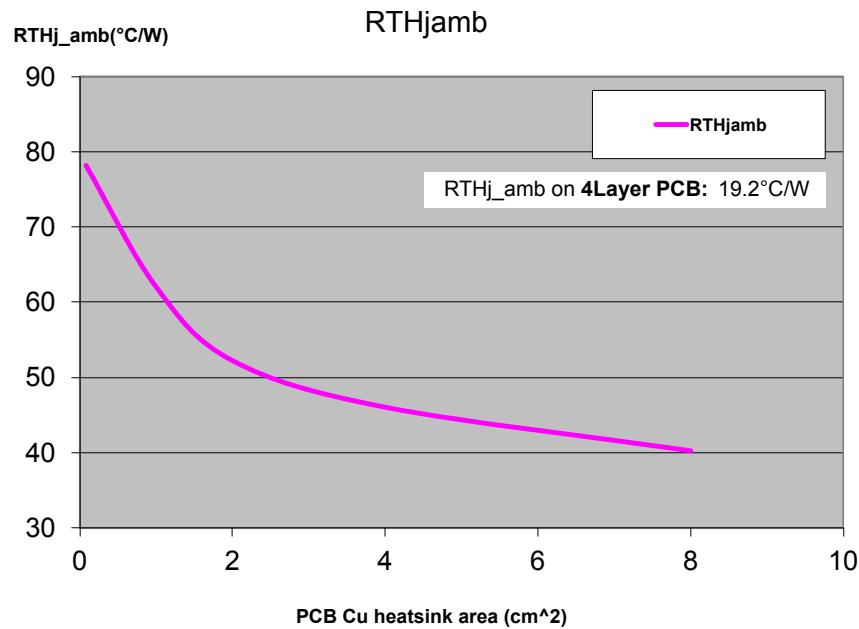
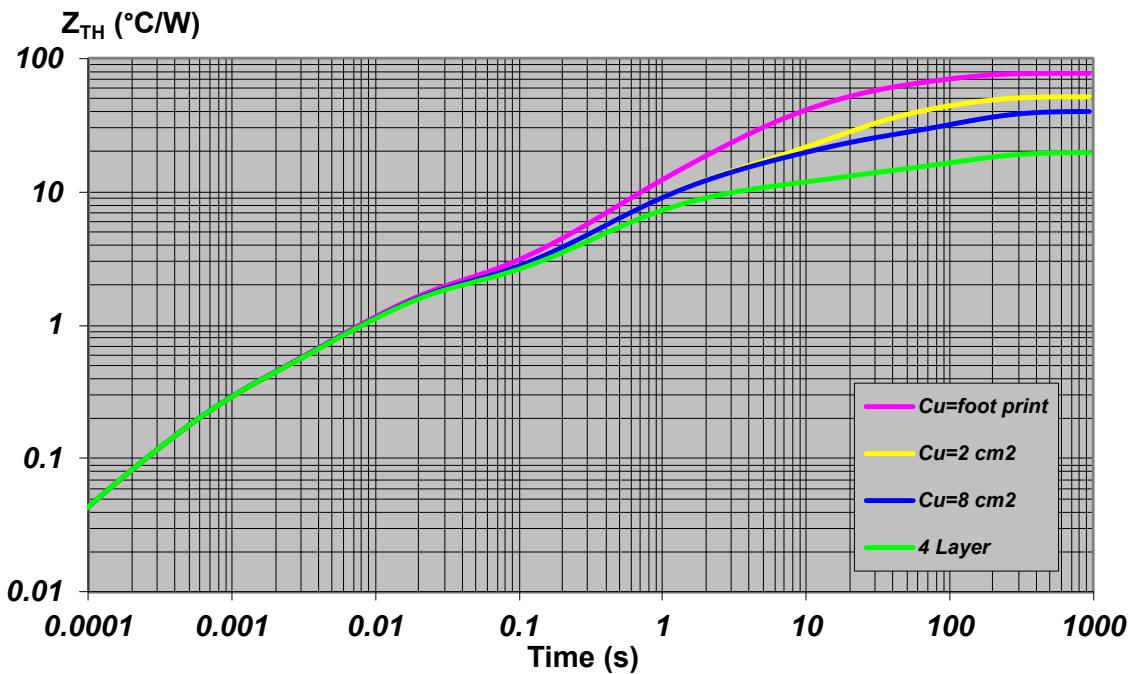


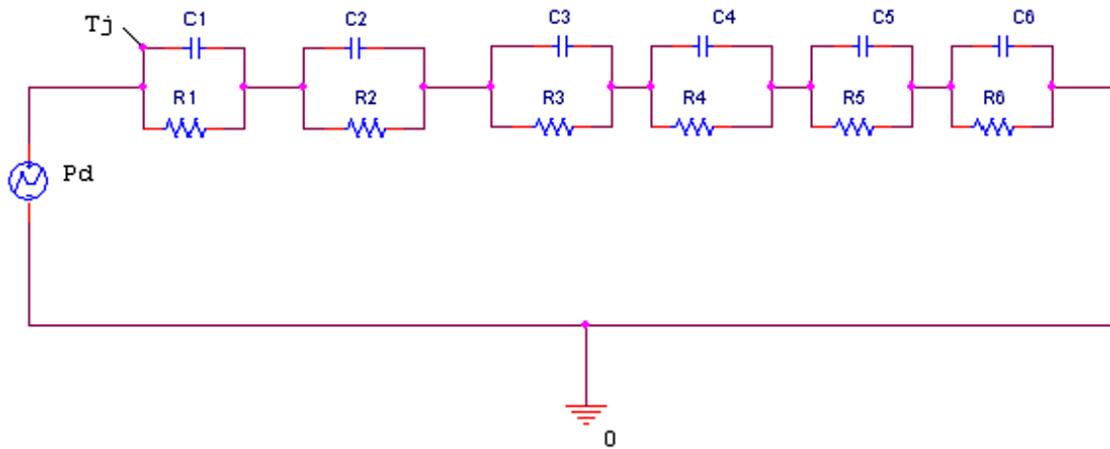
Figure 44. PowerSSO-16 thermal impedance junction ambient single pulse (one channel on)



Equation: pulse calculation formula

$$Z_{TH\delta} = R_{TH} \cdot \delta + Z_{THtp} (1 - \delta)$$

where $\delta = t_p/T$

Figure 45. Thermal fitting model of a double-channel HSD in PowerSSO-16


Note: the fitting model is a simplified thermal tool and is valid for transient evolutions where the embedded protections (power limitation or thermal cycling during thermal shutdown) are not triggered.

Table 15. Thermal parameters

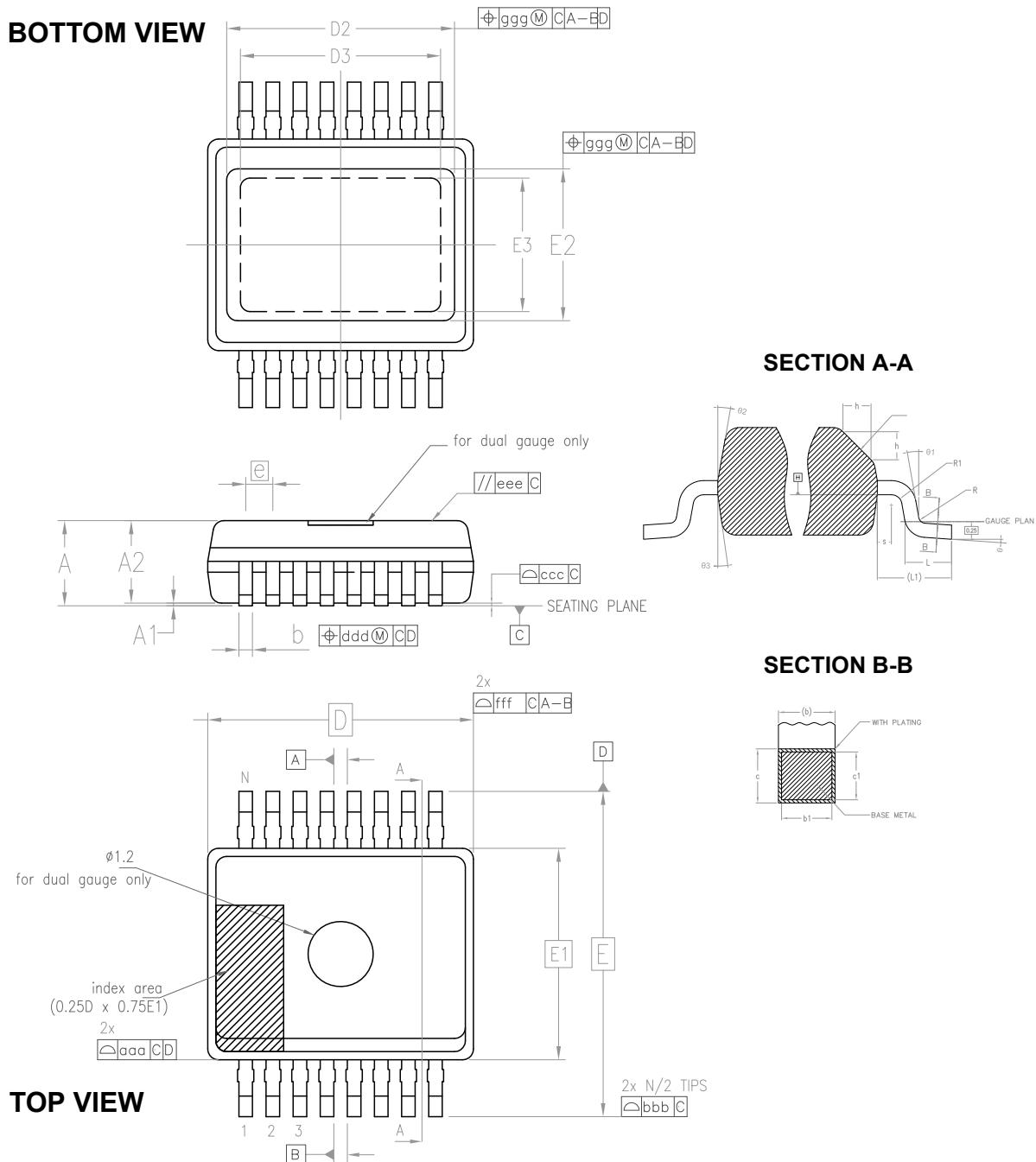
| Area/island (cm ²) | FP | 2 | 8 | 4L |
|--------------------------------|-------|-----|-----|-----|
| R1 (°C/W) | 0.2 | | | |
| R2 (°C/W) | 1.4 | | | |
| R3 (°C/W) | 4.6 | 4.6 | 4.6 | 4 |
| R4 (°C/W) | 16 | 6 | 6 | 4 |
| R5 (°C/W) | 30 | 20 | 10 | 3 |
| R6 (°C/W) | 26 | 20 | 18 | 7 |
| C1 (W·s/°C) | 0.003 | | | |
| C2 (W·s/°C) | 0.008 | | | |
| C3 (W·s/°C) | 0.12 | | | |
| C4 (W·s/°C) | 0.2 | 0.3 | 0.3 | 0.4 |
| C5 (W·s/°C) | 0.4 | 1 | 1 | 4 |
| C6 (W·s/°C) | 3 | 5 | 7 | 18 |

7 Package information

To meet environmental requirements, ST offers these devices in different grades of ECOPACK packages, depending on their level of environmental compliance. ECOPACK specifications, grade definitions, and product status are available at: www.st.com. ECOPACK is an ST trademark.

7.1 PowerSSO-16 package information

Figure 46. PowerSSO-16 package outline



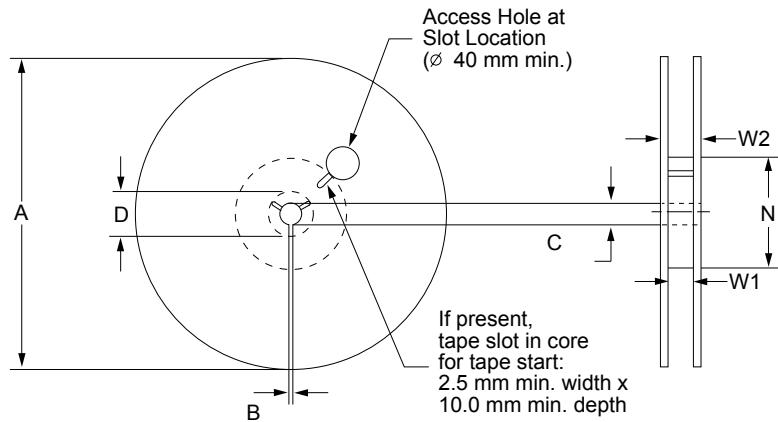
8017965_10_D

Table 16. PowerSSO-16 package mechanical data

| Symbol | Millimeters | | |
|--------------------------------|-------------|----------|------|
| | Min. | Typ. | Max. |
| Θ | 0° | | 8° |
| Θ1 | 0° | | |
| Θ2 | 5° | | 15° |
| Θ3 | 5° | | 15° |
| A | | | 1.70 |
| A1 | 0.00 | | 0.10 |
| A2 | 1.10 | | 1.60 |
| b | 0.20 | | 0.30 |
| b1 | 0.20 | 0.25 | 0.28 |
| c | 0.19 | | 0.25 |
| c1 | 0.19 | 0.20 | 0.23 |
| D | | 4.9 BSC | |
| D2 | 3.60 | | 4.20 |
| D3 | 2.90 | | |
| e | | 0.50 BSC | |
| E | | 6.00 BSC | |
| E1 | | 3.90 BSC | |
| E2 | 2.50 | | 3.10 |
| E3 | 1.80 | | |
| h | 0.25 | | 0.50 |
| L | 0.40 | 0.60 | 0.85 |
| L1 | | 1.00 REF | |
| N | | 16 | |
| R | 0.07 | | |
| R1 | 0.07 | | |
| S | 0.20 | | |
| Tolerance of form and position | | | |
| aaa | | 0.10 | |
| bbb | | 0.10 | |
| ccc | | 0.08 | |
| ddd | | 0.08 | |
| eee | | 0.10 | |
| fff | | 0.10 | |
| ggg | | 0.15 | |

7.2 PowerSSO-16 packing information

Figure 47. PowerSSO-16 reel 13"



TAPG2004151655CFT

Table 17. Reel dimensions

| Description | Value ⁽¹⁾ |
|----------------|----------------------|
| Base quantity | 2500 |
| Bulk quantity | 2500 |
| A (max) | 330 |
| B (min) | 1.5 |
| C (+0.5, -0.2) | 13 |
| D (min) | 20.2 |
| N | 100 |
| W1 (+2 /-0) | 12.4 |
| W2 (max) | 18.4 |

1. All dimensions are in mm.

Figure 48. PowerSSO-16 carrier tape

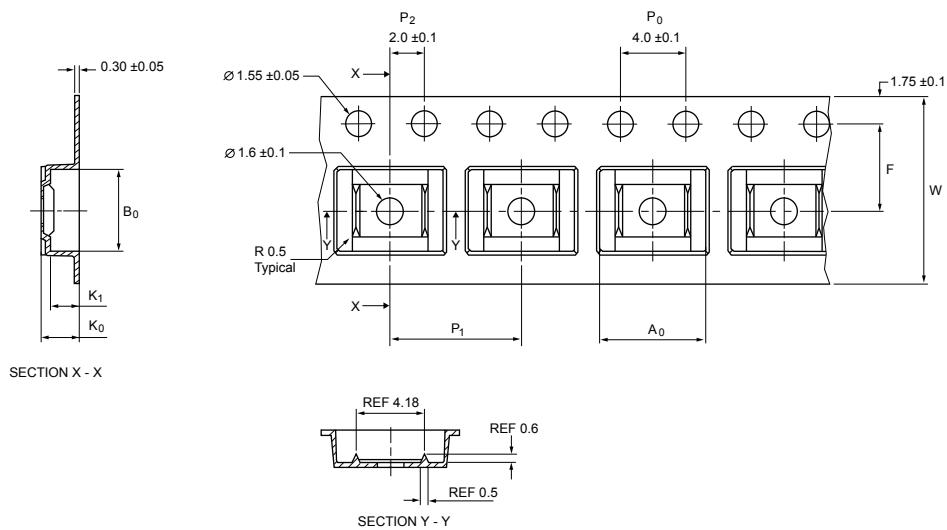
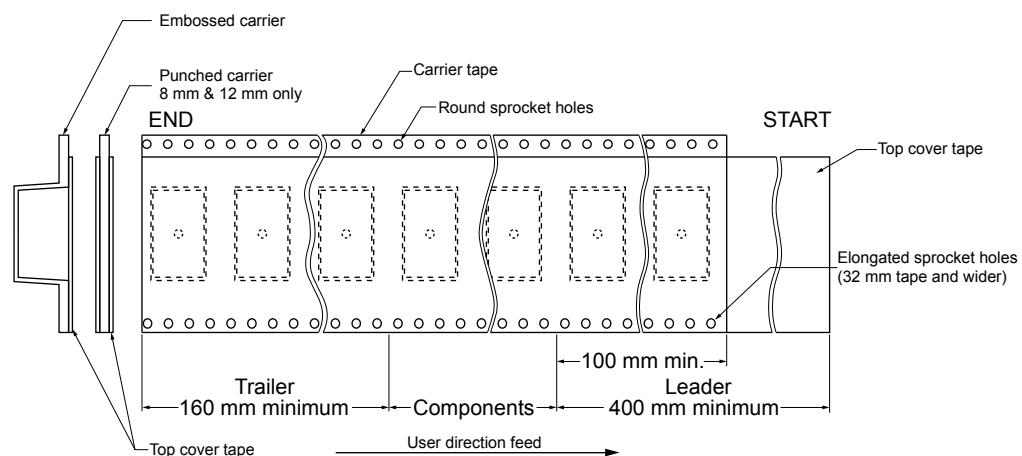


Table 18. PowerSSO-16 carrier tape dimensions

| Description | Value ⁽¹⁾ |
|----------------|----------------------|
| A ₀ | 6.50 ± 0.1 |
| B ₀ | 5.25 ± 0.1 |
| K ₀ | 2.10 ± 0.1 |
| K ₁ | 1.80 ± 0.1 |
| F | 5.50 ± 0.1 |
| P ₁ | 8.00 ± 0.1 |
| W | 12.00 ± 0.3 |

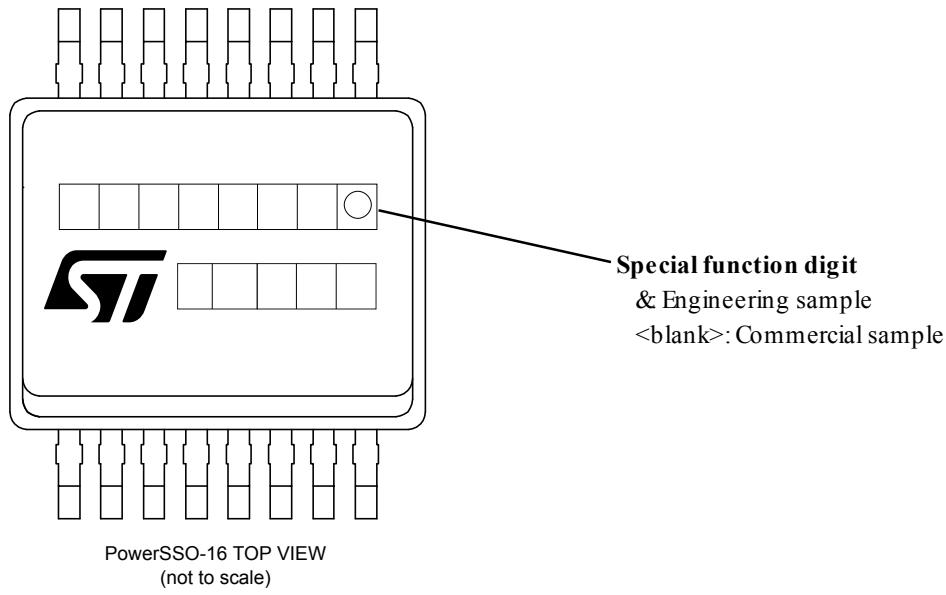
1. All dimensions are in mm.

Figure 49. PowerSSO-16 schematic drawing of leader and trailer tape

GAPG2004151511CFT

7.3 PowerSSO-16 marking information

Figure 50. PowerSSO-16 marking information



GADG0310161234SMD

Parts marked as ‘&’ are not yet qualified and therefore not approved for use in production. ST is not responsible for any consequences resulting from such use. In no event will ST be liable for the customer using any of these engineering samples in production. ST’s Quality department must be contacted prior to any decision to use these engineering samples to run a qualification activity.

Revision history

Table 19. Document revision history

| Date | Version | Changes |
|-------------|---------|--------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| 01-Mar-2018 | 1 | Initial release. |
| 28-Apr-2021 | 2 | <p>Updated <i>Features</i> in cover page.</p> <p>Updated <i>Section 1 Block diagram and pin description</i>.</p> <p>Updated <i>Figure 3. Current and voltage conventions</i>.</p> <p>Updated <i>Section 2.1 Absolute maximum ratings</i>.</p> <p>Updated <i>Section 2.3 Main electrical characteristics</i>.</p> <p>Updated <i>Section 2.4 Waveforms</i>.</p> <p>Added <i>Section 5 Package information</i>.</p> <p>Minor text changes.</p> |
| 14-Apr-2022 | 3 | <p>Updated <i>Section Features</i>.</p> <p>Updated <i>Table 2. Suggested connections for unused and not connected pins</i>, <i>Section 2.1: Absolute maximum ratings</i>, <i>Table 4. Thermal data</i>, <i>Table 6. Switching</i>, <i>Table 8. Protections</i> and <i>Table 9. CurrentSense</i>.</p> <p>Added <i>Section 2.5: Electrical characteristics (curves)</i>.</p> <p>Updated <i>Section 4: Application information</i>, <i>Section 4.1: GND protection network against reverse battery</i>, <i>Section 4.2: Immunity against transient electrical disturbances</i> and <i>Figure 37. Analog HSD – open-load detection in off-state</i>.</p> <p>Added <i>Section 5: Maximum demagnetization energy ($V_{CC} = 16$ V)</i> and <i>Section 6: Package and PCB thermal data</i>.</p> <p>Minor text changes.</p> |
| 28-Jul-2022 | 4 | <p>Updated <i>Figure 11. Standby state diagram</i>, <i>Section 2.5: Electrical characteristics (curves)</i> and <i>Section 5: Maximum demagnetization energy ($V_{CC} = 16$ V)</i>.</p> <p>Minor text changes.</p> |
| 17-Jan-2025 | 5 | Updated <i>Table 3. Absolute maximum ratings</i> and <i>Table 9. CurrentSense</i> . |

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