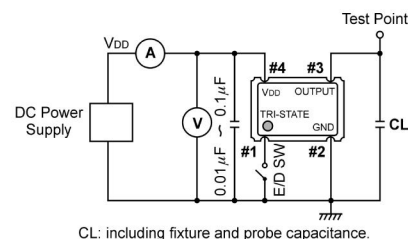




+3.3 V

* Internal crystal oscillation to be halted (pin#1=VIL)

Test circuit:



The diagram shows a digital signal waveform. The vertical axis represents voltage with levels: V_{DD} (90% or 80% V_{DD}), 50% V_{DD} , 10% or 20% V_{DD} , and 0V DC (GND). The horizontal axis represents time. Key parameters are labeled: t_R (rise time), t_F (fall time), t (pulse width), T (period), and $\text{Symmetry} = t/T \times 100(\%)$. The signal transitions between a "1" level and a "0" level.

