

# **CMOS Crystal Oscillator**

#### **Features**

- · CMOS Output XO
- · Output Frequencies from 625 kHz to 32.5 kHz
- 3.3V, 2.5V, and 1.8V Operation
- · Low Jitter Performance
- · Output Disable Feature
- Operating Temperature Ranging from –55°C to +125°C
- Small Industry Standard Package, 3.2 mm × 2.5 mm × 1.2 mm VDFN
- Product is RoHS Compliant and Fully Compatible with Lead-free Assembly

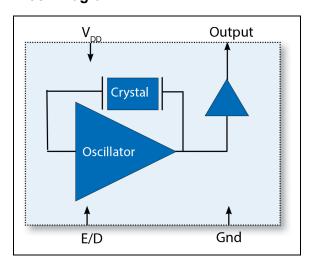
## **Applications**

- · SONET/SDH/DWDM
- · Ethernet, GE, SynchE
- · Storage Area Networking
- Fiber Channel
- · Digital Video
- · Broadband Access
- · Base Stations, Picocells

#### **General Description**

Microchip's VC-820 Crystal Oscillator (XO) is a quartz stabilized square wave generator with a CMOS output. The VC-820 uses a fundamental or a third overtone crystal, oscillating in a fundamental tone, resulting in very low jitter performance, and a monolithic IC which improves reliability and reduces cost.

## **Block Diagram**



#### 1.0 ELECTRICAL CHARACTERISTICS

### **Absolute Maximum Ratings †**

Storage Temperature (T <sub>S</sub> )	–55°C to +125°C
Soldering Temp/Time (T <sub>LS</sub> )	+260°C/30 seconds
ESD Rating, Human Body Model (Note 1)	1500V
ESD Rating, Charged Device Model (Note 1)	1000V

 $\dagger$  Notice: Stresses in excess of the Absolute Maximum Ratings can permanently damage the device. Functional operation is not implied at these or any other conditions in excess of conditions represented in the operational sections of this data sheet. Exposure to Absolute Maximum Ratings for extended periods may adversely affect device reliability. Permanent damage is also possible if E/D is applied before  $V_{DD}$ 

Note 1: Although ESD protection circuitry has been designed into the VC-820, proper precautions should be taken when handling and mounting. Microchip employs a Human Body Model (HBM) and a Charged Device Model (CDM) for ESD susceptibility testing and design protection evaluation. Human Body Model tested to MIL-STD-883, Method 3015 conditions. Charged Device Model tested to JESD22-C101 conditions.

## **ELECTRICAL CHARACTERISTICS, 3.3V OPTION**

Parameter	Sym.	Min.	Тур.	Max.	Units	Conditions
Supply						
Voltage	$V_{DD}$	3.15	3.3	3.45	V	Note 1
Max. Supply Voltage	_	-0.5	_	5.0	V	_
		_	_	6		≤20.000 MHz
		_	_	7		20.000 MHz to 39.999 MHz
		_	_	8		40.000 MHz to 49.999 MHz
Current (Note 2)	I <sub>DD</sub>	_	_	9	mA	50.000 MHz to 79.999 MHz
				10		80.000 MHz to 99.999 MHz
		_	_	40		100.000 MHz to 133.000 MHz
Current, Output Disabled	_	_	_	5	μΑ	

- **Note 1:** The power supply should have by-pass capacitors as close to the supply and to ground as possible, for example 0.1 uF and 0.01 uF.
  - 2: Parameters are tested with the test circuit shown in Figure 1-1.
  - 3: See Standard Frequencies and Ordering Information tables for more specific information.
  - **4:** Includes initial accuracy, operating temperature, supply voltage, shock and vibration (not under operation) and aging.
  - 5: Duty Cycle is measured as On Time/Period, see Figure 1-2.
  - 6: Broadband Period Jitter measured using Wavecrest SIA3300C, 90K samples.
  - 7: The output is enabled if the Enable/Disable is left open.
  - 8: Only ±50 ppm and ±100 ppm stability options are available for -40/+105 °C, -40/+125 °C, -55/+105 °C, and -55/+125 °C temperature range.

## **ELECTRICAL CHARACTERISTICS, 3.3V OPTION (CONTINUED)**

Parameter	Sym.	Min.	Тур.	Max.	Units	Conditions
Frequency		•				
Nominal Frequency	f <sub>NOM</sub>	0.032768	_	133.000	MHz	Note 3
		_	_	±20		
Stability (Note 4, Note 8)		_	_	±25	nnm	Ordering Option
Stability (Note 4, Note 6)		_	_	±50	ppm	Ordering Option
		_	_	±100		
Outputs						
Output Logic Level High, < 40 MHz	V <sub>OH</sub>	0.9 × V <sub>DD</sub>	_		V	
Output Logic Level Low, < 40 MHz	V <sub>OL</sub>	_	_	0.1 × V <sub>DD</sub>	V	Note 0
Output Logic High Drive, < 40 MHz	I <sub>OH</sub>	4	_	_	A	Note 2
Output Logic Low Driver, < 40 MHz	I <sub>OL</sub>	4	_	_	mA	
Output Logic Level High, 40.00 MHz–99.99 MHz	V <sub>OH</sub>	V <sub>DD</sub> – 0.4	_	_	V	
Output Logic Level Low, 40.00 MHz–99.99 MHz	V <sub>OL</sub>	_	_	0.4	V	Note 0
Output Logic High Drive, 40.00 MHz–99.99 MHz	I <sub>OH</sub>	4	_	_	m A	Note 2
Output Logic Low Driver, 40.00 MHz–99.99 MHz	I <sub>OL</sub>	4	_	_	mA	
Output Logic Level High, 100.00 MHz–133.000 MHz	V <sub>OH</sub>	V <sub>DD</sub> – 0.4	_	_	V	
Output Logic Level Low, 100.00 MHz–133.000 MHz	V <sub>OL</sub>	_	_	0.4	V	Nete 0
Output Logic High Drive, 100.00 MHz–133.000 MHz	I <sub>OH</sub>	4	_	_	1	Note 2
Output Logic Low Driver, 100.00 MHz–133.000 MHz	I <sub>OL</sub>	4	_	_	mA	
Load	I <sub>OUT</sub>	_	_	15	pF	_
Output Rise/Fall Time (Note 2)	t <sub>R</sub> /t <sub>F</sub>	_		4	ns	_
Duty Cycle	_	45	50	55	%	Note 2, Note 5

- **Note 1:** The power supply should have by-pass capacitors as close to the supply and to ground as possible, for example 0.1 uF and 0.01 uF.
  - 2: Parameters are tested with the test circuit shown in Figure 1-1.
  - **3:** See Standard Frequencies and Ordering Information tables for more specific information.
  - **4:** Includes initial accuracy, operating temperature, supply voltage, shock and vibration (not under operation) and aging.
  - 5: Duty Cycle is measured as On Time/Period, see Figure 1-2.
  - **6:** Broadband Period Jitter measured using Wavecrest SIA3300C, 90K samples.
  - 7: The output is enabled if the Enable/Disable is left open.
  - 8: Only ±50 ppm and ±100 ppm stability options are available for -40/+105 °C, -40/+125 °C, -55/+105 °C, and -55/+125 °C temperature range.

## **ELECTRICAL CHARACTERISTICS, 3.3V OPTION (CONTINUED)**

Parameter	Sym.	Min.	Тур.	Max.	Units	Conditions	
Period Jitter, RMS		_	2.4	_		Note 6	
Period Jitter, Peak-to-Peak		_	20.2	_		Note 6	
Random Jitter	$\Phi_{J}$	_	2.4	_	ps	_	
Deterministic Jitter	<b>↓</b> J	_	0		Po	_	
RMS Jitter, 12 kHz–20 MHz, 125 MHz		_	0.06	0.3		_	
Enable/Disable	Enable/Disable						
Output Enable	$V_{IH}$	0.7 × V <sub>DD</sub>	_	_	٧	Note 7	
Output Disable	$V_{IL}$	_	_	0.3 × V <sub>DD</sub>	<b>V</b>	Note 7	
Disable Time	t <sub>D</sub>	_	_	150	ns	_	
Start-Up Time	t <sub>SU</sub>	_	_	5	ms	_	
		-10	_	+70			
		-40	_	+85			
On a wating a Tayon a water	-	-40	_	+105	°C	Ondonina Ontion	
Operating Temperature	T <sub>OP</sub>	-40	_	+125	°C	Ordering Option	
		-55		+105			
		<b>-</b> 55	_	+125			

- **Note 1:** The power supply should have by-pass capacitors as close to the supply and to ground as possible, for example 0.1 uF and 0.01 uF.
  - 2: Parameters are tested with the test circuit shown in Figure 1-1.
  - 3: See Standard Frequencies and Ordering Information tables for more specific information.
  - **4:** Includes initial accuracy, operating temperature, supply voltage, shock and vibration (not under operation) and aging.
  - 5: Duty Cycle is measured as On Time/Period, see Figure 1-2.
  - **6:** Broadband Period Jitter measured using Wavecrest SIA3300C, 90K samples.
  - 7: The output is enabled if the Enable/Disable is left open.
  - **8:** Only ±50 ppm and ±100 ppm stability options are available for -40/+105 °C, -40/+125 °C, -55/+105 °C, and -55/+125 °C temperature range.

## **ELECTRICAL CHARACTERISTICS, 2.5V OPTION**

Parameter	Sym.	Min.	Тур.	Max.	Units	Conditions
Supply						
Voltage	$V_{DD}$	2.375	2.5	2.625	V	Note 1
Max. Supply Voltage	_	-0.5	_	5.0	V	_
		_	_	4.5		≤20.000 MHz
		_	_	5.5		20.000 MHz to 39.999 MHz
Current (Note 2)	I <sub>DD</sub>	_	_	7.0	mA	40.000 MHz to 79.999 MHz
		_	_	7.5		80.000 MHz to 99.999 MHz
				30.0		100.000 MHz to 125.000 MHz
Current, Output Disabled	_	_	_	5	μΑ	_
Frequency						
Nominal Frequency	f <sub>NOM</sub>	0.032768	_	125.000	MHz	Note 3
		_	_	±20		Oud aris a Oution
Stability (Note 4, Note 8)		_	_	±25	nnm	
Stability (Note 4, Note 6)	_	_	_	±50	ppm	Ordering Option
		_	_	±100		
Outputs						
Output Logic Level High, < 40 MHz	V <sub>OH</sub>	0.9 × V <sub>DD</sub>	_	_	M	
Output Logic Level Low, < 40 MHz	V <sub>OL</sub>	_	_	0.1 × V <sub>DD</sub>	V	Note 2, Note 3
Output Logic High Drive, < 40 MHz	I <sub>OH</sub>	4	_	_		
Output Logic Low Driver, < 40 MHz	l <sub>OL</sub>	4	_	_	mA	

- **Note 1:** The power supply should have by-pass capacitors as close to the supply and to ground as possible, for example 0.1 uF and 0.01 uF.
  - 2: Parameters are tested with the test circuit shown in Figure 3-1.
  - 3: See Standard Frequencies and Ordering Information tables for more specific information.
  - **4:** Includes initial accuracy, operating temperature, supply voltage, shock and vibration (not under operation) and aging.
  - 5: Duty Cycle is measured as On Time/Period, see Figure 4-1.
  - **6:** Broadband Period Jitter measured using Wavecrest SIA3300C, 90K samples.
  - 7: The output is enabled if the Enable/Disable is left open.
  - **8:** Only ±50 ppm and ±100 ppm stability options are available for -40/+105 °C, -40/+125 °C, -55/+105 °C, and -55/+125 °C temperature range.

## **ELECTRICAL CHARACTERISTICS, 2.5V OPTION (CONTINUED)**

Parameter	Sym.	Min.	Тур.	Max.	Units	Conditions
Output Logic Level High, 40.00 MHz–99.99 MHz	V <sub>OH</sub>	V <sub>DD</sub> - 0.4	_	_	V	
Output Logic Level Low, 40.00 MHz–99.99 MHz	V <sub>OL</sub>	_	1	0.4	V	Note 0
Output Logic High Drive, 40.00 MHz–99.99 MHz	I <sub>OH</sub>	4	1	_	A	Note 2
Output Logic Low Driver, 40.00 MHz–99.99 MHz	I <sub>OL</sub>	4		_	mA	
Output Logic Level High, 100.00 MHz–133.000 MHz	V <sub>OH</sub>	1.65	1	_	V	
Output Logic Level Low, 100.00 MHz–133.000 MHz	V <sub>OL</sub>	_	_	0.4	V	Note 0
Output Logic High Drive, 100.00 MHz–133.000 MHz	I <sub>OH</sub>	8	_	_	A	Note 2
Output Logic Low Driver, 100.00 MHz–133.000 MHz	I <sub>OL</sub>	8	_	_	mA	
Load	I <sub>OUT</sub>	_	_	15	pF	_
Output Rise/Fall Time	t <sub>R</sub> /t <sub>F</sub>	_	_	4	ns	Note 2
Duty Cycle	_	45	50	55	%	_
Period Jitter, RMS		_	2.4	_		Note 6
Period Jitter, Peak-to-Peak		_	20.2	_		Note 6
Random Jitter	Φ	_	2.4	_	ps	_
Deterministic Jitter	T YJ	_	0	_	рз	_
RMS Jitter, 12 kHz–20 MHz, 125 MHz		_	0.061	0.3		_
Enable/Disable						
Output Enable	V <sub>IH</sub>	0.7 × V <sub>DD</sub>	_	_	V	Note 7
Output Disable	V <sub>IL</sub>	_	_	0.3 × V <sub>DD</sub>	V	Note 7
Disable Time	t <sub>D</sub>	_	_	150	ns	_
Start-Up Time	t <sub>SU</sub>			5	ms	

- **Note 1:** The power supply should have by-pass capacitors as close to the supply and to ground as possible, for example 0.1 uF and 0.01 uF.
  - 2: Parameters are tested with the test circuit shown in Figure 3-1.
  - 3: See Standard Frequencies and Ordering Information tables for more specific information.
  - **4:** Includes initial accuracy, operating temperature, supply voltage, shock and vibration (not under operation) and aging.
  - 5: Duty Cycle is measured as On Time/Period, see Figure 4-1.
  - **6:** Broadband Period Jitter measured using Wavecrest SIA3300C, 90K samples.
  - **7:** The output is enabled if the Enable/Disable is left open.
  - 8: Only ±50 ppm and ±100 ppm stability options are available for -40/+105 °C, -40/+125 °C, -55/+105 °C, and -55/+125 °C temperature range.

## **ELECTRICAL CHARACTERISTICS, 2.5V OPTION (CONTINUED)**

Parameter	Sym.	Min.	Тур.	Max.	Units	Conditions	
		-10	_	+70			
		-40	_	+85			
On and the Towns and the	T <sub>OP</sub>	-40	_	+105	00	Oud a visu su Oudi a sa	
Operating Temperature		IOP	-40	_	+125	°C	Ordering Option
		-55		+105			
		-55	_	+125			

- **Note 1:** The power supply should have by-pass capacitors as close to the supply and to ground as possible, for example 0.1 uF and 0.01 uF.
  - 2: Parameters are tested with the test circuit shown in Figure 3-1.
  - **3:** See Standard Frequencies and Ordering Information tables for more specific information.
  - **4:** Includes initial accuracy, operating temperature, supply voltage, shock and vibration (not under operation) and aging.
  - **5:** Duty Cycle is measured as On Time/Period, see Figure 4-1.
  - **6:** Broadband Period Jitter measured using Wavecrest SIA3300C, 90K samples.
  - 7: The output is enabled if the Enable/Disable is left open.
  - **8:** Only ±50 ppm and ±100 ppm stability options are available for -40/+105 °C, -40/+125 °C, -55/+105 °C, and -55/+125 °C temperature range.

## **ELECTRICAL CHARACTERISTICS, 1.8V OPTION**

Parameter	Sym.	Min.	Тур.	Max.	Units	Conditions
Supply						
Voltage	$V_{DD}$	1.71	1.8	1.89	>	Note 1
Max. Supply Voltage	_	-0.5		3.6	>	_
		_		2.5		≤40.000 MHz
		_		3.5		40.000 MHz to 49.999 MHz
Current (Note 2)	I <sub>DD</sub>	_	1	6.5	mA	50.000 MHz to 79.999 MHz
		_	_	7		80.000 MHz to 99.999 MHz
				20		100.000 MHz to 125.000 MHz
Current, Output Disabled	_	_	_	5	μA	_
Frequency						
Nominal Frequency	f <sub>NOM</sub>	0.032768		125.000	MHz	Note 3
		_	_	±20		
Stability (Note 4, Note 8)		_		±25	nnm	Ordering Option
Stability (Note 4, Note 6)		_		±50	ppm	Ordering Option
		_	_	±100		
Outputs						
Output Logic Level High, < 40 MHz	V <sub>OH</sub>	0.9 × V <sub>DD</sub>	1	_	W	
Output Logic Level Low, < 40 MHz	V <sub>OL</sub>	_	_	0.1 × V <sub>DD</sub>	V	Note 2
Output Logic High Drive, < 40 MHz	I <sub>OH</sub>	2.8	_	_	A	
Output Logic Low Driver, < 40 MHz	l <sub>OL</sub>	2.8	_	_	mA	

- **Note 1:** The power supply should have by-pass capacitors as close to the supply and to ground as possible, for example 0.1 uF and 0.01 uF.
  - 2: Parameters are tested with the test circuit shown in Figure 3-1.
  - 3: See Standard Frequencies and Ordering Information tables for more specific information.
  - **4:** Includes initial accuracy, operating temperature, supply voltage, shock and vibration (not under operation) and aging.
  - 5: Duty Cycle is measured as On Time/Period, see Figure 4-1.
  - **6:** Broadband Period Jitter measured using Wavecrest SIA3300C, 90K samples.
  - **7:** The output is enabled if the Enable/Disable is left open.
  - **8:** Only ±50 ppm and ±100 ppm stability options are available for -40/+105 °C, -40/+125 °C, -55/+105 °C, and -55/+125 °C temperature range.

## **ELECTRICAL CHARACTERISTICS, 1.8V OPTION (CONTINUED)**

Parameter	Sym.	Min.	Тур.	Max.	Units	Conditions
Output Logic Level High, 40.00 MHz–125.00 MHz	V <sub>OH</sub>	V <sub>DD</sub> - 0.4	_	_	.,	
Output Logic Level Low, 40.00 MHz–125.00 MHz	V <sub>OL</sub>	_	_	0.4	V	Note 0
Output Logic High Drive, 40.00 MHz–125.00 MHz	I <sub>OH</sub>	4	_	_	A	Note 2
Output Logic Low Driver, 40.00 MHz–125.00 MHz	I <sub>OL</sub>	4	_	_	mA	
Load	I <sub>OUT</sub>	_	_	15	pF	_
Output Rise/Fall Time	t <sub>R</sub> /t <sub>F</sub>	_	_	5	ns	Note 2
Duty Cycle	_	45	50	55	%	Note 2, Note 5
Period Jitter, RMS		_	2.4	_		Note 6
Period Jitter, Peak-to-Peak		_	20.2	_	ps	Note 6
Random Jitter	Фл	_	2.4	_		_
Deterministic Jitter	ΨJ	_	0	_		_
RMS Jitter, 12 kHz–20 MHz, 125 MHz		_	0.4	0.9		_
Enable/Disable						
Output Enable	V <sub>IH</sub>	0.7 × V <sub>DD</sub>	_	_	V	Note 7
Output Disable	V <sub>IL</sub>	_	_	0.3 × V <sub>DD</sub>	V	Note 7
Disable Time	t <sub>D</sub>	_	_	150	ns	_
Start-Up Time	t <sub>SU</sub>	_	_	5	ms	_
		-10	_	+70		
		-40	_	+85		
On another a Teneral (	_	-40	_	+105		Ordering Option
Operating Temperature	T <sub>OP</sub>	-40	_	+125	°C	
		-55		+105		
		-55	_	+125		

- **Note 1:** The power supply should have by-pass capacitors as close to the supply and to ground as possible, for example 0.1 uF and 0.01 uF.
  - 2: Parameters are tested with the test circuit shown in Figure 3-1.
  - 3: See Standard Frequencies and Ordering Information tables for more specific information.
  - **4:** Includes initial accuracy, operating temperature, supply voltage, shock and vibration (not under operation) and aging.
  - 5: Duty Cycle is measured as On Time/Period, see Figure 4-1.
  - **6:** Broadband Period Jitter measured using Wavecrest SIA3300C, 90K samples.
  - **7:** The output is enabled if the Enable/Disable is left open.
  - 8: Only  $\pm 50$  ppm and  $\pm 100$  ppm stability options are available for -40/+105 °C, -40/+125 °C, -55/+105 °C, and -55/+125 °C temperature range.

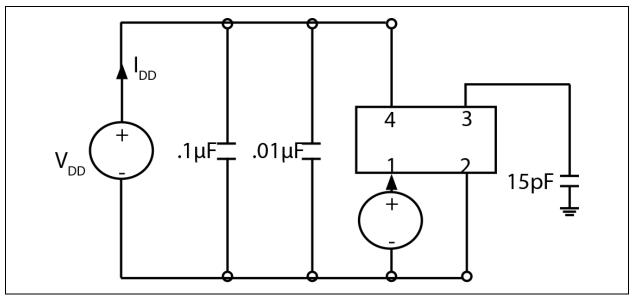


FIGURE 1-1: TEST CIRCUIT.

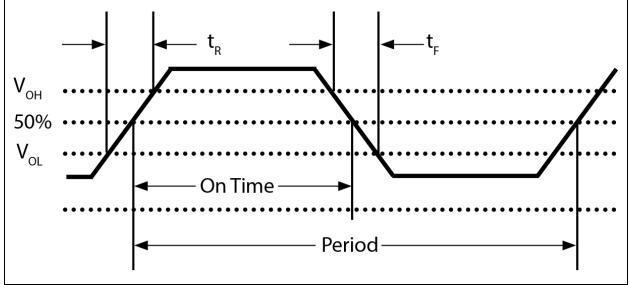


FIGURE 1-2: WAVEFORM.

## 2.0 PIN DESCRIPTIONS

The descriptions of the pins are listed in Table 2-1.

TABLE 2-1: PIN FUNCTION TABLE

Pin Number	Pin Name	Description
1	E/D	Enable/Disable
2	GND	Case and Electrical Ground
3	Output	Output
4	$V_{DD}$	Power Supply Voltage

## TABLE 2-2: ENABLE/DISABLE FUNCTION

E/D Pin	Output
High	Clock Output
Open	Clock Output
Low	High Impedance

#### 3.0 RELIABILITY

Microchip qualification includes aging at various extreme temperatures, shock and vibration, temperature cycling, and IR reflow simulation. The VC-820 family is capable of meeting the following qualification tests.

TABLE 3-1: ENVIRONMENTAL COMPLIANCE

Parameter	Conditions
Mechanical Shock	MIL-STD-883, Method 2002
Mechanical Vibration	MIL-STD-883, Method 2007
Solderability	MIL-STD-883, Method 2003
Gross and Fine Leak	MIL-STD-883, Method 1014
Resistance to Solvents	MIL-STD-883, Method 2015
Moisture Sensitivity Level	MSL 1
Contact Pads	Gold (0.3 μm min. to 1.0 μm max.) over Nickel
Weight	27 mg

#### 4.0 IR REFLOW

The VC-820 is qualified to meet the JEDEC standard for Pb-Free assembly. The temperatures and time intervals listed are based on the Pb-Free small body requirements. The VC-820 device is hermetically sealed, so an aqueous wash is not an issue.

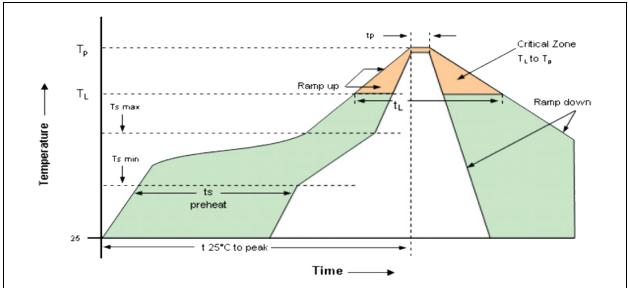


FIGURE 4-1: Solder Profile.

TABLE 4-1: REFLOW PROFILE

Symbol	Minimum	Maximum	Conditions
T <sub>S</sub>	150°C	200°C	
t <sub>S</sub>	60 seconds	260 seconds	
R <sub>UP</sub>	_	3°C per second	
t <sub>L</sub>	60 seconds	150 seconds	Pb-Free
T <sub>AMB-P</sub>	_	480 seconds	
t <sub>P</sub>	_	30 seconds	
R <sub>DN</sub>	_	6°C per second	

## 5.0 TAPE AND REEL

TABLE 5-1: TAPE AND REEL DIMENSIONS

Tape Dimensions (mm)					Reel Dimensions (mm)								
Dimension	W	F	Do	Ро	P1	Α	В	С	D	N	W1	W2	# per
Tolerance	Тур.	Тур.	Тур.	Тур.	Тур.	Тур.	Min.	Тур.	Min.	Min.	Тур.	Max.	Reel
VC-820	8	3.5	1.5	4	4	175	2	13	21	60	10	14	3000

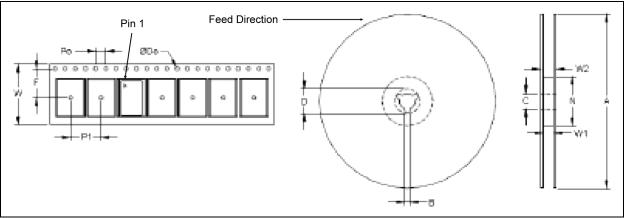


FIGURE 5-1: Tape and Reel.

Note: Pin 1 and feed direction are standard per EIA-481

## 5.1 Standard Output Frequencies in MHz

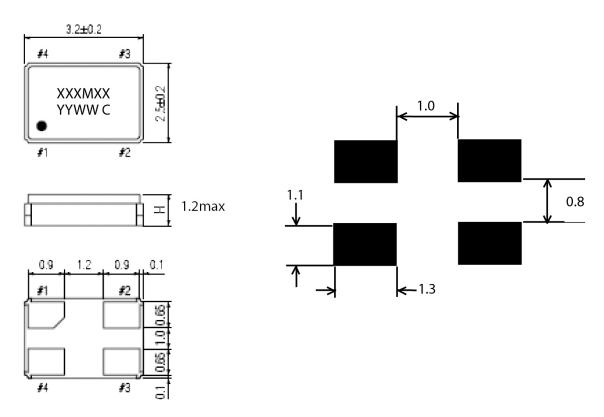
- 0.032768
- 0.625000
- 2.000
- 4.000
- 8.000
- 10.000
- 10.700
- 14.31818
- 16.000
- 16.384
- 16.875
- 18.432
- 20.000
- 24.000
- 24.576
- 25.000
- 25.0125
- 26.000
- 27.00028.63630
- 20.00000
- 29.4912
- 30.000

- 31.250
- 31.700
- 32.000
- 33.000
- 33.333000
- 35.328
- 40.000
- 43.675771
- 48.000
- 50.000
- 62.500
- 64.000
- 04.000
- 66.66600075.000
- 80.000
- 93.750
- . . . . . . .
- 100.000
- 106.250
- 108.000
- 114.285
- 125.000
- 133.000

## 6.0 PACKAGING INFORMATION

# 4-Lead 3.2 mm $\times$ 2.5 mm $\times$ 1.2 mm VDFN [FEC] Package Outline and Recommended Land Pattern

**Note:** For the most current package drawings, please see the Microchip Packaging Specification located at http://www.microchip.com/packaging



Dimensions in mm

# APPENDIX A: REVISION HISTORY

# Revision A (April 2024)

- Converted Vectron document VC-820 to Microchip data sheet template DS20006895A.
- Minor grammatical text changes throughout.

1	I 1		-8	7	$\mathbf{\Omega}$
V	Ц	او	-0	Z	U

NOTES:

# PRODUCT IDENTIFICATION SYSTEM

To order or obtain information, e.g., on pricing or delivery, contact your local Microchip representative or sales office.

XX-XXX	<u>-X</u>		<u>X</u>	<u>X</u>	<u>-X</u>	<u>x</u>	X	<u>X</u>	-xxXxxxxxxx	<u>XX</u>
Device	Power Supply	O	utput	Temperature Range	Stability	Enable/Disable	Load	Custom Options	Frequency	Packaging
Device:	VC-820			Oscillator as 3.		mm ×	Exam	ples:		
			1.2 11111	rocialillo VBI IV	•		a)	VC-820-EA7-KAAN-	1M00000000TR	
_	E	=	3.3VD0	2					Supply, CMOS, -40	
Power Supply:	Н	=	2.5VD0						m and ±100 ppm o e High, 15 pF Load	
Supply.	J	=	1.8VD0						e підп, то рг Load MHz Frequency, 3,	
							b)	VC-820-EAB-KAAN-	10M000000	
Output:	Α	=	CMOS					3 3VDC Power 9	Supply, CMOS, -5	5°C to
									m and ±100 ppm c	
	W		_10°C	to +70°C					e High, 15 pF Load	
	Ë			to +85°C				Option, 10.0000	MHz Frequency, 1	100/Reel
Temp.	F	_		to +105°C (±50	ppm and ±1	100 ppm only)	c)	VC-820-EAW-SAAN	-44M2368000	
Range:	7			to +125°C (±50			,	3 3VDC Power 9	Supply, CMOS, -10	0°C to +70°C
	В			to +105°C (±50					ble High, 15 pF Loa	
	С		–55°C 1	to +125°C (±50	ppm and ±1	100 ppm only)			MHz Frequency, 1	
							d)	VC-820-HAC-KAAN-	125M0000000	
	E		±20 pp				,	2 5VDC Power 9	Supply, CMOS, -5	5°C to
Stability:	F		±25 pp						m and ±100 ppm c	
	K S		±50 pp						e High, 15 pF Load	
	3	_	±100 p	pili				Option, 125.000	0 MHz Frequency,	100/Reel
							e)	VC-820-JAE-FAAN-6	66M6660000TR	
Enable/ Disable:	Α	=	Enable	High				1.8VDC Power S	Supply, CMOS, -40	)°C to +85°C,
Disable:				_					e High, 15 pF Load	
								Option, 66.6660	MHz Frequency, 3	3,000/Reel
Load:	Α	=	15 pF							
Custom	N	_	Ctanda	rd Ontion						
Options:	N	=	Standa	rd Option			Note	1: Tape and Ree	l identifier only app	ears in the
							Note		ımber description.	
			F	NALI=					ering purposes and	
Frequency:	xxMxxxxxxxx								package. Check w	
	***********	_	ricque	IIOy III KI IZ					ice for package av	ailability with
								the Tape and F	Reel option. ris 10 digits long in	cluding M fo
Packaging:	TR			Reel (standard 1					ris 10 digits long in kHz, and the prefi:	
. ackaging.	<blaue></blaue>	=	100/Re	el (non-standar	d Tape & Re	eel)		or 3 digits long		A Call DE 1, Z

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NOTES:

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