

CMOS Crystal Oscillator

Features

- Ultra Low Jitter, Fundamental or 3rd OT Crystal Design
- · CMOS Output Crystal Oscillator
- Output Frequencies from 1.024 MHz to 160.000 MHz
- +1.8, +2.5, +3.3 or +5.0V Operation
- · Output Disable Feature
- · Excellent ±20 ppm Temperature Stability
- -10/70°C to -55/125°C Operating Temperature options
- Small Industry Standard Package, 3.2 × 2.5 mm (Product is compliant to RoHS directive and fully compatible with lead free assembly, excluding solder dipped, _SNPB, option.)

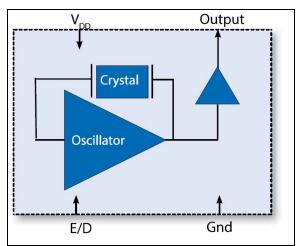
Applications

- · SONET/SDH/DWDM
- · Ethernet, GE, SynchE
- · Storage Area Networking
- · Fiber Channel
- Digital Video
- · Broadband Access
- · Base Stations, Picocells

General Description

Microchip's VC-820A Crystal Oscillator (XO) is a quartz stabilized square wave generator with a CMOS output. The VC-820A uses a fundamental or a 3rd overtone crystal, oscillating in a fundamental tone, resulting in very low jitter performance, and a monolithic IC which improves reliability and reduces cost.

Block Diagram



1.0 ELECTRICAL CHARACTERISTICS

Absolute Maximum Ratings †

| Storage Temperature (T _S) | –55°C to +125°C |
|---|-----------------|
| Soldering Temperature, 30 seconds (T _{LS}) | +260°C |
| ESD Rating (Human Body Model, JES22-A115 Conditions, Note 1) | 400V |
| ESD Rating (Charged Device Model, JESD22-C101E Conditions, Note 1 |)2 kV |

† Notice: Stresses in excess of the absolute maximum ratings can permanently damage the device. Functional operation is not implied at these or any other conditions in excess of conditions represented in the operational sections of this data sheet. Exposure to absolute maximum ratings for extended periods may adversely affect device reliability. Permanent damage is also possible if Enable/Disable is applied before V_{DD}.

Note 1: Although ESD protection circuitry has been designed into the VC-820A, proper precautions should be taken when handling and mounting. Microchip employs a human body model (HBM) and a charged device model (CDM) for ESD susceptibility testing and design protection evaluation.

ELECTRICAL CHARACTERISTICS, 5.0V OPTION

| Parameter | Symbol | Min. | Тур. | Max. | Units | Conditions |
|--------------------------------|--------------------------------|-----------------------|------|-----------------------|-------|-----------------------|
| Supply | | | | | | |
| Voltage (Note 1) | V_{DD} | 4.5 | 5.0 | 5.5 | V | _ |
| Max. Supply Voltage | _ | -0.5 | _ | 6.5 | V | _ |
| Max. Voltage E/D | _ | -0.5 | _ | V _{DD} + 0.5 | V | _ |
| | | _ | _ | 5 | | ≤12 MHz |
| | | _ | _ | 13 | | 12.001 MHz to 20 MHz |
| Current (Note 2) | I _{DD} | _ | _ | 18 | mA | 20.001 MHz to 40 MHz |
| | | _ | _ | 21 | | 40.001 MHz to 65 MHz |
| | | _ | _ | 30 | | 65.001 MHz to 100 MHz |
| Current | I _{DD} | _ | _ | 10 | μA | Output Disabled |
| Frequency | | | | | | |
| Nominal Frequency | f _{NOM} | 1.024 | | 100.000 | MHz | _ |
| | f _{STAB} | _ | ±20 | _ | ppm | |
| Frequency Stability (Note 3) | | _ | ±25 | _ | | Ordering option |
| Frequency Stability (Note 3) | | _ | ±50 | _ | | Ordering option |
| | | _ | ±100 | _ | | |
| Outputs | | | | | | |
| Output Logic Level High | V _{OH} | 0.9 × V _{DD} | _ | _ | V | Note 2 |
| Output Logic Level Low | V_{OL} | _ | | 0.1 × V _{DD} | V | Note 2 |
| Load | I _{OUT} | _ | 15 | 30 | pF | _ |
| Outnot Diss/Fall Times | | _ | _ | 8 | | ≤20 MHz |
| Output Rise/Fall Time (Note 2) | t _r /t _f | _ | _ | 5 | ns | 20.001 MHz to 50 MHz |
| (11010 2) | | _ | | 3 | | 50.001 MHz to 100 MHz |
| Output Leakage | I _Z | _ | _ | ±10 | μA | Output disabled |
| Duty Cycle | DC | 45 | 50 | 55 | % | Note 2, Note 4 |
| Period Jitter (Note 5) | φ. | _ | 1.7 | _ | ne | 100 MHz, RMS |
| T GITOG JILLET (TVOLE J) | фЈ | _ | 16 | _ | ps | 100 MHz, peak-to-peak |
| RMS Jitter (Note 6) | фЈ | _ | 65 | 100 | fs | 12 kHz to 20 MHz |

ELECTRICAL CHARACTERISTICS, 5.0V OPTION (CONTINUED)

| Parameter | Symbol | Min. | Тур. | Max. | Units | Conditions |
|--------------------------------|-----------------|-----------------------|------|------|-------|-----------------|
| Enable/Disable | | | | | | |
| Output Enable Voltage | V_{IH} | 0.7 × V _{DD} | _ | _ | V | Note 7 |
| Output Disable Voltage | V _{IL} | _ | _ | 0.4 | V | Note / |
| Disable Time | t _D | _ | _ | 100 | ns | _ |
| Start-Up Time | t _{SU} | _ | _ | 10 | ms | _ |
| | | -10 | _ | +70 | | Ordering option |
| | | -40 | _ | +85 | | |
| Operating Temperature Range | T _{OP} | -40 | _ | +105 | °C | |
| | | -40 | _ | +125 | | |
| | | -55 | _ | +125 | | |

- **Note 1:** The power supply should have bypass capacitors as close to the supply and to ground as possible. For example, 0.1 μF and 0.01 μF.
 - 2: Parameters are tested with the test circuit shown in Figure 1-1.
 - **3:** Includes initial accuracy, operating temperature, supply voltage, shock and vibration (not under operation), and 10 years' aging for ±50 ppm and ±100 ppm options.
 - 4: Duty cycle is measured as On-Time/Period. See Figure 1-2.
 - **5:** Broadband period jitter measured using a LeCroy Waverunner 610Zi, 100k samples.
 - 6: Measured using an Agilent E5052 or equivalent at 100 MHz and +25°C.
 - 7: The output is enabled if Enable/Disable is left open. A 10 k Ω pull-up to V_{DD} is recommended.

ELECTRICAL CHARACTERISTICS, 3.3V OPTION

| Parameter | Symbol | Min. | Тур. | Max. | Units | Conditions |
|------------------------------|-------------------|-------|------|-----------------------|-------|------------------------|
| Supply | | | | <u> </u> | | |
| Voltage (Note 1) | V_{DD} | 2.97 | 3.3 | 3.63 | V | _ |
| Max. Supply Voltage | _ | -0.5 | _ | 6.5 | V | _ |
| Max. Voltage E/D | _ | -0.5 | _ | V _{DD} + 0.5 | V | _ |
| | | _ | _ | 3 | | ≤12 MHz |
| | | _ | _ | 4 | | 12.001 MHz to 20 MHz |
| | | _ | _ | 8 | | 20.001 MHz to 40 MHz |
| Current (Note 2) | I _{DD} | _ | _ | 18 | mA | 40.001 MHz to 65 MHz |
| | | _ | _ | 25 | | 65.001 MHz to 100 MHz |
| | | _ | _ | 30 | | 100.001 MHz to 133 MHz |
| | | _ | _ | 40 | | 133.001 MHz to 160 MHz |
| Current | I _{DD} | _ | _ | 10 | μA | Output Disabled |
| Frequency | | | | | | |
| Nominal Frequency | f _{NOM} | 1.024 | _ | 160.000 | MHz | _ |
| | | _ | ±20 | _ | | |
| [| f | | ±25 | | nnm | Ordering ention |
| Frequency Stability (Note 3) | f _{STAB} | _ | ±50 | _ | ppm | Ordering option |
| | | _ | ±100 | _ | | |

ELECTRICAL CHARACTERISTICS, 3.3V OPTION (CONTINUED)

| Parameter | Symbol | Min. | Тур. | Max. | Units | Conditions |
|--------------------------------|--------------------------------|-----------------------|------|-----------------------|-------|-----------------------|
| Outputs | | | | | | |
| Output Logic Level High | V _{OH} | 0.9 × V _{DD} | _ | _ | V | Note 2 |
| Output Logic Level Low | V _{OL} | _ | _ | 0.1 × V _{DD} | ٧ | Note 2 |
| Load | I _{OUT} | _ | 15 | 30 | pF | _ |
| 0 (10 /5 /5 /17 | | _ | _ | 8 | | ≤20 MHz |
| Output Rise/Fall Time (Note 2) | t _r /t _f | _ | _ | 5 | ns | 20.001 MHz to 50 MHz |
| (Note 2) | | _ | _ | 3 | | 50.001 MHz to 160 MHz |
| Output Leakage | I _Z | _ | _ | ±10 | μA | Output disabled |
| Duty Cycle | DC | 45 | 50 | 55 | % | Note 2, Note 4 |
| David Litter (Nata 5) | 1 | _ | 2.3 | | | 100 MHz, RMS |
| Period Jitter (Note 5) | фЈ | _ | 21 | _ | ps | 100 MHz, peak-to-peak |
| RMS Jitter (Note 6) | фЈ | _ | 76 | 115 | fs | 12 kHz to 20 MHz |
| Enable/Disable | | | | | | |
| Output Enable Voltage | V _{IH} | 0.7 × V _{DD} | _ | _ | V | Note 7 |
| Output Disable Voltage | V _{IL} | _ | _ | 0.4 | V | Note / |
| Disable Time | t _D | _ | _ | 100 | ns | _ |
| Start-Up Time | t _{SU} | _ | _ | 10 | ms | _ |
| | | -10 | _ | +70 | | |
| 0 " T | | -40 | _ | +85 | | |
| Operating Temperature Range | T _{OP} | -40 | _ | +105 | °C | Ordering option |
| | | -40 | _ | +125 | | |
| | | - 55 | _ | +125 | | |

Note 1: The power supply should have bypass capacitors as close to the supply and to ground as possible. For example, 0.1 μ F and 0.01 μ F.

- 2: Parameters are tested with the test circuit shown in Figure 1-1.
- **3:** Includes initial accuracy, operating temperature, supply voltage, shock and vibration (not under operation), and 10 years' aging for ±50 ppm and ±100 ppm options.
- 4: Duty cycle is measured as On-Time/Period. See Figure 1-2.
- **5:** Broadband period jitter measured using a LeCroy Waverunner 610Zi, 100k samples.
- **6:** Measured using an Agilent E5052 or equivalent at 100 MHz and +25°C.
- 7: The output is enabled if Enable/Disable is left open. A 10 k Ω pull-up to V_{DD} is recommended.

ELECTRICAL CHARACTERISTICS, 2.5V OPTION

| Parameter | Symbol | Min. | Тур. | Max. | Units | Conditions |
|--------------------------------|--------------------------------|-----------------------|------|-----------------------|-------|------------------------|
| Supply | | | | | | |
| Voltage (Note 1) | V_{DD} | 2.25 | 2.5 | 2.75 | V | _ |
| Max. Supply Voltage | _ | -0.5 | _ | 6.5 | V | _ |
| Max. Voltage E/D | _ | -0.5 | _ | V _{DD} + 0.5 | V | _ |
| | | _ | _ | 2 | | ≤12 MHz |
| | | _ | _ | 3 | | 12.001 MHz to 20 MHz |
| | | _ | _ | 7 | | 20.001 MHz to 40 MHz |
| Current (Note 2) | I _{DD} | _ | | 12 | mA | 40.001 MHz to 65 MHz |
| | | _ | _ | 18 | | 65.001 MHz to 100 MHz |
| | | _ | | 21 | | 100.001 MHz to 133 MHz |
| | | _ | _ | 30 | | 133.001 MHz to 160 MHz |
| Current | I _{DD} | _ | _ | 10 | μΑ | Output Disabled |
| Frequency | • | | | • | | |
| Nominal Frequency | f _{NOM} | 1.024 | _ | 160.000 | MHz | _ |
| | | _ | ±20 | _ | - ppm | |
| F | | _ | ±25 | _ | | |
| Frequency Stability (Note 3) | f _{STAB} | _ | ±50 | _ | | Ordering option |
| | | _ | ±100 | _ | | |
| Outputs | • | | | • | | |
| Output Logic Level High | V _{OH} | 0.9 × V _{DD} | _ | _ | V | Note 2 |
| Output Logic Level Low | V _{OL} | _ | _ | 0.1 × V _{DD} | V | Note 2 |
| Load | I _{OUT} | _ | 15 | 30 | pF | _ |
| O 1 15: /5 T | | _ | _ | 8 | | ≤20 MHz |
| Output Rise/Fall Time (Note 2) | t _r /t _f | _ | _ | 5 | ns | 20.001 MHz to 50 MHz |
| (Note 2) | | _ | _ | 4 | | 50.001 MHz to 160 MHz |
| Output Leakage | IZ | _ | _ | ±10 | μΑ | Output disabled |
| Duty Cycle | DC | 45 | 50 | 55 | % | Note 2, Note 4 |
| Period Jitter, 100 MHz | | _ | 2.8 | _ | n - | RMS |
| (Note 5) | фЈ | _ | 26 | _ | ps | Peak-to-peak |
| RMS Jitter (Note 6) | фЈ | _ | 97 | 145 | fs | 12 kHz to 20 MHz |

ELECTRICAL CHARACTERISTICS, 2.5V OPTION (CONTINUED)

| Parameter | Symbol | Min. | Тур. | Max. | Units | Conditions |
|-----------------------------|-----------------|-----------------------|------|------|-------|-----------------|
| Enable/Disable | | | | | | |
| Output Enable Voltage | V _{IH} | 0.7 × V _{DD} | _ | _ | V | Note 7 |
| Output Disable Voltage | V _{IL} | _ | _ | 0.4 | V | Note 7 |
| Disable Time | t _D | _ | _ | 100 | ns | _ |
| Start-Up Time | t _{SU} | _ | _ | 10 | ms | _ |
| | | -10 | _ | +70 | | |
| O " T ' | | -40 | _ | +85 | | |
| Operating Temperature Range | T _{OP} | -40 | _ | +105 | °C | Ordering option |
| range | | -40 | _ | +125 | | |
| | | -55 | _ | +125 | | |

- Note 1: The power supply should have bypass capacitors as close to the supply and to ground as possible. For example, 0.1 μF and 0.01 μF.
 - 2: Parameters are tested with the test circuit shown in Figure 1-1.
 - 3: Includes initial accuracy, operating temperature, supply voltage, shock and vibration (not under operation), and 10 years' aging for ±50 ppm and ±100 ppm options.
 - 4: Duty cycle is measured as On-Time/Period. See Figure 1-2.
 - 5: Broadband period jitter measured using a LeCroy Waverunner 610Zi, 100k samples.
 - **6:** Measured using an Agilent E5052 or equivalent at 100 MHz and +25°C.
 - 7: The output is enabled if Enable/Disable is left open. A 10 k Ω pull-up to V_{DD} is recommended.

ELECTRICAL CHARACTERISTICS, 1.8V OPTION

| Parameter | Symbol | Min. | Тур. | Max. | Units | Conditions |
|------------------------------|-------------------|-----------------------|------|-----------------------|-------|------------------------|
| Supply | | | | | | |
| Voltage (Note 1) | V_{DD} | 1.71 | 1.8 | 1.89 | V | _ |
| Max. Supply Voltage | _ | -0.5 | _ | 6.5 | V | _ |
| Max. Voltage E/D | _ | -0.5 | _ | V _{DD} + 0.5 | V | _ |
| | | _ | _ | 2 | | ≤12 MHz |
| | | _ | _ | 3 | | 12.001 MHz to 20 MHz |
| Current (Note 2) | I _{DD} | _ | _ | 11 | mA | 20.001 MHz to 65 MHz |
| | | _ | _ | 18 | | 65.001 MHz to 133 MHz |
| | | _ | _ | 25 | | 133.001 MHz to 160 MHz |
| Current | I _{DD} | _ | _ | 10 | μA | Output Disabled |
| Frequency | | | | | | |
| Nominal Frequency | f _{NOM} | 1.024 | _ | 160.000 | MHz | _ |
| | | _ | ±20 | _ | | |
| Fraguency Stability (Note 2) | f | _ | ±25 | _ | nnm | Ordering ention |
| Frequency Stability (Note 3) | f _{STAB} | _ | ±50 | _ | ppm | Ordering option |
| | | _ | ±100 | _ | | |
| Outputs | | | | | | |
| Output Logic Level High | V _{OH} | 0.9 × V _{DD} | _ | _ | V | Note 2 |
| Output Logic Level Low | V _{OL} | _ | _ | 0.1 × V _{DD} | V | Note 2 |
| Load | I _{OUT} | _ | 15 | 30 | pF | _ |

ELECTRICAL CHARACTERISTICS, 1.8V OPTION (CONTINUED)

| Parameter | Symbol | Min. | Тур. | Max. | Units | Conditions |
|--------------------------------|--------------------------------|-----------------------|------|------|-------|-----------------------|
| O + + D: /E !! T | | _ | _ | 8 | | ≤20 MHz |
| Output Rise/Fall Time (Note 2) | t _r /t _f | _ | _ | 5 | ns | 20.001 MHz to 50 MHz |
| (Note 2) | | _ | _ | 5 | | 50.001 MHz to 160 MHz |
| Output Leakage | I _Z | _ | _ | ±10 | μA | Output disabled |
| Duty Cycle | DC | 45 | 50 | 55 | % | Note 2, Note 4 |
| Period Jitter, 100 MHz | 4 | _ | 3.6 | _ | no | RMS |
| (Note 5) | фЈ | _ | 35 | _ | ps | Peak-to-peak |
| RMS Jitter (Note 6) | фЈ | _ | 212 | 320 | fs | 12 kHz to 20 MHz |
| Enable/Disable | | | | | | |
| Output Enable Voltage | V _{IH} | 0.7 × V _{DD} | _ | _ | V | Note 7 |
| Output Disable Voltage | V_{IL} | _ | _ | 0.4 | v | Note 7 |
| Disable Time | t _D | _ | _ | 100 | ns | _ |
| Start-Up Time | t _{SU} | _ | _ | 10 | ms | _ |
| | | -10 | _ | +70 | | |
| | | -40 | _ | +85 | | Ordering option |
| Operating Temperature Range | T _{OP} | -40 | _ | +105 | °C | |
| rango | | -40 | _ | +125 | | |
| | | -55 | _ | +125 | | |

- **Note 1:** The power supply should have bypass capacitors as close to the supply and to ground as possible. For example, $0.1 \mu F$ and $0.01 \mu F$.
 - 2: Parameters are tested with the test circuit shown in Figure 1-1.
 - **3:** Includes initial accuracy, operating temperature, supply voltage, shock and vibration (not under operation), and 10 years' aging for ±50 ppm and ±100 ppm options.
 - 4: Duty cycle is measured as On-Time/Period. See Figure 1-2.
 - 5: Broadband period jitter measured using a LeCroy Waverunner 610Zi, 100k samples.
 - 6: Measured using an Agilent E5052 or equivalent at 100 MHz and +25°C.
 - 7: The output is enabled if Enable/Disable is left open. A 10 k Ω pull-up to V_{DD} is recommended.

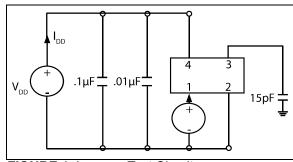


FIGURE 1-1: Test Circuit.

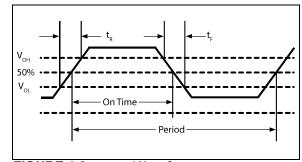


FIGURE 1-2: Waveform.

2.0 PIN DESCRIPTIONS

The descriptions of the pins are listed in Table 2-1.

TABLE 2-1: PIN FUNCTION TABLE

| Pin Number | Pin Name | Description |
|------------|----------|-----------------------------|
| 1 | E/D | Enable/Disable. |
| 2 | GND | Case and electrical ground. |
| 3 | Output | Output. |
| 4 | V_{DD} | Power supply voltage. |

TABLE 2-2: ENABLE/DISABLE FUNCTION

| E/D Pin | Output |
|---------|----------------|
| High | Clock Output |
| Open | Clock Output |
| Low | High Impedance |

3.0 RELIABILITY

Microchip qualification includes aging at various extreme temperatures, shock and vibration, temperature cycling, and IR reflow simulation. The VC-820A family is capable of meeting the following qualification tests:

TABLE 3-1: ENVIRONMENTAL COMPLIANCE

| Parameter | Conditions | | | |
|----------------------------|---|--|--|--|
| Mechanical Shock | MIL-STD-883, Method 2002 | | | |
| Mechanical Vibration | MIL-STD-883, Method 2007 | | | |
| Solderability | MIL-STD-883, Method 2003 | | | |
| Gross and Fine Leak | MIL-STD-883, Method 1014 | | | |
| Resistance to Solvents | MIL-STD-883, Method 2015 | | | |
| Moisture Sensitivity Level | MSL 1 | | | |
| Contact Pads | Gold (0.3 μm min. to 1 μm max.) over Nickel | | | |
| Contact Pads, _SNPB Option | Tinned using solder alloy Sn63Pb37 in accordance with J-STD-006 | | | |
| Weight | 27 mg | | | |

Although ESD protection circuitry has been designed into the VC-820A proper precautions should be taken when handling and mounting. Vectren employs a human body model (HBM) and a charged device model (COM) for ESD susceptibility testing and design protection evaluation.

TABLE 3-2: ESD RATINGS

| Model | Minimum | Conditions | | | | |
|----------------------|---------|--------------|--|--|--|--|
| Human Body Model | 400V | JES22-A115 | | | | |
| Charged Device Model | 2000V | JESD22-C101E | | | | |

Stresses in excess of the absolute maximum ratings can permanently damage the device. Functional operation is not implied at these or any other conditions in excess of conditions represented in the operational sections of this data sheet. Exposure to absolute maximum ratings for extended periods may adversely affect device reliability. Permanent damage is also possible if E/D is applied before V_{DD} .

TABLE 3-3: ABSOLUTE MAXIMUM RATINGS

| Parameter | Symbol | Ratings | Unit |
|------------------------------|-----------------|------------|--------------|
| Storage Temperature | T _S | -55 to 125 | °C |
| Soldering Temperature / Time | T _{LS} | 260 / 30 | °C / seconds |

4.0 IR REFLOW

The VC-820A is qualified to meet the JEDEC standard for Pb-Free assembly. The temperatures and time intervals listed are based on the Pb-Free small body requirements. The VC-820A device is hermetically sealed so an aqueous wash is not an issue. **Note:** Devices that have been solder dipped (_SNPB option) will not be Pb-Free.

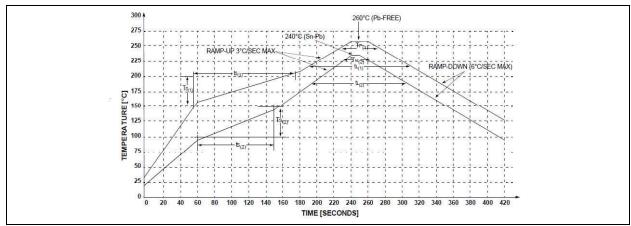


FIGURE 4-1: Reflow Profile.

TABLE 4-1: REFLOW PROFILE

| Symbol | Minimum | Maximum | Conditions | | |
|-------------------|---------|----------|--------------|--|--|
| T _{S(1)} | 150°C | 200°C | Pb-Free | | |
| T _{S(2)} | 100°C | 150°C | _SNPB Option | | |
| t _{s(1)} | 60 sec. | 180 sec. | Pb-Free | | |
| t _{s(2)} | 60 sec. | 120 sec. | _SNPB Option | | |
| t _{l(1)} | 60 sec. | 150 sec. | Pb-Free | | |
| t _{l(2)} | 60 sec. | 150 sec. | _SNPB Option | | |
| T _{p(1)} | 245°C | 260°C | Pb-Free | | |
| T _{p(2)} | 225°C | 240°C | _SNPB Option | | |

5.0 TAPE AND REEL

TABLE 5-1: TAPE AND REEL DIMENSIONS

| Tape Dimensions (mm) | | | | | Reel Dimensions (mm) | | | | | | | |
|----------------------|------|------|------|------|----------------------|----------------|------|------|------|------|------|------|
| Dimension | W | F | Do | Po | P1 | A B C D N W1 W | | | | | W2 | |
| Tolerance | Тур. | Тур. | Тур. | Тур. | Тур. | Тур. | Min. | Тур. | Min. | Min. | Тур. | Max. |
| VC-820A | 8.0 | 3.5 | 1.5 | 4.0 | 4.0 | 178 | 2.0 | 13.0 | 21.0 | 60.0 | 10 | 14 |

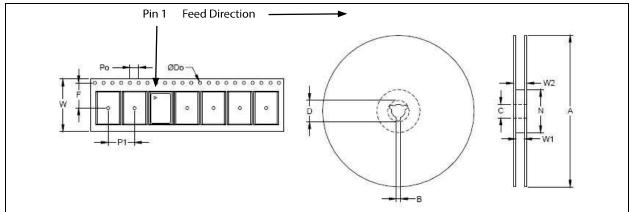
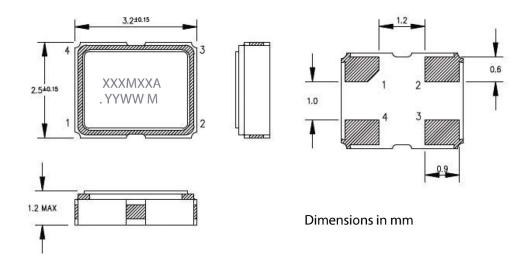


FIGURE 5-1: Tape and Reel.

6.0 PACKAGING INFORMATION

4-Lead VDFN 3.2 mm × 2.5 mm Package Outline and Recommended Land Pattern

Note: For the most current package drawings, please see the Microchip Packaging Specification located at http://www.microchip.com/packaging



Marking Information

XXXMXX =Frequency, eg 125M00 = 125.000MHz

A = Revision Level

YY = Year

WW = Week

M = Manufacturing Location, examples, C, C3, J1

APPENDIX A: REVISION HISTORY

Revision A (October 2022)

• Initial release of VC-820A as Microchip data sheet DS20006739A.



NOTES:

PRODUCT IDENTIFICATION SYSTEM

To order or obtain information, e.g., on pricing or delivery, contact your local Microchip representative or sales office.

| Part Number | <u>-X</u> | <u>x</u> | <u>x</u> | <u>-X</u> | <u>x</u> | 3 | <u>x</u> | <u>x</u> | xxMxx | xxxx | <u>xx</u> | |
|--------------------|--------------------------|----------|---|---------------|--------------------|----|----------|----------------------|-----------------------|---|---|--|
| Device | Power Supply | Output | Temp. Range | Stability | Enable/ Disable | Lo | ad | Custo | | ency | Media Type | |
| Device: | VC-820A: | C | :MOS Crystal | Oscillator ir | n 3.2 mm x | | E> | camples | | | | |
| Bevice. | E | | .5 mm Ceran | nic Package | | | a) |) VC-820A 50M0000 | -EAW-KAAN- 0000TR: | CMOS | OA, 3.3VDC Power Supply, Output, -10°C to +70°C Range, ±50 ppm Stability, | |
| Power Supply: | Н | | .5VDC .5VDC | | | | | | | | /Disable Enable High, | |
| Power Suppry. | J | | | | | | | | | | _oad, Standard Option, | |
| | J | - 1 | .8VDC | | | | | | | 50.000 | MHz, Tape and Reel | |
| Output: | A W | | :MOS 10°C to +70° | ^ | | | b) |) VC-820A 100M000 | | ply, CM +105°C Stability | DA, VDC Power Sup- IOS Output, _40°C to C Temp. Range, ± ppm y, Enable/Disable Enable pF Load, Standard | |
| | Ë | | 40°C to +85° | | | | | | | | _ pr 2000, Otanidard , 100.000 MHz, Cut Tape | |
| Temperature | F | = - | 40°C to +105 | °C (±50 ppn | | | C) |) VC-820A | -0051- | | OA, VDC Power Sup- | |
| Range: | 7 | | 40°C to +125 | | | | ٠, | | 0000TR: | | IOS Output, –40°C to | |
| | B C | | 55°C to +105 55°C to +125 | | | | | | | +105°C Stability | C Temp. Range, ± ppm y, Enable/Disable Enable pF Load, Standard | |
| | E F | | 20 ppm 25 ppm | | | | | | | | _ pr Load, Standard , 100.000 MHz, Tape and | |
| Stability: | K | | 50 ppm | | | | ١ | | | | | |
| | S | | 100 ppm | | | | No | р | art number des | cription. | only appears in the catalog This identifier is used for not printed on the device | |
| Enable/Disable: | Α | = E | nable/Disable | e, Enable Hi | gh | | | р | ackage. Check | k with your Microchip Sales Office for bility with the Tape and Reel option. | | |
| Load: | Α | = 1 | 5 pF | | | | | | | | | |
| Custom Options: | N | = S | tandard optic | n | | | | | | | | |
| Frequency: | xxMxxxxxx | | requency in N Brd character | | | | | | | | | |
| Media Type: | <black> TR _SNPB</black> | = T | ut Tape/non- ape and Reel in Lead solde | • | s | | | | | | | |
| | | | | | | | | | | | | |



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