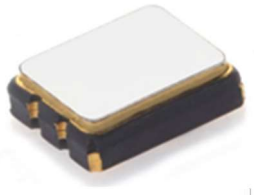
Model 357
HCMOS VCXO



Part Dimensions:
7.0 × 5.0 × 2.0mm • 178.462 mg

Features

- Ceramic Surface Mount Package
- Low Phase Jitter Performance
- Fundamental Crystal Design
- Frequency Range 1.5 – 122.88MHz *
- +3.3V or +5.0V Operation
- Output Enable Standard
- Tape and Reel Packaging, EIA-481

Standard Frequencies

* Check with factory for availability of uncommon frequencies.

Applications

- Broadcast Video Systems
- Storage Area Networking
- Test and Measurement
- Ethernet/GbE/SyncE
- Broadband Access
- Phase-Locked Loop
- Networking Equipment
- Fiber Channel

Description

CTS Model 357 is a low-cost, high-performance voltage-controlled oscillator supporting HCMOS output. M357 has excellent stability and low phase jitter performance.

Ordering Information

Model	Supply Voltage	Absolute Pull Range	Frequency Stability	Temperature Range	Frequency Code
357	L	B	3	I	XXXMXXXX

Code	Voltage
L	+3.3V, Pin 2 Enable
S	+5.0V, Pin 2 Enable
V	+3.3V, Pin 5 Enable
W	+5.0V, Pin 5 Enable

Code	Stability
3	±50ppm
5	±25ppm
6	±20ppm [1]

Code	Frequency
Product Frequency Code [2]	

Code	APR
B	±50ppm
C	±80ppm
D	±100ppm [3]

Code	Temp. Range
C	-20°C to +70°C
I	-40°C to +85°C

Notes:

1] Only available with "C" temperature range.

2] Frequency is recorded with 3 leading digits before and 4 significant digits after the "M" [including zeroes].
[Ex. 3.579545MHz = 003M5795; 14.31818MHz = 014M3181; 25MHz = 025M0000; 125MHz = 125M0000]

3] Consult factory for availability.

Not all performance combinations and frequencies may be available.
Contact your local CTS Representative or CTS Customer Service for availability.

Electrical Specifications

Operating Conditions

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNIT
Maximum Supply Voltage	V_{CC}	-	-0.5	-	7.0	V
Maximum Control Voltage	V_C	-	-0.5	-	V_{CC}	V
Supply Voltage	V_{CC}	±10%	2.97 4.5	3.3 5.0	3.63 5.5	V
Supply Current		Typical @ C_L = 15 pF, V_{CC} = +3.3V, T_A = +25°C				
	I_{CC}	1.5MHz to <20MHz	-	5	20	mA
		20MHz to <40MHz	-	8	30	
		40MHz to <60MHz	-	10	40	
		60MHz to 122.88MHz	-	12	45	
Output Load	C_L	-	-	-	15	pF
Operating Temperature	T_A	-	-20 -40	+25	+70 +85	°C
Storage Temperature	T_{STG}	-	-55	-	+125	°C

Frequency Stability

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNIT
Frequency Range	f_O	-		1.5 - 122.88		MHz
Frequency Stability [Note 1]	$\Delta f/f_O$	±20ppm stability, -20°C to +70°C only		20, 25, or 50		±ppm
Absolute Pull Range [Note 2]	APR	-	50, 80, 100	-	-	±ppm
Aging	$\Delta f/f_{25}$	First Year @ +25°C, nominal V_{CC} and V_C	-3	-	3	ppm

1.] Inclusive of initial tolerance at time of shipment, changes in supply voltage, load, temperature and 1st year aging.

2.] Minimum guaranteed frequency shift from f_O over variations in temperature, aging, power supply and load.

Output Parameters

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNIT
Output Type	-	-		HCMOS		-
Output Voltage Levels	V_{OH}	Logic '1' Level, CMOS Load	$0.9V_{CC}$	-	-	V
	V_{OL}	Logic '0' Level, CMOS Load	-	-	$0.1V_{CC}$	
Output Duty Cycle	SYM	@ 50% Level	45	-	55	%
Rise and Fall Time	T_R, T_F	@ 10%/90% Levels	-	3.5	5.0	ns
Start Up Time	T_S	Application of V_{CC}	-	-	10	ms
Enable Function		Standby				
Enable Input Voltage	V_{IH}	Pin 2 or Pin 5 Logic '1', Output Enabled	$0.7V_{CC}$	-	-	V
Disable Input Voltage	V_{IL}	Pin 2 or Pin 5 Logic '0', Output Standby	-	-	$0.3V_{CC}$	V
Standby Current	I_{STB}	Pin 2 or Pin 5 Logic '0', Output Standby	-	-	10	µA
Enable Time	T_{PLZ}	Pin 2 or Pin 5 Logic '1'	-	-	2	ms
Phase Jitter, RMS	tjrms	Bandwidth 12kHz - 20MHz	-	0.5	1	ps
Phase Noise	-	See Typical Plots	-	-	-	-

Electrical Specifications

Control Voltage

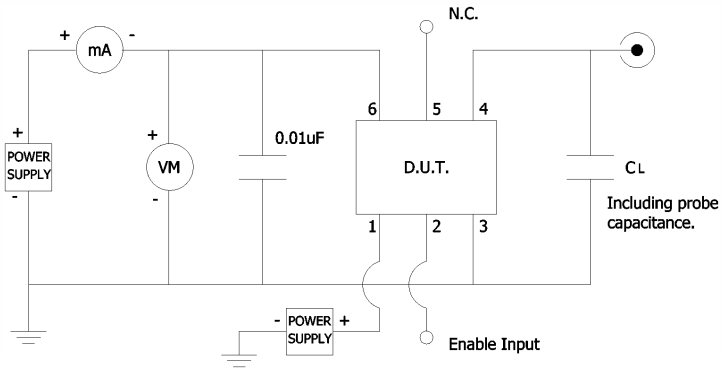
PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNIT
Control Voltage	V_C	V_{CC} = +3.3V	0.30	1.65	3.00	V
		V_{CC} = +5.0V	0.50	2.50	4.50	
Frequency Deviation	$\Delta f/f_O$	25°C at Time of Shipment, over Vc range		135		ppm
Linearity	L	Best Straight Line Fit	-	5	10	%
Gain Transfer	K_V	Pull Sensitivity; @ +1.65V, +25°C	-	65	-	ppm/V
Input Impedance	Z_{Vc}	-	100	-	-	kOhms
Modulation Roll-off	-	@ -3dB	10	-	-	kHz
Transfer Function	-	-		Positive		-

Enable Truth Table

Pin 2	Pin 4
Logic '1'	Output Enabled
Open	Output Enabled
Logic '0'	Output Disabled, High Impedance

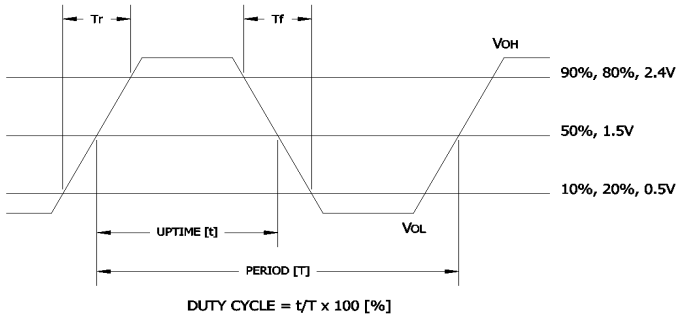
Test Circuit

HCMOS



Output Waveform

HCMOS

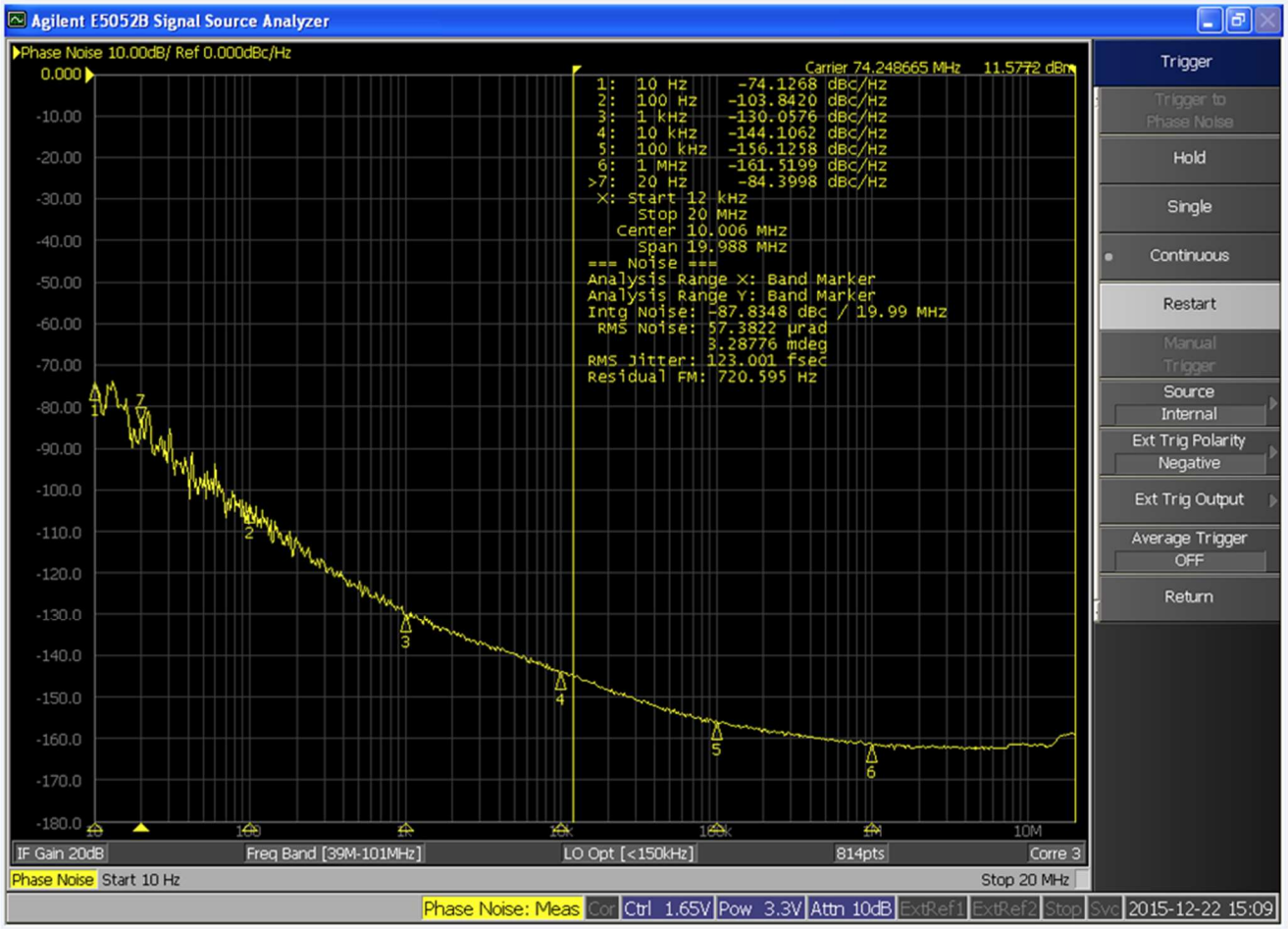


Electrical Specifications

Performance Data

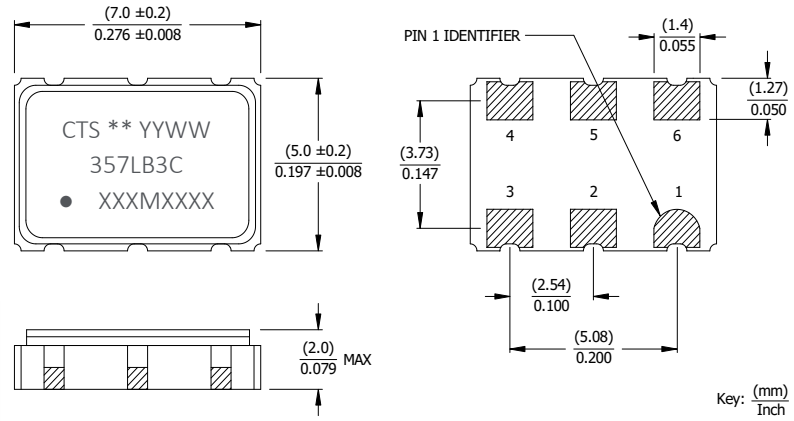
Phase Noise [typical]

74.25MHz, HCMOS, V_{CC} = +3.3V, V_C = +1.65V, T_A = +25°C



Mechanical Specifications

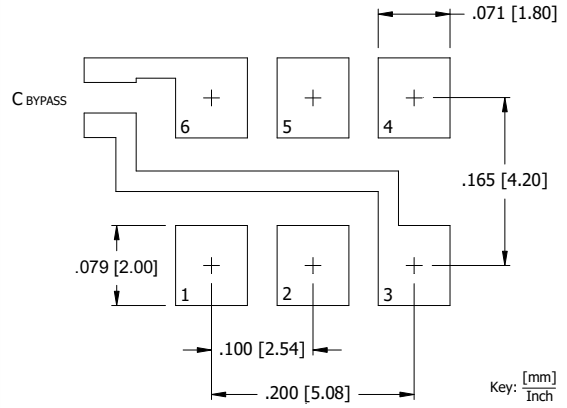
Package Drawing



Marking Information

1. ** - Manufacturing Site Code.
2. YYWW – Date code, YY – year, WW – week.
3. Truncated CTS part number.
4. XXXMXXXX - Frequency marked with 4 significant digits after the 'M'.

Recommended Pad Layout



C_{BYPASS} should be ≥ 0.01 uF.

Notes

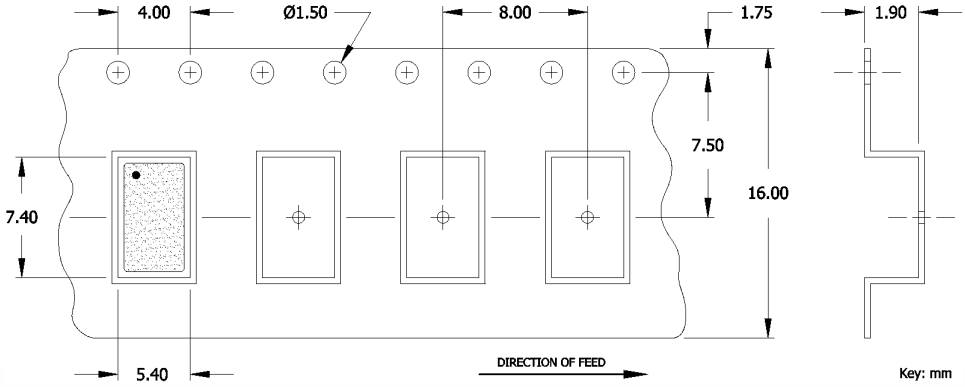
1. JEDEC termination code (e4). Barrier-plating is nickel [Ni] with gold [Au] flash plate.
2. Reflow conditions per JEDEC J-STD-020; +260°C maximum, 20 seconds.
3. MSL = 1.

Pin Assignments

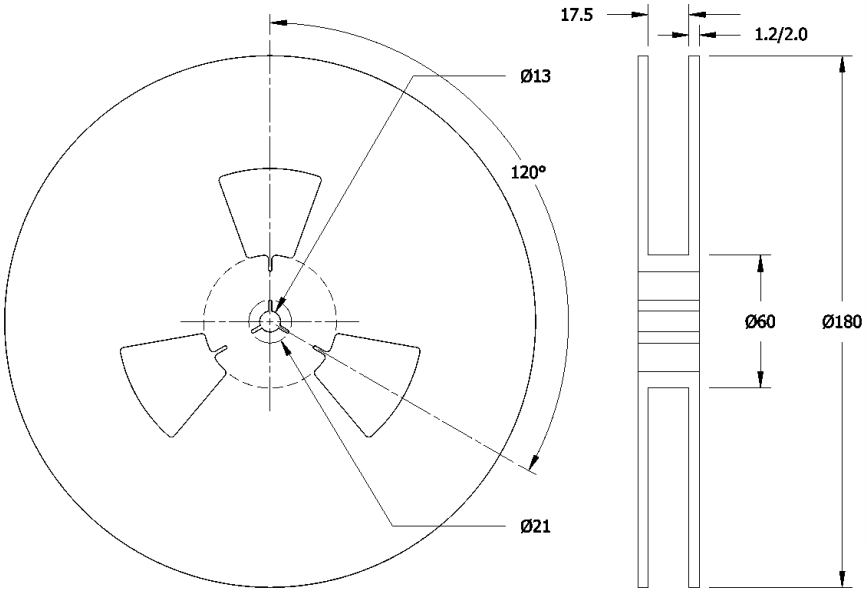
Pin	Symbol	Function
1	V_C	Voltage Control
2	EOH	Enable [standby]
3	GND	Circuit & Package Ground
4	Output	RF Output
5	N.C.	No Connect
6	V_{CC}	Supply Voltage

Packaging - Tape and Reel

Tape Drawing



Reel Drawing



Notes

1. Device quantity is 1k pieces maximum per 180mm reel.
2. Complete CTS part number, frequency value and date code information must appear on reel and carton labels.