

Technical Datasheet

HFBR-53A5VEMZ-C (3.3V)

Avago Broadcom® Compatible 1.25Gb/s 1x9 Transceiver

Duplex SC, +3.3V, VCSEL, Multi-Mode, 850nm, 500m, Commercial Temperature

FEATURES

- Industry Standard 1x9 Pin Package Footprint, Multi-Mode Transceiver
- Differential Inputs and Outputs
- Compliant with Specification for Fiber Channel.
- Compliant with Specification for IEEE802.3z / D5.
- Class 1 Laser International Safety Standard IEC-60825-1:2014 Compliant. Complies with EN60825-1:2014/A11:2021 and FDA 21 CFR 1040.10 and 1040.11.
- Commercial Operating Temperature Range: 0 to 70°C
- RoHS Compliant

APPLICATIONS

- ATM switch, multimode fiber media converters, multimode fiber backbone links
- Bridges/Routers/intelligent hub and concentrators
- Fast Ethernet

DESCRIPTION

ATGBICS® Compatible HFBR-53A5VEMZ-C transceiver is the industry standard 1x9 package with duplex fiber optical connector for serial optical data communications such as Gigabit Ethernet IEEE802.3z / D5 and FiberChannel. This module is designed for multi-mode-fiber (MMF) and operates at a nominal wavelength of 850 nm with cost effective and high performance.

The transmitter consists of a high-performance 850nm Vertical Cavity Surface Emitting Laser (VCSEL) in the optical subassembly (OSA), which is housed within a plastic barrel package. In addition, this component is also class 1 laser that complies with International Safety Standard IEC-60825-1:2014. It complies with EN60825-1:2014/A11:2021 and FDA 21 CFR 1040.10 and 1040.11.

The receiver contains a GaAs PIN photodiode that is coupled to a high sensitivity transimpedance amplifier (TIA) in an OSA. This OSA combination is mated to a post amplifier IC that provides the post amplification and SD (Signal Detection) or LOS (Loss of Signal) indication circuit which provides the logic high state output when an unusable input optical signal level detected.

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Electrical and Optical Characteristics:

Transmitter Section:

Parameter	Symbol	Min.	Typical	Max.	Unit
Supply Voltage	V _{CC}	3.15	-	5.25	V
Data Differential Input Voltage	V _{in, pp}	400	-	2000	mV
TX Input Low Voltage	V _{IL} - V _{CC}	-1.81			-
TX Input High Voltage	V _{IH} - V _{CC}	-1.16	-	-0.88	V
Pout@TX Disable Asserted	P _{OFF}	-	-	-45	dBm
Output Optical Power	P _O	-10	-	-3	dBm
Center Wavelength	λ _C	830	850	870	nm
Spectral Width (RMS)	Δλ(RMS)	-	-	0.85	nm
Optical Rise Time (20%-80%)	t _r	-	-	0.26	ns
Optical Fall Time (20%-80%)	t _f	-	-	0.26	ns
Extinction Ratio	ER	9	-	-	dB

Receiver Section:

Parameter	Symbol	Min.	Typical	Max.	Unit
Supply Voltage	V _{CC}	3.15	-	5.25	V
Data Differential Output Voltage	V _{out, pp}	500	-	1200	mV
Signal Detect Output Voltage-High	V _{OH}	2	-	V _{CC}	V
Signal Detect Output Voltage-Low	V _{OL}	0	-	0.8	V
Optical Rise Time (20%-80%)	t _r	-	-	0.35	ns
Optical Fall Time (20%-80%)	t _f	-	-	0.35	ns
Output Optical Power	P _O	-10	-	-3	dBm
Center Wavelength	λ _C	830	850	870	nm
Spectral Width (RMS)	Δλ(RMS)	-	-	0.85	nm
Optical Rise Time (20%-80%)	t _r	-	-	0.26	ns
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Absolute Maximum Ratings:

Parameter	Symbol	Min.	Typical	Max.	Unit
Supply Voltage	VCC	0	-	6	V
Storage Temperature	TS	-40	-	85	°C
Operating Case Temperature	TOP	0	-	70	°C
Lead Soldering Limits	TSOLD	-	-	260/10	°C /sec

General Specifications

Parameter	Symbol	Min.	Typical	Max.	Unit
Data Rate	B	0.80	1.25	1.50	Gbps
Supported Link Length on 62.5/125(OM1) µm MMF	L	-	0.5	-	km
Supply Current	ITx+IRx	-	-	300	mA
Power Dissipation	PDis	-	-	1000	mW

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Recommended Circuit Schematic

Data Input/Output:

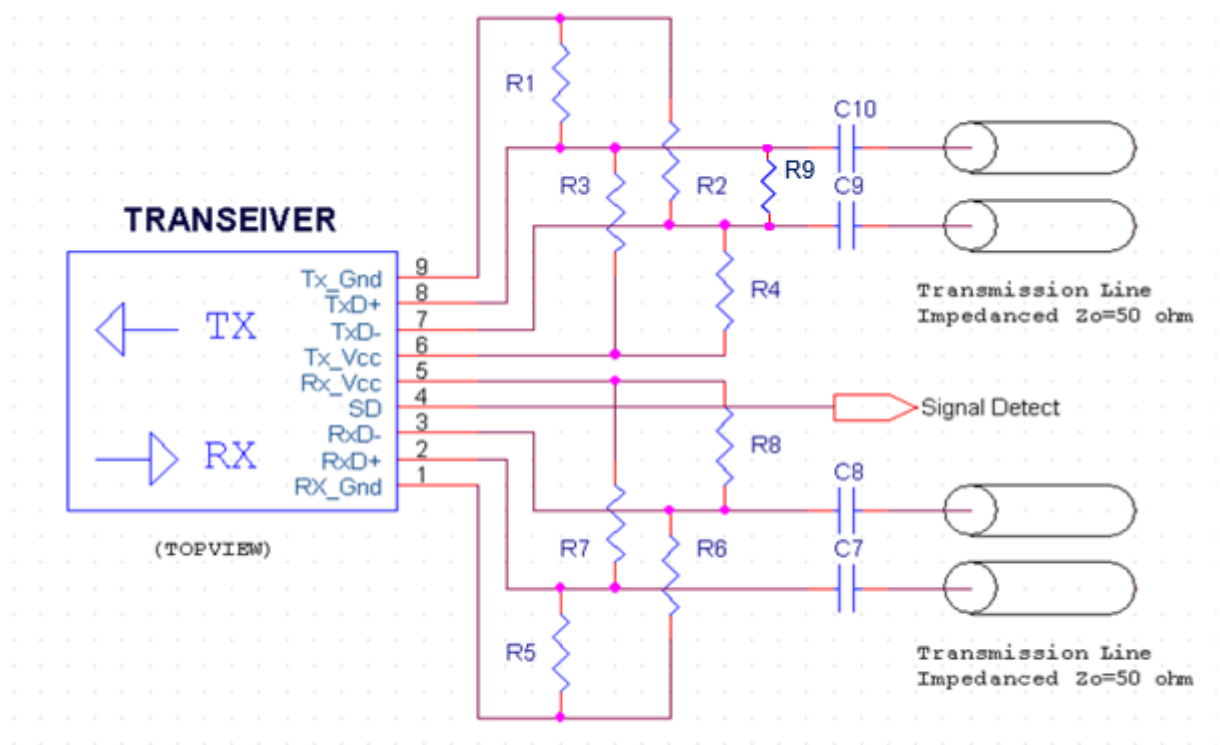


Figure 1

For 3.3V Normal Application: $R3/R4/R7/R8 = 130\ \Omega$, $R1/R2/R5/R6 = 82\ \Omega$, $R9 = NC$

For 3.3V Low-power Consumption: $R5/R6 = 180\ \Omega$, $R1/R2/R3/R4/R7/R8 = NC$, $R9 = 100\ \Omega$
 $C7/C8/C9/C10 = 0.1\ \mu F$

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Signal Detect:

The PECL output option of the signal detect line may be terminated a 50 ohm resistor to a Vcc-2 voltsource or the Thevenin equivalent in order to generate the correct voltage outputs.

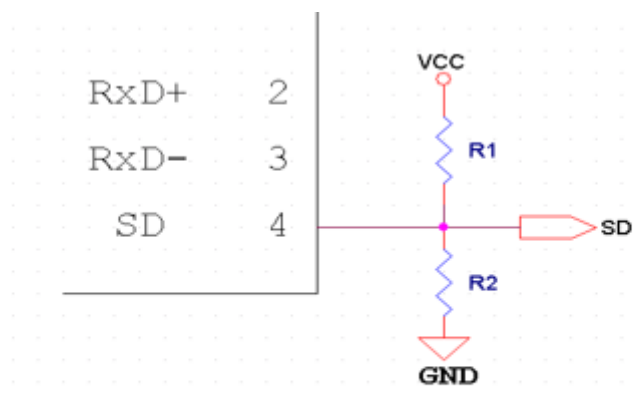


Figure 2

Power Coupling:

The L1 and L2 can use Ferrite Bead (BLM11A102S) or inductor (4.7uH).

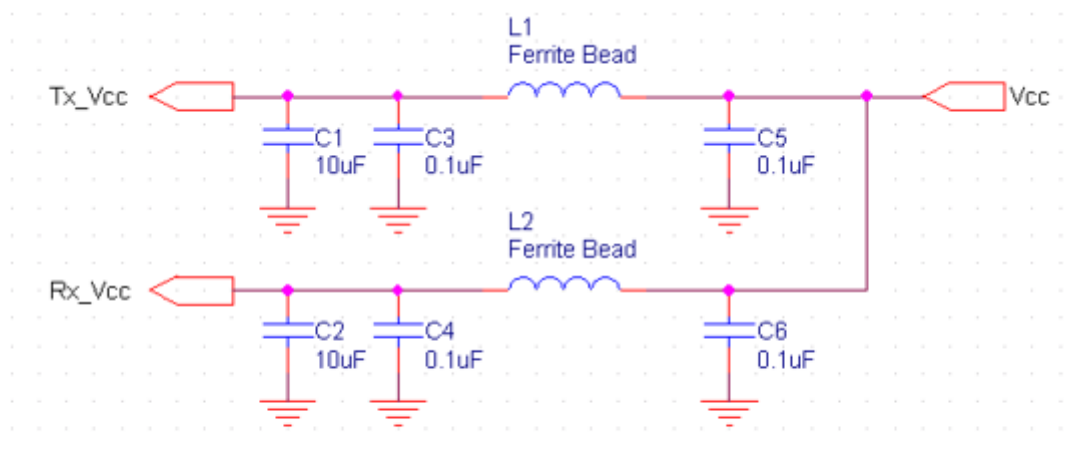
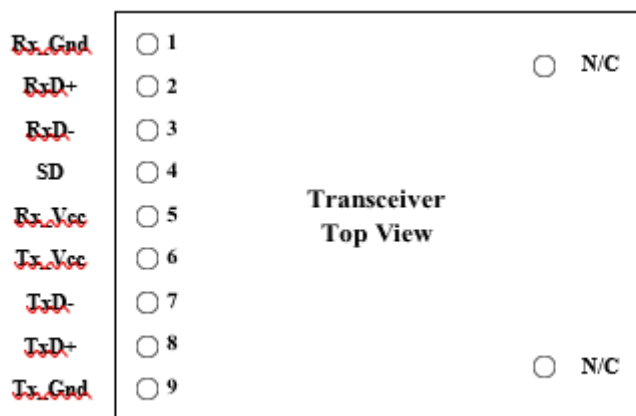


Figure 3

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Pin Assignment



Pinout Table

Pin	Symbol	Name/Description
1	Rx_Gnd	Receiver Signal Ground Directly connect this pin to receiver signal ground plane.
2	RxD+	Receiver Data Out RD+ is used to PECL output. Terminal this high-speed differential PECL output with standardPECL techniques at the follow-on device.
3	RxD-	Receiver Data Out Bar RD- is used to PECL output. Terminal this high-speed differential PECL output with standardPECL techniques at the follow-on device.
4	SD	Signal Detect Normal optical input levels to the receiver result in a logic “1” output, Voh, asserted. Low input optical levels to the receiver result in a fault condition indicated by alogic “0” output Vol, deasserted. There are several types for output interface, PECL, CMOS and TTL.
5	Rx_Vcc	Receiver Power Supply Provide (+5/+3.3V) via the recommended receiver power supply filter.
6	Tx_Vcc	Transmitter Power Supply Provide (+5/+3.3V) via the recommended transmitter power supply filter.
7	TxD-	Transmitter Data In Bar TxD- is used to PECL input. Terminate this high-speed differential PECL input with standardPECL techniques at transmitter input pin.
8	TxD+	Transmitter Data In TxD+ is used to PECL input. Terminate this high-speed differential PECL input with standardPECL techniques at transmitter input pin.
9	Tx_Gnd	Transmitter Signal Ground Directly connect this pin to transmitter signal ground plane.

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Pin Outline Drawing (units: mm)

SC Type

