TFT DISPLAY SPECIFICATION

WINSTAR Display Co.,Ltd.

華凌光電股份有限公司

Winstar Display Co., LTD
華凌光電股份有限公司
WEB: https://www.winstar.com.tw E-mail: sales@winstar.com.tw

SPECIFICATION

CUSTOMER : _____

MODULE NO.: WF35RSIACDNNB

APPROVED BY: **(FOR CUSTOMER USE ONLY)**	**PCB VERSION:** **DATA:**

SALES BY	APPROVED BY	CHECKED BY	PREPARED BY
			葉虹蘭
ISSUED DATE: 2021/09/03			

TFT Display Inspection Specification: https://www.winstar.com.tw/technology/download.html
Precaution in use of TFT module: https://www.winstar.com.tw/technology/download/declaration.html

MODLE NO：

RECORDS OF REVISION

DOC. FIRST ISSUE

VERSION	DATE	REVISED PAGE NO.	**SUMMARY**
0	2019/10/25		First issue
A	2020/06/08		Modify AC Characteristics
B	2021/09/03		Add Initial Code Modify Interface

Contents

1.Module Classification Information

W	F	35	R	S	I	A	C	D	N	N	B	#
①	②	③	④	⑤	⑥	⑦	⑧	⑨	⑩	⑪	⑫	⑬

①	Brand：WINSTAR DISPLAY CORPORATION		
②	Display Type：F→TFT Type, J→Custom TFT		
③	Display Size：3.5” TFT		
④	Model serials no.		
⑤	Backlight Type：	F→CCFL, White S→LED, High Light White	T→LED, White Z→Nichia LED, White
⑥	LCD Polarize Type/ Temperature range/ Gray Scale Inversion Direction	A→Transmissive, N.T, IPS TFT C→Transmissive, N. T, 6:00 ; F→Transmissive, N.T,12:00 ; I→Transmissive, W. T, 6:00 K→Transflective, W.T,12:00 L→Transmissive, W.T,12:00 N→Transmissive, Super W.T, 6:00	Q→Transmissive, Super W.T, 12:00 R→Transmissive, Super W.T, O-TFT V→Transmissive, Super W.T, VA TFT W→Transmissive, Super W.T, IPS TFT X→Transmissive, W.T, VA TFT Y→Transmissive, W.T, IPS TFT Z→Transmissive, W.T, O-TFT
⑦	A：TFT LCD B：TFT+SCREW HOLES+CONTROL BOARD C：TFT+ SCREW HOLES +A/D BOARD D：TFT+ SCREW HOLES +A/D BOARD+CONTROL BOARD E：TFT+ SCREW HOLES +POWER BOARD		F：TFT+CONTROL BOARD G：TFT+ SCREW HOLES H：TFT+D/V BOARD I：TFT+ SCREW HOLES +D/V BOARD J：TFT+POWER BD

⑧ Resolution:

A	128160	B	320234	C	320240	D	480234	E	480272	F	640480
G	800480	H	1024600	I	320480	J	240320	K	800600	L	240400
M	1024768	N	128128	P	1280800	Q	480800	R	640320	S	480128
T	800320	U	8001280	V	176220	W	1280398	X	1024250	Y	1920720
Z	800200	2	1024324	3	7201280	4	19201200	5	1366768	6	1280320

⑨ D: Digital L：LVDS M:MIPI

⑩ Interface:

N	Without control board	A	8Bit	B	16Bit	H	HDMI
I	I2C Interface	R	RS232	S	SPI Interface	U	USB

⑪ TS:

N	Without TS	T	Resistive touch panel	C	Capacitive touch panel (G-F-F)
G	Capacitive touch panel (G-G)	C1	Capacitive touch panel (G-F-F)+OCA		
C2	Capacitive touch panel (G-F-F)+OCR	G1	Capacitive touch panel (G-G)+OCA		
G2	Capacitive touch panel (G-G)+OCR	B	CTP+GG+USB		

⑫	Version: X:Raspberry pi	
⑬	Special Code	#:Fit in with ROHS directive regulations

2.Summary

TFT 3.5”is a TN transmissive type color active matrix TFT liquid crystal display that use amorphous silicon TFT as switching devices. This module is a composed of a TFT_LCD module, It is usually designed for industrial application and this module follows RoHs.

3.General Specifications

Item	Dimension	Unit
Size	3.5	inch
Dot Matrix	320 x RGBx240(TFT)	dots
Module dimension	76.84(W) x 63.84(H) x 3.27(D)	mm
Active area	70.08 x 52.56	mm
Dot pitch	0.073 x 0.219	mm
LCD type	TFT, Normally White, Transmissive	
View Direction	12 o'clock	
Gray Scale Inversion Direction	6 o'clock	
TFT Interface	8-bit/16-bit CPU or SPI+RGB or SPI (build in controller)	
Aspect Ratio	4:3	
Backlight Type	LED,Normally White	
IC	SSD2119 or Equivalent	
With /Without TP	Without TP	
Surface	Anti-Glare	

*Color tone slight changed by temperature and driving voltage.

4.Absolute Maximum Ratings

Item	Symbol	Min	Typ	Max	Unit
Operating Temperature	TOP	-20	—	+70	℃
Storage Temperature	TST	-30	—	+80	℃

Note: Device is subject to be damaged permanently if stresses beyond those absolute maximum ratings listed above

1. Temp. 60℃, 90% RH MAX. Temp.＞60℃, Absolute humidity shall be less than 90% RH at 60℃

5.Electrical Characteristics

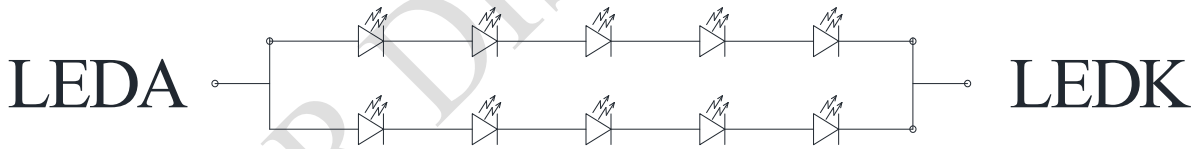
5.1. Operating conditions:

Item	Symbol	MIN	TYP	MAX	Unit	Remark
Power supply voltage	VCI	2.5	3.3	3.6	V	
Power supply pin of IO pins	VDDIO	1.4	3.3	3.6	V	
Current consumption	IVCI+IVDDIO	-	6	-	mA	
Dot clock	DCK	-	5.5	8.2	MHz	

5.2. LED driving conditions

Parameter	Symbol	Min.	Typ.	Max.	Unit	Remark
LED current		-	40		mA	
Power Consumption		540	620	660	mW	
LED voltage	LED+	13.5	15.0	16.5	V	Note 1
LED Life Time		-	50,000	-	Hr	Note 2,3,4

Note 1 : There are 1 Groups LED



CIRCUIT DIAGRAM

Note 2 : Ta = 25 ℃
Note 3 : Brightness to be decreased to 50% of the initial value
Note 4 : The single LED lamp case

6.AC Characteristics

6.1. Parallel 6800-series Interface Timing Characteristics

(TA = -40 to 85℃, VDDIO = 1.4V to 2.4)

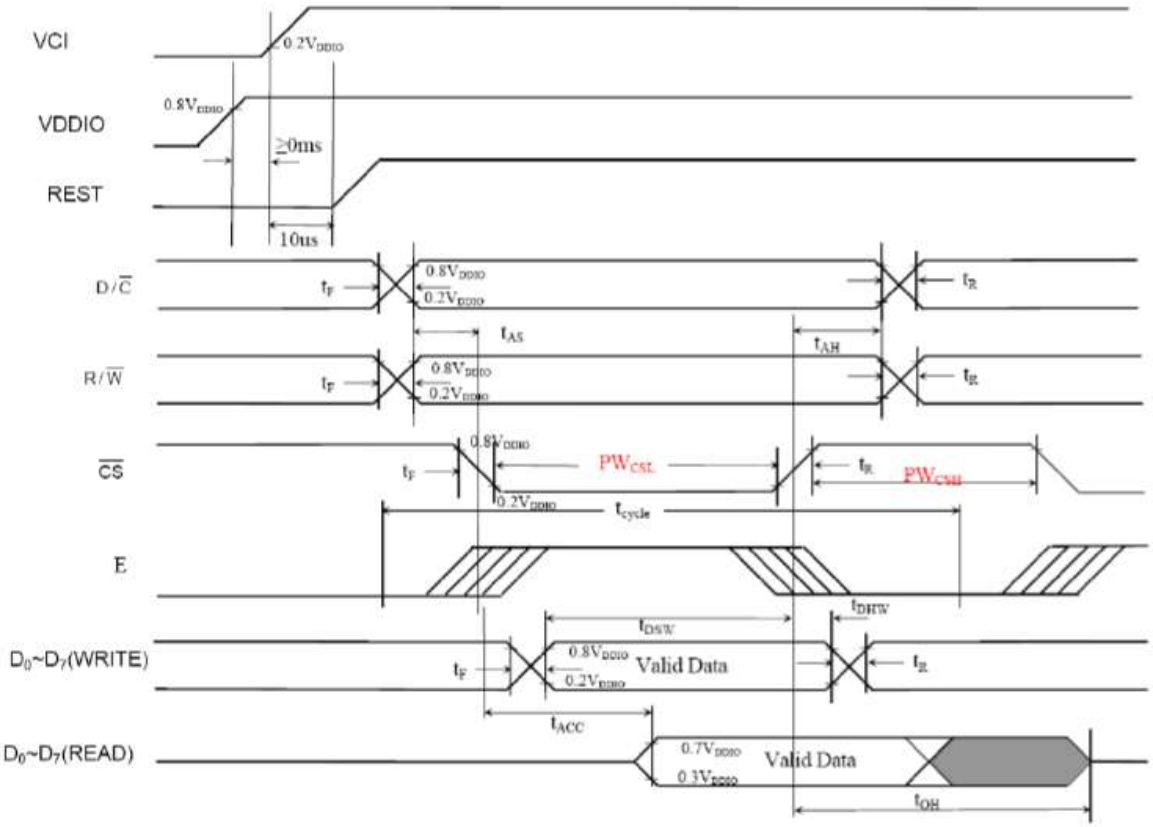
Symbol	Parameter	Min	Typ	Max	Unit
tcycle	Clock cycle time (write cycle)	75	-	-	ns
tcycle	Clock cycle time (read cycle) (Based on VOL/VOH = 0.3*VDDIO/0.7*VDDIO)	1000	-	-	ns
t_{AS}	Address setup time (R/W)	0	-	-	ns
t_{AH}	Address hold time (R/W)	0	-	-	ns
t_{DSW}	Data setup time(D0~D7,WRITE)	5	-	-	ns
t_{DHW}	Data hold time(D0~D7,WRITE)	5	-	-	ns
t_{ACC}	Data access time(D0~D7,READ)	250	-	-	ns
t_{OH}	Output hold time(D0~D7,READ)	100	-	-	ns
PW_{CSL}	Pulse width/CS low(write cycle)	40	-	-	ns
PW_{CSH}	Pulse width/CS high(write cycle)	25	-	-	ns
PW_{CSL}	Pulse width/CS low(read cycle)	500	-	-	ns
PW_{CSH}	Pulse width/CS high(read cycle)	500	-	-	ns
t_R	Rise time(/CS)	-	-	15	ns
t_F	Fall time(/CS)	-	-	15	ns

(TA = -40 to 85℃, VDDIO = 2.4V to 3.6V)

Symbol	Parameter	Min	Typ	Max	Unit
tcycle	Clock cycle time (write cycle)	75	-	-	ns
tcycle	Clock cycle time (read cycle) (Based on VOL/VOH = 0.3*VDDIO/0.7*VDDIO)	450	-	-	ns
t_{AS}	Address setup time (R/W)	0	-	-	ns
t_{AH}	Address hold time (R/W)	0	-	-	ns
t_{DSW}	Data setup time(D0~D7,WRITE)	5	-	-	ns
t_{DHW}	Data hold time(D0~D7,WRITE)	5	-	-	ns
t_{ACC}	Data access time(D0~D7,READ)	200	-	-	ns
t_{OH}	Output hold time(D0~D7,READ)	100	-	-	ns
PW_{CSL}	Pulse width/CS low(write cycle)	40	-	-	ns
PW_{CSH}	Pulse width/CS high(write cycle)	25	-	-	ns
PW_{CSL}	Pulse width/CS low(read cycle)	225	-	-	ns
PW_{CSH}	Pulse width/CS high(read cycle)	225	-	-	ns
t_R	Rise time(/CS)	-	-	15	ns
t_F	Fall time(/CS)	-	-	15	ns

Note: CS can be pulled low during the write cycle, only /RW is needed to be toggled

Parallel 6800-series interface timing characteristics

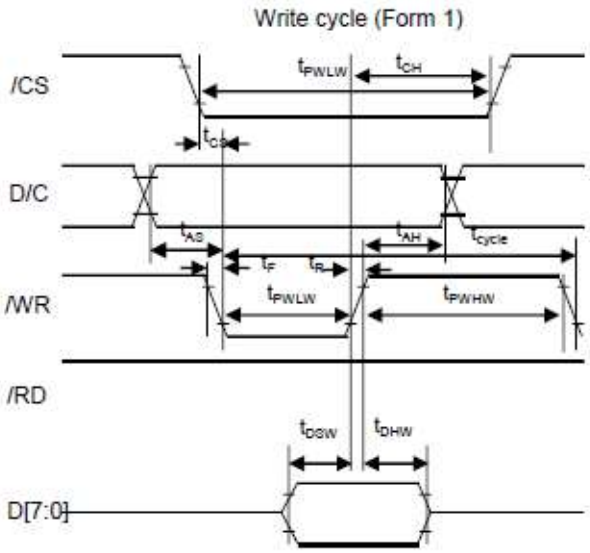


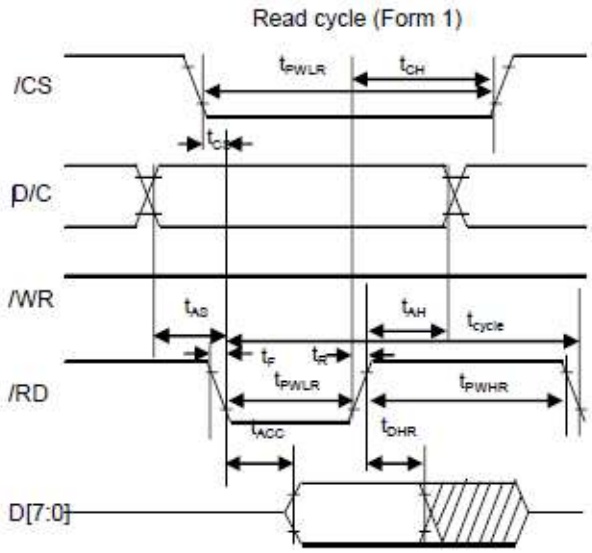
6.2. Parallel 8080 Timing Characteristics

Symbol	Parameter	Min	Typ	Max	Unit
tcycle	Clock cycle time (write cycle)	100	-	-	ns
t_{AS}	Address setup time	10	-	-	ns
t_{AH}	Address hold time	0	-	-	ns
t_{CS}	Chip select time	0			ns
t_{CH}	Chip select hold time	0			ns
t_{DSW}	Write Data setup time	10	-	-	ns
t_{DHW}	Write Data hold time	10	-	-	ns
t_{DHR}	Read Data hold time	100			ns
t_{ACC}	Access time(RAM) Access time(command)	250 250	-	-	ns ns
t_{PWLR} t_{PWLR} t_{PWLW}	Chip select low pulse width(read RAM) Chip select low pulse width(read command) Chip select low pulse width(write)	500 500 50	-	-	ns ns ns
t_{PWHR} t_{PWHW}	Chip select high pulse width(read) Chip select high pulse width(write)	500 50	-	-	ns ns
t_R	Rise time	-	-	15	ns
t_F	Fall time	-	-	15	ns

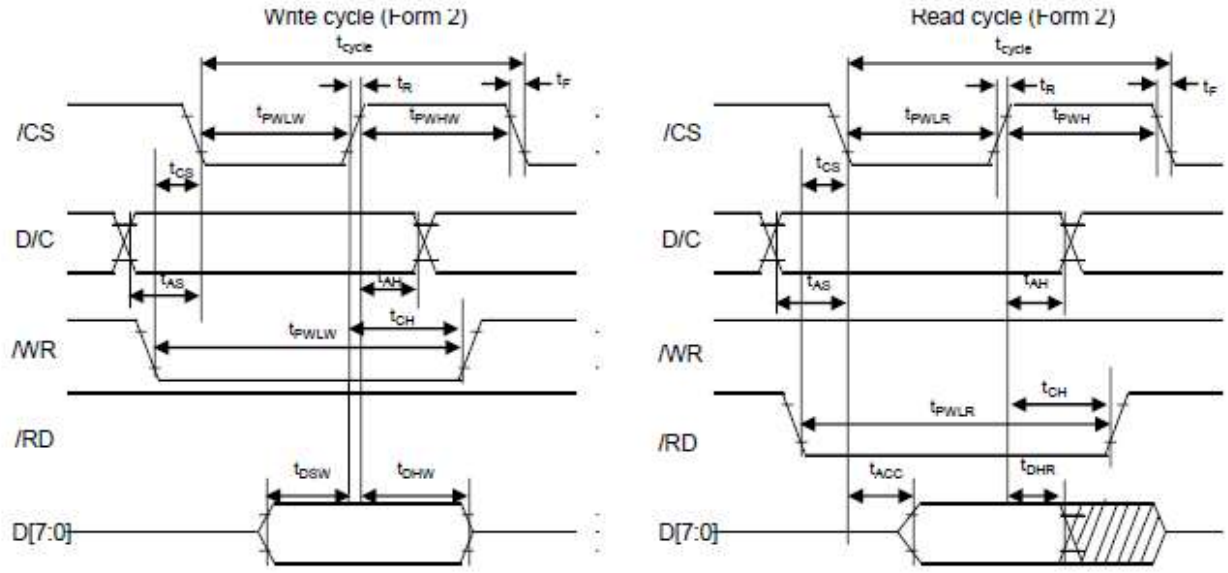
Note: all timings are based on 20% to 80% of V_{DDIO}-V_{SS}

8080-series parallel interface characteristics (Form 1: /CS low pulse width > W/ R low pulse width)





8080-series parallel interface characteristics (Form 2: /CS low pulse width < W/ R low pulse width)

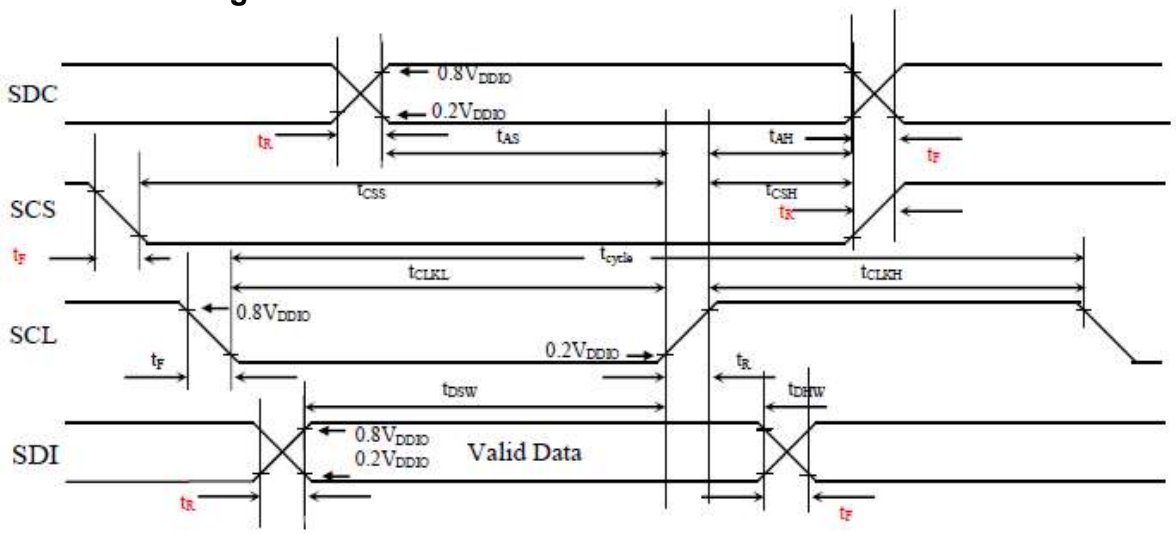


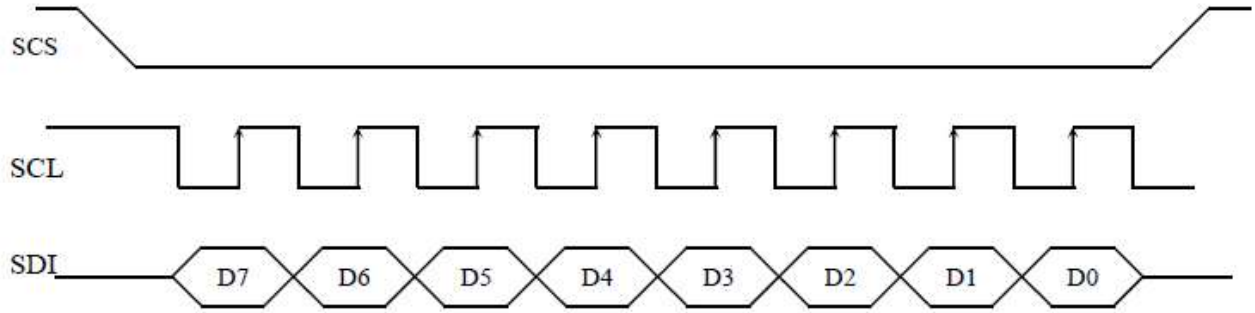
6.3. Serial Timing Characteristics

(Ta=-40 to 85℃, VDDIO = 1.4V to 3.6V)

Symbol	Parameter	Min	Typ	Max	Unit
tcycle	Clock cycle time	77	-	-	ns
f_{CLK}	Serial clock cycle time SPI clock tolerance =+/- 2 ppm	-	-	15	MHz
t_{AS}	Register select setup time	4	-	-	ns
t_{AH}	Register select hold time	5	-	-	ns
t_{CSS}	Chip select setup time	2			ns
t_{CSH}	Chip select hold time	10			ns
t_{DSW}	Write Data setup time	5	-	-	ns
t_{OHW}	Write Data hold time	10	-	-	ns
t_{CLKL}	Clock low time	38			ns
t_{CLKH}	Clock high time	38	-	-	ns
t_R	Rise time	-	-	15	ns
t_F	Fall time	-	-	15	ns

4 wire serial timing characteristics





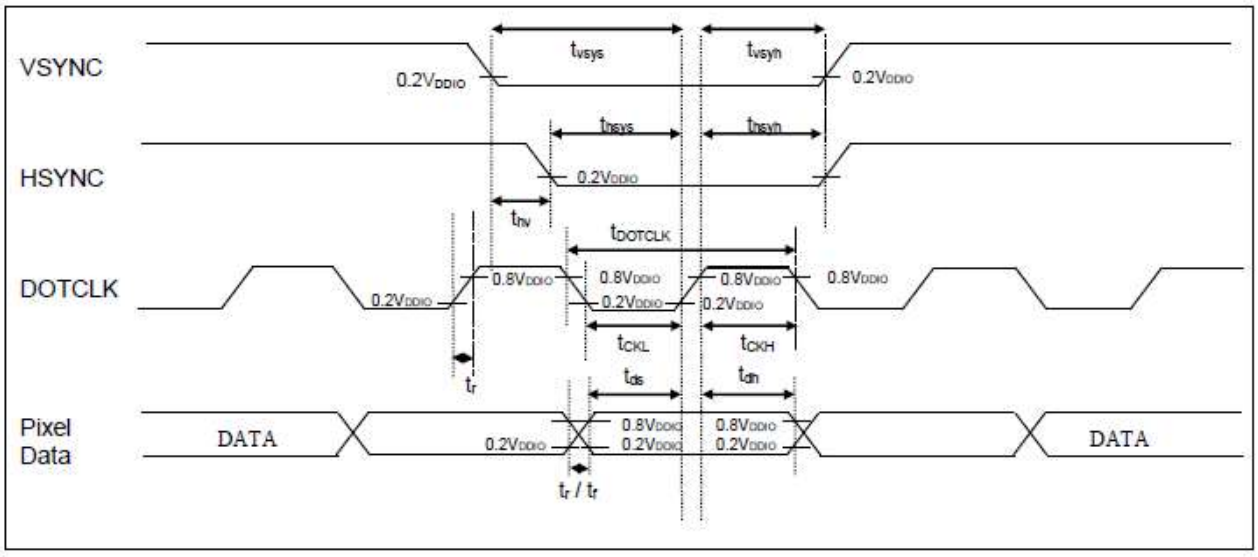
6.4. RGB Timing Characteristics

(Ta=-40 to 85℃, VDDIO = 1.4V to 3.6V)

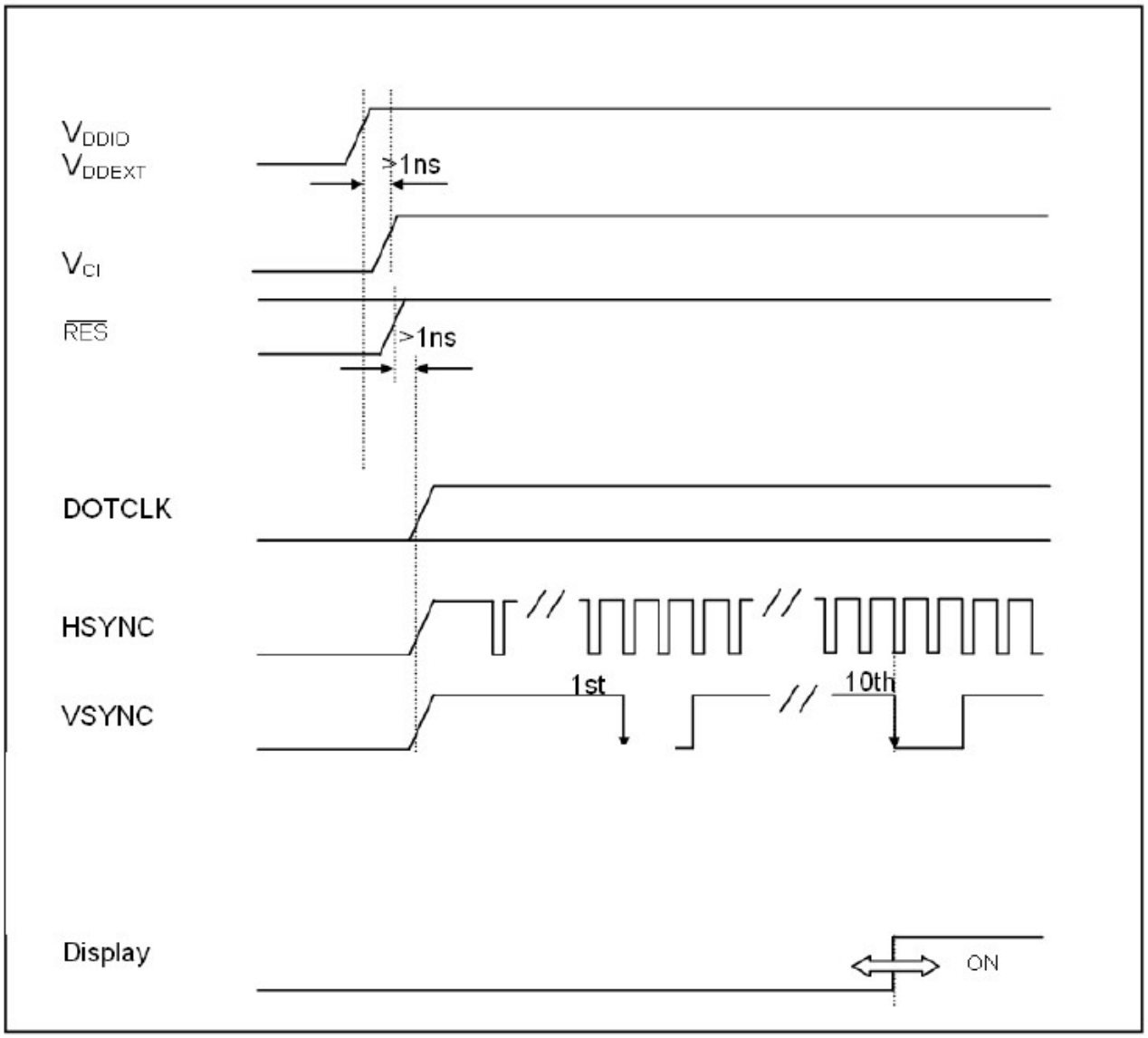
Symbol	Parameter	Min	Typ	Max	Unit
fDOTCLK	DOTCLK frequency (70Hz frame rate)	1	5.5	8.2	MHZ
tDOTCLK	DOTCLK period	122	182	1000	ns
tVSYS	Vertical sync setup time	20	-	-	ns
tVSYH	Vertical sync hold time	20			ns
tHSYS	Horizontal sync setup time	20			ns
tHSYH	Horizontal sync hold time	20	-	-	ns
tHV	Phase difference of sync signal falling edge	0	-	HFP-1	t_{DOTCLK}
tCLK	DOTCLK low period	61	-	-	ns
tCKH	DOTCLK high period	61			ns
tDS	Data setup time	25	-	-	ns
tDH	Data hold time	25	-	-	ns

Note: External clock source must be provided to DOTCLK pin of SSD2119M1. The driver will not operate in absence of the clocking signal.
*HFP: Horizontal Front Porch setting in customers' setup

RGB timing characteristics

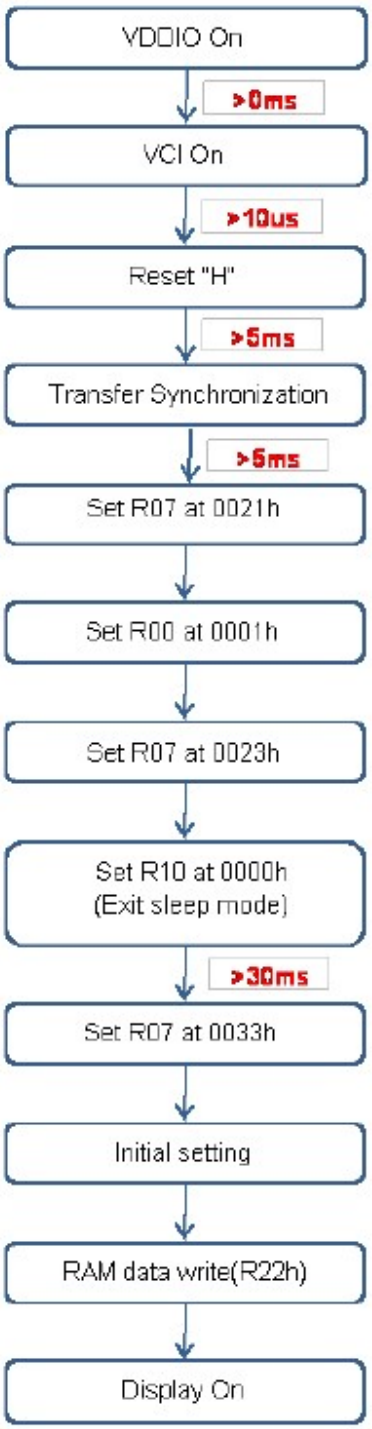


6.5. Power Up Sequence for RGB mode



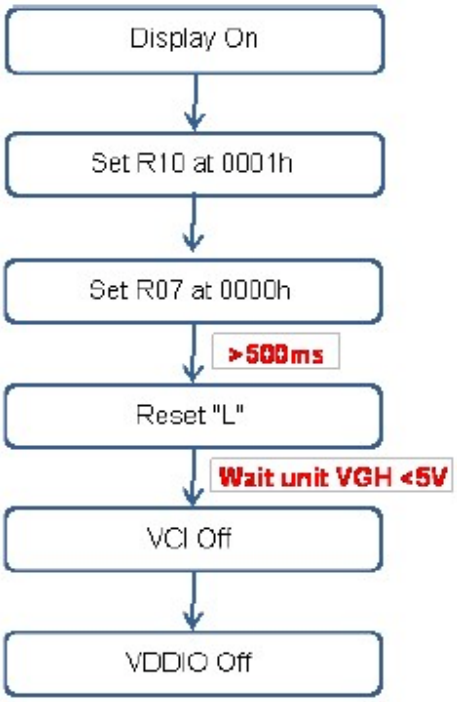
6.6. Display on sequence

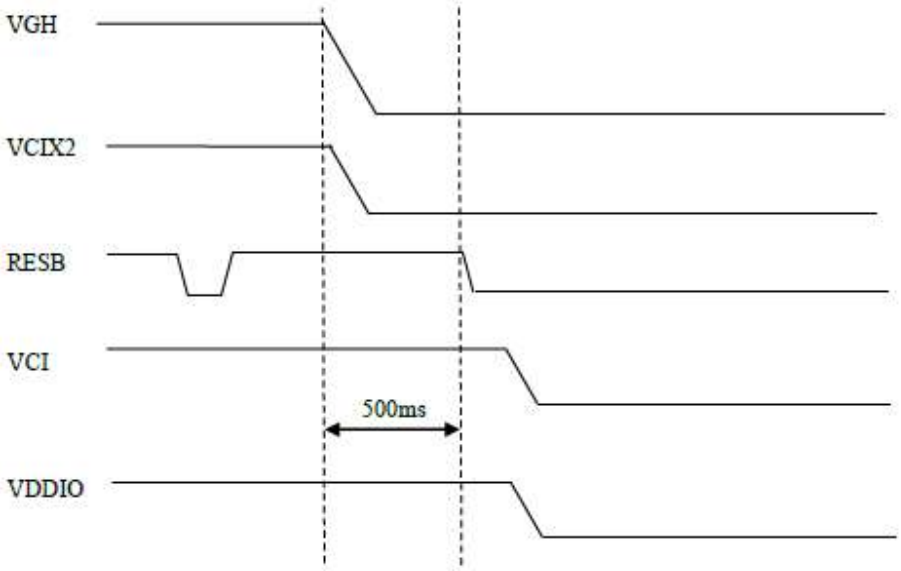
Note: To prevent potential damage to the device, all capacitors must be discharged to below 0.5V before the driver is removed from, or before the driver is attached to those components.



6.7. **Display off sequence**

Note: To prevent potential damage to the device, all capacitors must be discharged to below 0.5V before the driver is removed from, or before the driver is attached to those components.





Note:

1. VDDIO should be the last to fall, or VCI/VDDIO could be power off at the same time
2. If OTP is active in the application, the OTP programming voltage should be turned off and cap discharged before VCI/VDDIO are turned off.

7.Optical Characteristics

Item		Symbol	Condition.	Min	Typ.	Max.	Unit	Remark
Response time		Tr+ Tf	θ=0°、Φ=0°	-	25	-	ms	Note 3
Contrast ratio		CR	At optimized viewing angle	300	-	-	-	Note 4
Color Chromaticity	White	Wx	θ=0°、Φ=0	0.26	0.31	0.36	-	Note 2,6,7
		Wy		0.28	0.33	0.38	-	
Viewing angle (Gray Scale Inversion Direction)	Hor.	ΘR	CR 10	-	60	-	Deg.	Note 1
		ΘL		-	60	-		
	Ver.	ΦT		-	50	-		
		ΦB		-	60	-		
Brightness		-	-	800	900	-	cd/m^2	Center of display
Uniformity		(U)	-	75	-	-	%	Note5

Ta=25±2℃, IL=20mA

Note 1: Definition of viewing angle range

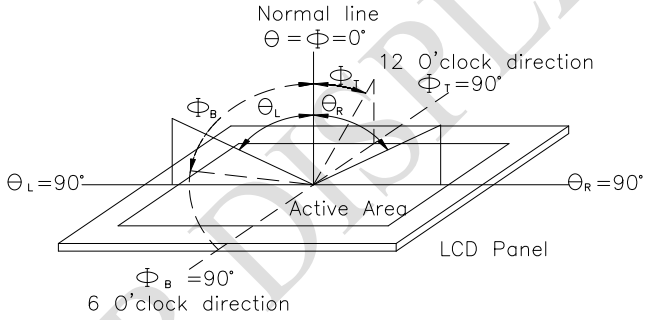


Fig 7.1. Definition of viewing angle

Note 2: Test equipment setup:

After stabilizing and leaving the panel alone at a driven temperature for 10 minutes, the measurement should be executed. Measurement should be executed in a stable, windless, and dark room. Optical specifications are measured by Topcon BM-7orBM-5 luminance meter 1.0° field of view at a distance of 50cm and normal direction.

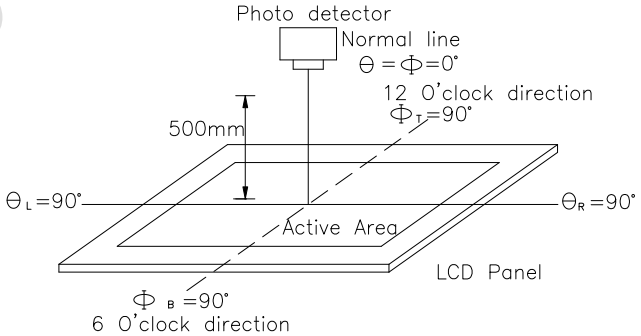
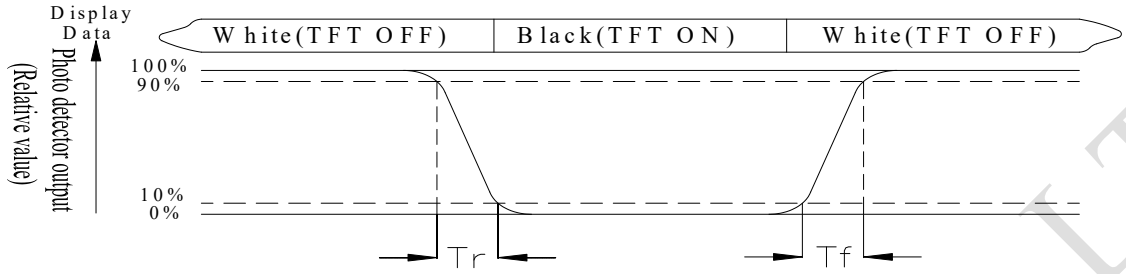


Fig 7.2. Optical measurement system setup

Note 3: Definition of Response time:

The response time is defined as the LCD optical switching time interval between “White” state and “Black” state. Rise time, Tr, is the time between photo detector output intensity changed from 90%to 10%. And fall time, Tf, is the time between photo detector output intensity changed from 10%to 90%



Note 4: Definition of contrast ratio:
The contrast ratio is defined as the following expression.

$$\text{Contrast ratio (CR)} = \frac{\text{Luminance measured when LCD on the "White" state}}{\text{Luminance measured when LCD on the "Black" state}}$$

Note 5: Definition of Luminance Uniformity
Active area is divided into 9 measuring areas (reference the picture in below). Every measuring point is placed at the center of each measuring area.
Luminance Uniformity (U) = Lmin/Lmax x100%
L = Active area length
W = Active area width

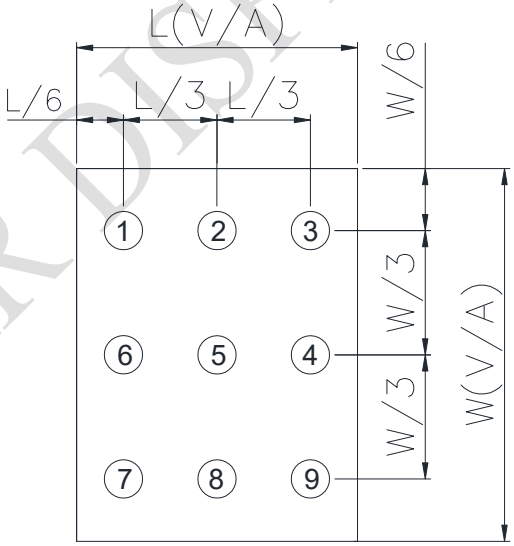


Fig 7.3. Definition of uniformity

Note 6: Definition of color chromaticity (CIE 1931)
Color coordinates measured at the center point of LCD

Note 7: Measured at the center area of the panel when all the input terminals of LCD panel are electrically opened.

8.Interface

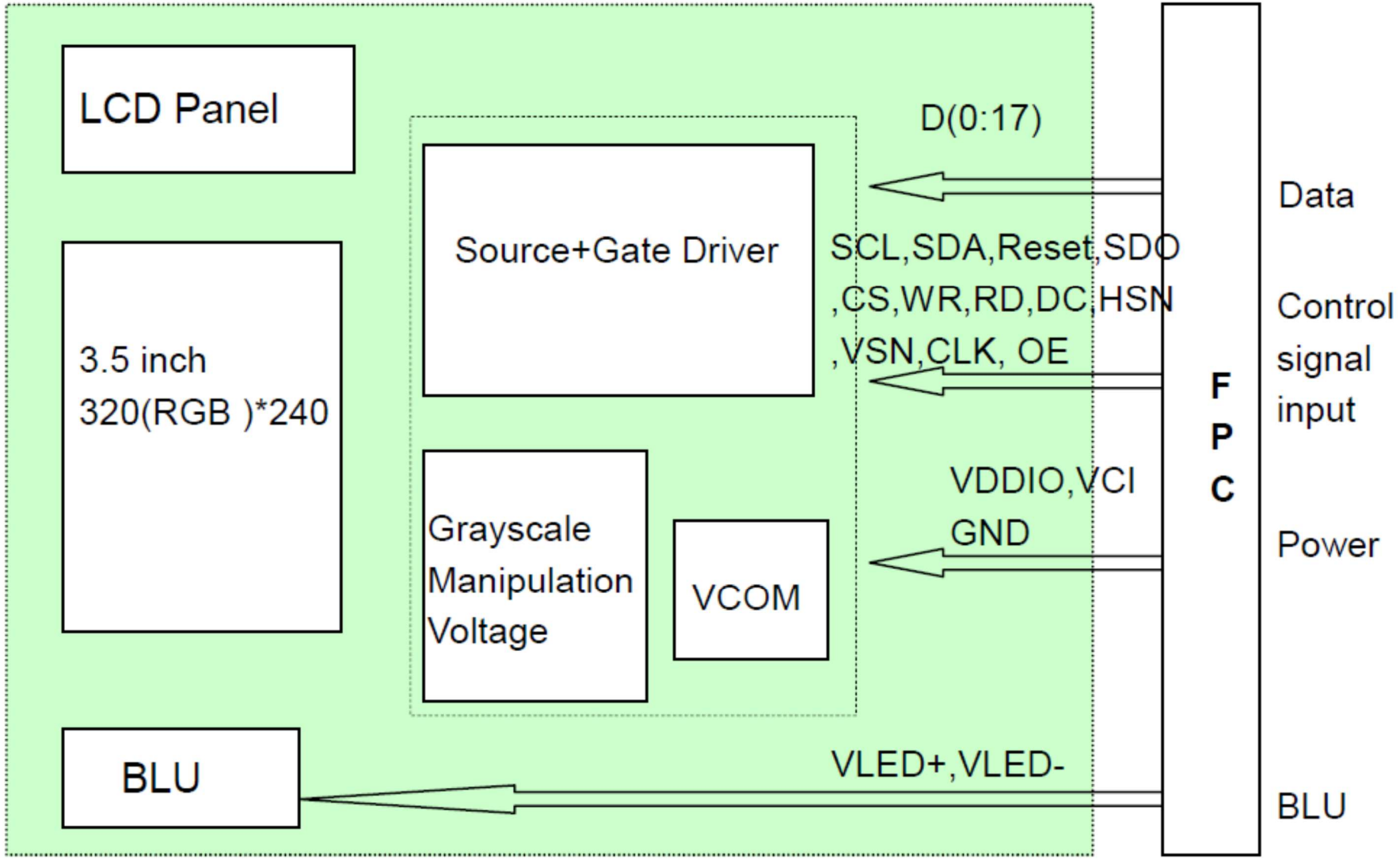
8.1. LCM PIN Definition

No.	Symbol	Description
1	VCI	Booster input voltage pin
2	VCI	Booster input voltage pin
3	VSS	Ground
4	VDDIO	Voltage input pin for logic
5	VSS	Ground
6	RESET	Reset Signal pin (“Low” is enable)
7	DC/SDC	Data or Command select PIN.
8	E/RD	6800 system: E(enable signal) 8080 system : RD(read strobe signal) Serial mode: Not use and should be connected to VDDIO or VSS
9	WR	6800 system : RW (indicates read cycle when high ,write cycle when low) 8080 system : WR (write strobe signal)
10	CS	Chip select
11	SCL	Serial Clock.
12	SD0	Serial Data output
13	SDI	Serial Data Input
14	WSYNC	Ram write synchronization output. Leave it OPEN when not used.
15~32	D17~D0	Data bus
33	VSS	Ground
34	DOTCLK	Dot-clock signal and oscillator source
35	HSYNC	Line Synchronous Signal
36	VSYNC	Frame Synchronous Signal
37	DE	Display enable pin for controller
38	VSS	Ground
39	PS0	Interface select PIN
40	PS1	
41	PS2	
42	PS3	
43	VSS	Ground
44~47	NC	NC
48	VSS	Ground

49	LEDK	Backlight LED Cathode
50	LEDA	Backlight LED Anode.

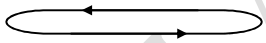
PS3	PS2	PS1	PS0	Interface Mode	Data bus input
0	0	0	0	16-bit 6800 parallel interface	D[17:10], D[8:1]
0	0	0	1	8-bit 6800 parallel interface	D[17:10]
0	0	1	0	16-bit 8080 parallel interface	D[17:10], D[8:1]
0	0	1	1	8-bit 8080 parallel interface	D[17:10]
0	1	0	0	9-bit generic D[9:16] (262k colour) + 3-wire SPI If 65K color, D12 shorts to D17 internally	
0	1	0	1	16-bit generic (262k colour) + 3-wire SPI	
0	1	1	0	18-bit generic (262k colour) + 3-wire SPI	
0	1	1	1	6-bit generic D[8:3] (262k colour) + 3-wire SPI	
1	0	0	0	18-bits 6800 parallel interface	D[17:0]
1	0	0	1	9-bits 6800 parallel interface	D[17:9]
1	0	1	0	18-bit 8080 parallel interface	D[17:0]
1	0	1	1	9-bit 8080 parallel interface	D[17:9]
1	1	1	0	3-wire SPI	
1	1	1	1	4-wire SPI	

9.Block Diagram



10.Reliability

Content of Reliability Test (Wide temperature, -20℃~70℃)

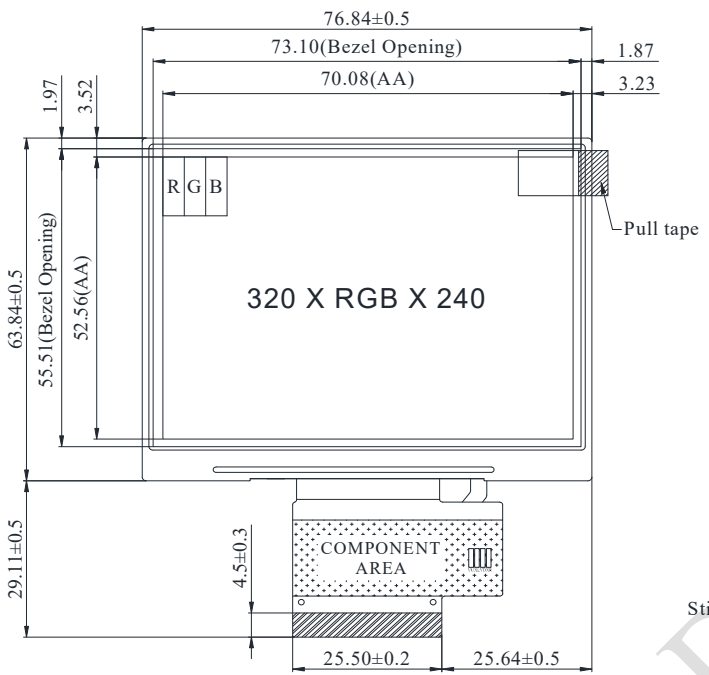
Environmental Test			
Test Item	**Content of Test**	**Test Condition**	**Note**
High Temperature storage	Endurance test applying the high storage temperature for a long time.	80℃ 200hrs	2
Low Temperature storage	Endurance test applying the low storage temperature for a long time.	-30℃ 200hrs	1,2
High Temperature Operation	Endurance test applying the electric stress (Voltage & Current) and the thermal stress to the element for a long time.	70℃ 200hrs	——
Low Temperature Operation	Endurance test applying the electric stress under low temperature for a long time.	-20℃ 200hrs	1
High Temperature/ Humidity Operation	The module should be allowed to stand at 60℃,90%RH max	60℃,90%RH 96hrs	1,2
Thermal shock resistance	The sample should be allowed stand the following 10 cycles of operation -20℃ 25℃ 70℃  30min 5min 30min 1 cycle	-20℃/70℃ 10 cycles	——
Vibration test	Endurance test applying the vibration during transportation and using.	Total fixed amplitude : 1.5mm Vibration Frequency : 10~55Hz One cycle 60 seconds to 3 directions of X,Y,Z for Each 15 minutes	3
Static electricity test	Endurance test applying the electric stress to the terminal.	VS=±600V(contact), ±800v(air), RS=330Ω CS=150pF 10 times	——

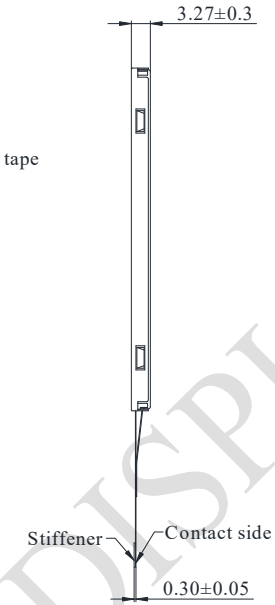
Note1: No dew condensation to be observed.

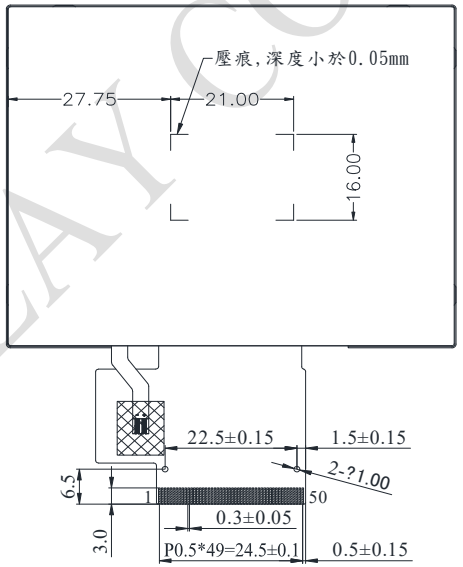
Note2: The function test shall be conducted after 4 hours storage at the normal Temperature and humidity after remove from the test chamber.

Note3: The packing have to including into the vibration testing.

11.Contour Drawing







PIN NO.	SYMBOL	PIN NO.	SYMBOL
1	VCI	26	D6
2	VCI	27	D5
3	VSS	28	D4
4	VDDIO.	29	D3
5	VSS	30	D2
6	RESET	31	D1
7	DC/SDC(RS)	32	D0
8	E/RD	33	VSS
9	WR	34	DOTCLK
10	CS	35	HSYNC
11	SCL	36	VSYNC
12	SDO	37	DE
13	SDI	38	VSS
14	WSYNC(NC)	39	PS0
15	D17	40	PS1
16	D16	41	PS2
17	D15	42	PS3
18	D14	43	VSS
19	D13	44	NC(YU)
20	D12	45	NC(XL)
21	D11	46	NC(YD)
22	D10	47	NC(XR)
23	D9	48	VSS
24	D8	49	LEDK
25	D7	50	LEDA

The non-specified tolerance of dimension is ±0.3 mm .

12.Initial Code For Reference

```
/****************************************
8-bit/16-bit CPU mode initialization
Resolution 320x240
****************************************/
    Write_Command(0x0028);
    Write_Data16(0x0006);

    Write_Command(0x0000);
    Write_Data16(0x0001);

    Write_Command(0x0010);
    Write_Data16(0x0000);

    Write_Command(0x0007);
    Write_Data16(0x0033);

    Write_Command(0x0011);
    Write_Data16(0x6230);


    Write_Command(0x0016);
    Write_Data16(0xffff);
    Write_Command(0x0017);
    Write_Data16(0xffff);

    Write_Command(0x0002);
    Write_Data16(0x0600);

    Write_Command(0x0003);
    Write_Data16(0xaaae);


    Write_Command(0x0001);

    Write_Data16(0x32EF);


    Write_Command(0x000f);
    Write_Data16(0x0000);

    Write_Command(0x000b);
    Write_Data16(0x5208);


    Write_Command(0x000c);
    Write_Data16(0x0005);
```

```
Write_Command(0x002a);
Write_Data16(0x09d5);

Write_Command(0x000d);
Write_Data16(0x000d);


Write_Command(0x000e);
Write_Data16(0x2400);


Write_Command(0x001e);
Write_Data16(0x00ac);


Write_Command(0x0044);
Write_Data16(0xef00);

Write_Command(0x0045);
Write_Data16(0x0000);

Write_Command(0x0046);
Write_Data16(0x013f);

Write_Command(0x004e);
Write_Data16(0x0000);

Write_Command(0x004f);
Write_Data16(0x0000);


Write_Command(0x0030);
Write_Data16(0x0100);

Write_Command(0x0031);
Write_Data16(0x0000);

Write_Command(0x0032);
Write_Data16(0x0106);

Write_Command(0x0033);
Write_Data16(0x0000);

Write_Command(0x0034);
Write_Data16(0x0000);

Write_Command(0x0035);
Write_Data16(0x0403);
```

```
Write_Command(0x0036);
Write_Data16(0x0000);

Write_Command(0x0037);
Write_Data16(0x0000);

Write_Command(0x003a);
Write_Data16(0x1100);

Write_Command(0x003b);
Write_Data16(0x0009);

Write_Command(0x0025);
Write_Data16(0xe000);

Write_Command(0x0026);
Write_Data16(0x3800);
```

```
/***************************************
SSD2119 3-Line SPI mode initialization
Resolution 320x240
***************************************/

#define SPI_COMMAND 0
#define SPI_DATA    1

//Register Address
#define VCOM_OTP          0x28
#define OSC_START         0x00
#define SLEEP_MODE        0x10
#define DISP_CTRL         0x07
#define ENTRY_MODE        0x11
#define H_PORCH           0x16
#define V_PORCH           0x17
#define LCD_DRIVER        0x02
#define PWR_CTRL_1        0x03
#define DRIVER_OUTPUT     0x01

#define GATE_SCAN_POS     0x0F
#define CYCLE_CTRL        0x0B
#define PWR_CTRL_2        0x0C
#define PWR_CTRL_3        0x0D
#define PWR_CTRL_4        0x0E
#define PWR_CTRL_5        0x1E
#define V_ADDR            0x44
#define H_STR_ADDR        0x45
#define H_END_ADDR        0x46
#define RAM_XADDR         0x4E
#define RAM_YADDR         0x4F

#define GRAM_WRITE        0x22

void SPI_WRT_3PIN(unsigned char DC, unsigned char dat)
{
    unsigned char i;

    SSD2119_CS = 0;
    SSD2119_SCK = 0;
    SSD2119_SDA = DC;
    SSD2119_SCK = 1;

    for(i=0; i < 8; i++)
    {
        SSD2119_SCK = 0;

        if(dat&0x80)
            SSD2119_SDA = 1;
        else
```

```
            SSD2119_SDA = 0;

        dat <<= 1;
        SSD2119_SCK = 1;
    }

    SSD2119_SCK = 0;
    SSD2119_CS = 1;
}

void LCD_RST(void)
{
    IC_RST =1;
    delay(6000);

    IC_RST = 0;
    delay(30000);

    IC_RST = 1;

    delay(60000);
    delay(60000);
}

void SSD2119_PWR_ON_SEQUENCE()
{
    SPI_WRT_3PIN(SPI_COMMAND, DISP_CTRL);
    SPI_WRT_3PIN(SPI_DATA, 0x00);
    SPI_WRT_3PIN(SPI_DATA, 0x08);

    SPI_WRT_3PIN(SPI_COMMAND, OSC_START);
    SPI_WRT_3PIN(SPI_DATA, 0x00);
    SPI_WRT_3PIN(SPI_DATA, 0x01);

    SPI_WRT_3PIN(SPI_COMMAND, DISP_CTRL);
    SPI_WRT_3PIN(SPI_DATA, 0x00);
    SPI_WRT_3PIN(SPI_DATA, 0x23);

    SPI_WRT_3PIN(SPI_COMMAND, SLEEP_MODE);
    SPI_WRT_3PIN(SPI_DATA, 0x00);
    SPI_WRT_3PIN(SPI_DATA, 0x00);

    delay(60000);
    delay(60000);
    delay(60000);
    delay(60000);
    delay(60000);
    delay(60000);
    delay(60000);
    delay(60000);
```

```
    SPI_WRT_3PIN(SPI_COMMAND, DISP_CTRL);
    SPI_WRT_3PIN(SPI_DATA, 0x00);
    SPI_WRT_3PIN(SPI_DATA, 0x33);
}

void SSD2119_35U_SPI_INIT()
{
    SPI_WRT_3PIN(SPI_COMMAND, ENTRY_MODE);//check sync, den later
    SPI_WRT_3PIN(SPI_DATA, 0x62);
    SPI_WRT_3PIN(SPI_DATA, 0x30);

    SPI_WRT_3PIN(SPI_COMMAND, H_PORCH);
    SPI_WRT_3PIN(SPI_DATA, 0x00);
    SPI_WRT_3PIN(SPI_DATA, SSD2119_HBP);

    SPI_WRT_3PIN(SPI_COMMAND, V_PORCH);
    SPI_WRT_3PIN(SPI_DATA, SSD2119_VFP);
    SPI_WRT_3PIN(SPI_DATA, SSD2119_VBP);

    SPI_WRT_3PIN(SPI_COMMAND, LCD_DRIVER);   //lcd driver
    SPI_WRT_3PIN(SPI_DATA, 0x06);
    SPI_WRT_3PIN(SPI_DATA, 0x00);

    SPI_WRT_3PIN(SPI_COMMAND, PWR_CTRL_1);
    SPI_WRT_3PIN(SPI_DATA, 0xaa);
    SPI_WRT_3PIN(SPI_DATA, 0xae);

    SPI_WRT_3PIN(SPI_COMMAND, DRIVER_OUTPUT);
    SPI_WRT_3PIN(SPI_DATA, 0x32);
    SPI_WRT_3PIN(SPI_DATA, 0xEF);

    SPI_WRT_3PIN(SPI_COMMAND, GATE_SCAN_POS);
    SPI_WRT_3PIN(SPI_DATA, 0x00);
    SPI_WRT_3PIN(SPI_DATA, 0x00);

    SPI_WRT_3PIN(SPI_COMMAND, CYCLE_CTRL);
    SPI_WRT_3PIN(SPI_DATA, 0x52);
    SPI_WRT_3PIN(SPI_DATA, 0x08);

    SPI_WRT_3PIN(SPI_COMMAND, PWR_CTRL_2);
    SPI_WRT_3PIN(SPI_DATA, 0x00);
    SPI_WRT_3PIN(SPI_DATA, 0x05);

    SPI_WRT_3PIN(SPI_COMMAND, 0x002a);
    SPI_WRT_3PIN(SPI_DATA, 0x09);
    SPI_WRT_3PIN(SPI_DATA, 0xd5);

    SPI_WRT_3PIN(SPI_COMMAND, PWR_CTRL_3);
    SPI_WRT_3PIN(SPI_DATA, 0x00);
```

```
    SPI_WRT_3PIN(SPI_DATA, 0x0d);

    SPI_WRT_3PIN(SPI_COMMAND, PWR_CTRL_4);
    SPI_WRT_3PIN(SPI_DATA, 0x24);
    SPI_WRT_3PIN(SPI_DATA, 0x00);

    SPI_WRT_3PIN(SPI_COMMAND, PWR_CTRL_5);
    SPI_WRT_3PIN(SPI_DATA, 0x00);
    SPI_WRT_3PIN(SPI_DATA, 0xac);

    SPI_WRT_3PIN(SPI_COMMAND, V_ADDR);
    SPI_WRT_3PIN(SPI_DATA, 0xEF);
    SPI_WRT_3PIN(SPI_DATA, 0x00);

    SPI_WRT_3PIN(SPI_COMMAND, H_STR_ADDR);
    SPI_WRT_3PIN(SPI_DATA, 0x00);
    SPI_WRT_3PIN(SPI_DATA, 0x00);

    SPI_WRT_3PIN(SPI_COMMAND, H_END_ADDR);
    SPI_WRT_3PIN(SPI_DATA, 0x01);
    SPI_WRT_3PIN(SPI_DATA, 0x3F);

    SPI_WRT_3PIN(SPI_COMMAND, RAM_XADDR);
    SPI_WRT_3PIN(SPI_DATA, 0x00);
    SPI_WRT_3PIN(SPI_DATA, 0x00);

    SPI_WRT_3PIN(SPI_COMMAND, RAM_YADDR);
    SPI_WRT_3PIN(SPI_DATA, 0x00);
    SPI_WRT_3PIN(SPI_DATA, 0x00);

//-------Gamma control---------------------//
    SPI_WRT_3PIN(SPI_COMMAND, 0x30);
    SPI_WRT_3PIN(SPI_DATA, 0x01);
    SPI_WRT_3PIN(SPI_DATA, 0x00);

    SPI_WRT_3PIN(SPI_COMMAND, 0x31);
    SPI_WRT_3PIN(SPI_DATA, 0x00);
    SPI_WRT_3PIN(SPI_DATA, 0x00);

    SPI_WRT_3PIN(SPI_COMMAND, 0x32);
    SPI_WRT_3PIN(SPI_DATA, 0x01);
    SPI_WRT_3PIN(SPI_DATA, 0x06);

    SPI_WRT_3PIN(SPI_COMMAND, 0x33);
    SPI_WRT_3PIN(SPI_DATA, 0x00);
    SPI_WRT_3PIN(SPI_DATA, 0x00);

    SPI_WRT_3PIN(SPI_COMMAND, 0x34);
    SPI_WRT_3PIN(SPI_DATA, 0x00);
    SPI_WRT_3PIN(SPI_DATA, 0x00);
```

```
    SPI_WRT_3PIN(SPI_COMMAND, 0x35);
    SPI_WRT_3PIN(SPI_DATA, 0x04);
    SPI_WRT_3PIN(SPI_DATA, 0x03);

    SPI_WRT_3PIN(SPI_COMMAND, 0x36);
    SPI_WRT_3PIN(SPI_DATA, 0x00);
    SPI_WRT_3PIN(SPI_DATA, 0x00);

    SPI_WRT_3PIN(SPI_COMMAND, 0x37);
    SPI_WRT_3PIN(SPI_DATA, 0x00);
    SPI_WRT_3PIN(SPI_DATA, 0x00);

    SPI_WRT_3PIN(SPI_COMMAND, 0x3a);
    SPI_WRT_3PIN(SPI_DATA, 0x11);
    SPI_WRT_3PIN(SPI_DATA, 0x00);

    SPI_WRT_3PIN(SPI_COMMAND, 0x3b);
    SPI_WRT_3PIN(SPI_DATA, 0x00);
    SPI_WRT_3PIN(SPI_DATA, 0x09);

    SPI_WRT_3PIN(SPI_COMMAND, 0x25);
    SPI_WRT_3PIN(SPI_DATA, 0xe0);
    SPI_WRT_3PIN(SPI_DATA, 0x00);

    SPI_WRT_3PIN(SPI_COMMAND, 0x26);
    SPI_WRT_3PIN(SPI_DATA, 0x38);
    SPI_WRT_3PIN(SPI_DATA, 0x00);
}

void main()
{
    LCD_RST();

    SSD2119_PWR_ON_SEQUENCE();

    SSD2119_35U_SPI_INIT();

    SPI_WRT_3PIN(SPI_COMMAND, GRAM_WRITE);

    //start GRAM writing
    //...
    //end GTAM writing
}
```

```
/***************************************
SSD2119 3-Line SPI +RGB mode initialization
Resolution 320x240
***************************************/

#define SPI_COMMAND 0
#define SPI_DATA    1

//Register Address
#define VCOM_OTP          0x28
#define OSC_START         0x00
#define SLEEP_MODE        0x10
#define DISP_CTRL         0x07
#define ENTRY_MODE        0x11
#define H_PORCH           0x16
#define V_PORCH           0x17
#define LCD_DRIVER        0x02
#define PWR_CTRL_1        0x03
#define DRIVER_OUTPUT     0x01

#define GATE_SCAN_POS     0x0F
#define CYCLE_CTRL        0x0B
#define PWR_CTRL_2        0x0C
#define PWR_CTRL_3        0x0D
#define PWR_CTRL_4        0x0E
#define PWR_CTRL_5        0x1E
#define V_ADDR            0x44
#define H_STR_ADDR        0x45
#define H_END_ADDR        0x46
#define RAM_XADDR         0x4E
#define RAM_YADDR         0x4F

#define GRAM_WRITE        0x22

void SPI_WRT_3PIN(unsigned char DC, unsigned char dat)
{
    unsigned char i;

    SSD2119_CS = 0;
    SSD2119_SCK = 0;
    SSD2119_SDA = DC;
    SSD2119_SCK = 1;

    for(i=0; i < 8; i++)
    {
        SSD2119_SCK = 0;

        if(dat&0x80)
            SSD2119_SDA = 1;
        else
```

```
            SSD2119_SDA = 0;

        dat <<= 1;
        SSD2119_SCK = 1;
    }

    SSD2119_SCK = 0;
    SSD2119_CS = 1;
}

void LCD_RST(void)
{
    IC_RST =1;
    delay(6000);

    IC_RST = 0;
    delay(30000);

    IC_RST = 1;

    delay(60000);
    delay(60000);
}

void SSD2119_PWR_ON_SEQUENCE()
{
    SPI_WRT_3PIN(SPI_COMMAND, DISP_CTRL);
    SPI_WRT_3PIN(SPI_DATA, 0x00);
    SPI_WRT_3PIN(SPI_DATA, 0x08);

    SPI_WRT_3PIN(SPI_COMMAND, OSC_START);
    SPI_WRT_3PIN(SPI_DATA, 0x00);
    SPI_WRT_3PIN(SPI_DATA, 0x01);

    SPI_WRT_3PIN(SPI_COMMAND, DISP_CTRL);
    SPI_WRT_3PIN(SPI_DATA, 0x00);
    SPI_WRT_3PIN(SPI_DATA, 0x23);

    SPI_WRT_3PIN(SPI_COMMAND, SLEEP_MODE);
    SPI_WRT_3PIN(SPI_DATA, 0x00);
    SPI_WRT_3PIN(SPI_DATA, 0x00);

    delay(60000);
    delay(60000);
    delay(60000);
    delay(60000);
    delay(60000);
    delay(60000);
    delay(60000);
    delay(60000);
```

```
    SPI_WRT_3PIN(SPI_COMMAND, DISP_CTRL);
    SPI_WRT_3PIN(SPI_DATA, 0x00);
    SPI_WRT_3PIN(SPI_DATA, 0x33);
}

void SSD2119_35U_SPI_INIT()
{
    SPI_WRT_3PIN(SPI_COMMAND, ENTRY_MODE);//check sync, den later
    SPI_WRT_3PIN(SPI_DATA, 0xC7);
    SPI_WRT_3PIN(SPI_DATA, 0x30);

    SPI_WRT_3PIN(SPI_COMMAND, H_PORCH);
    SPI_WRT_3PIN(SPI_DATA, 0x00);
    SPI_WRT_3PIN(SPI_DATA, SSD2119_HBP);

    SPI_WRT_3PIN(SPI_COMMAND, V_PORCH);
    SPI_WRT_3PIN(SPI_DATA, SSD2119_VFP);
    SPI_WRT_3PIN(SPI_DATA, SSD2119_VBP);

    SPI_WRT_3PIN(SPI_COMMAND, LCD_DRIVER);   //lcd driver
    SPI_WRT_3PIN(SPI_DATA, 0x06);
    SPI_WRT_3PIN(SPI_DATA, 0x00);

    SPI_WRT_3PIN(SPI_COMMAND, PWR_CTRL_1);
    SPI_WRT_3PIN(SPI_DATA, 0xaa);
    SPI_WRT_3PIN(SPI_DATA, 0xae);

    SPI_WRT_3PIN(SPI_COMMAND, DRIVER_OUTPUT);
    SPI_WRT_3PIN(SPI_DATA, 0x32);
    SPI_WRT_3PIN(SPI_DATA, 0xEF);

    SPI_WRT_3PIN(SPI_COMMAND, GATE_SCAN_POS);
    SPI_WRT_3PIN(SPI_DATA, 0x00);
    SPI_WRT_3PIN(SPI_DATA, 0x00);

    SPI_WRT_3PIN(SPI_COMMAND, CYCLE_CTRL);
    SPI_WRT_3PIN(SPI_DATA, 0x52);
    SPI_WRT_3PIN(SPI_DATA, 0x08);

    SPI_WRT_3PIN(SPI_COMMAND, PWR_CTRL_2);
    SPI_WRT_3PIN(SPI_DATA, 0x00);
    SPI_WRT_3PIN(SPI_DATA, 0x05);

    SPI_WRT_3PIN(SPI_COMMAND, 0x002a);
    SPI_WRT_3PIN(SPI_DATA, 0x09);
    SPI_WRT_3PIN(SPI_DATA, 0xd5);

    SPI_WRT_3PIN(SPI_COMMAND, PWR_CTRL_3);
    SPI_WRT_3PIN(SPI_DATA, 0x00);
```

```
    SPI_WRT_3PIN(SPI_DATA, 0x0d);

    SPI_WRT_3PIN(SPI_COMMAND, PWR_CTRL_4);
    SPI_WRT_3PIN(SPI_DATA, 0x24);
    SPI_WRT_3PIN(SPI_DATA, 0x00);

    SPI_WRT_3PIN(SPI_COMMAND, PWR_CTRL_5);
    SPI_WRT_3PIN(SPI_DATA, 0x00);
    SPI_WRT_3PIN(SPI_DATA, 0xac);

    SPI_WRT_3PIN(SPI_COMMAND, V_ADDR);
    SPI_WRT_3PIN(SPI_DATA, 0xEF);
    SPI_WRT_3PIN(SPI_DATA, 0x00);

    SPI_WRT_3PIN(SPI_COMMAND, H_STR_ADDR);
    SPI_WRT_3PIN(SPI_DATA, 0x00);
    SPI_WRT_3PIN(SPI_DATA, 0x00);

    SPI_WRT_3PIN(SPI_COMMAND, H_END_ADDR);
    SPI_WRT_3PIN(SPI_DATA, 0x01);
    SPI_WRT_3PIN(SPI_DATA, 0x3F);

    SPI_WRT_3PIN(SPI_COMMAND, RAM_XADDR);
    SPI_WRT_3PIN(SPI_DATA, 0x00);
    SPI_WRT_3PIN(SPI_DATA, 0x00);

    SPI_WRT_3PIN(SPI_COMMAND, RAM_YADDR);
    SPI_WRT_3PIN(SPI_DATA, 0x00);
    SPI_WRT_3PIN(SPI_DATA, 0x00);

//-------Gamma control---------------------//
    SPI_WRT_3PIN(SPI_COMMAND, 0x30);
    SPI_WRT_3PIN(SPI_DATA, 0x01);
    SPI_WRT_3PIN(SPI_DATA, 0x00);

    SPI_WRT_3PIN(SPI_COMMAND, 0x31);
    SPI_WRT_3PIN(SPI_DATA, 0x00);
    SPI_WRT_3PIN(SPI_DATA, 0x00);

    SPI_WRT_3PIN(SPI_COMMAND, 0x32);
    SPI_WRT_3PIN(SPI_DATA, 0x01);
    SPI_WRT_3PIN(SPI_DATA, 0x06);

    SPI_WRT_3PIN(SPI_COMMAND, 0x33);
    SPI_WRT_3PIN(SPI_DATA, 0x00);
    SPI_WRT_3PIN(SPI_DATA, 0x00);

    SPI_WRT_3PIN(SPI_COMMAND, 0x34);
    SPI_WRT_3PIN(SPI_DATA, 0x00);
    SPI_WRT_3PIN(SPI_DATA, 0x00);
```

```
    SPI_WRT_3PIN(SPI_COMMAND, 0x35);
    SPI_WRT_3PIN(SPI_DATA, 0x04);
    SPI_WRT_3PIN(SPI_DATA, 0x03);

    SPI_WRT_3PIN(SPI_COMMAND, 0x36);
    SPI_WRT_3PIN(SPI_DATA, 0x00);
    SPI_WRT_3PIN(SPI_DATA, 0x00);

    SPI_WRT_3PIN(SPI_COMMAND, 0x37);
    SPI_WRT_3PIN(SPI_DATA, 0x00);
    SPI_WRT_3PIN(SPI_DATA, 0x00);

    SPI_WRT_3PIN(SPI_COMMAND, 0x3a);
    SPI_WRT_3PIN(SPI_DATA, 0x11);
    SPI_WRT_3PIN(SPI_DATA, 0x00);

    SPI_WRT_3PIN(SPI_COMMAND, 0x3b);
    SPI_WRT_3PIN(SPI_DATA, 0x00);
    SPI_WRT_3PIN(SPI_DATA, 0x09);

    SPI_WRT_3PIN(SPI_COMMAND, 0x25);
    SPI_WRT_3PIN(SPI_DATA, 0xe0);
    SPI_WRT_3PIN(SPI_DATA, 0x00);

    SPI_WRT_3PIN(SPI_COMMAND, 0x26);
    SPI_WRT_3PIN(SPI_DATA, 0x38);
    SPI_WRT_3PIN(SPI_DATA, 0x00);
}

void SSD1963_INIT() //To be modified 20210625
{
    //sw reset
    Write_Command(0x01);        //Software Reset
    delay(10000);

    //config PLL clk, 0xE2
    //10MHz to 10MHz
    Write_Command(0xE2);
    Write_Data(SSD1963_PLL_M);
    Write_Data(SSD1963_PLL_N);
    Write_Data(SSD1963_PLL_C);

    //turn on PLL
    Command_Write(0xe0,0x01);       //START PLL
    delay(10000);

    //Switch clk source to PLL
    Command_Write(0xe0,0x03);       //LOCK PLL
    delay(10000);
```

```
//sw reset
Write_Command(0x01);        //Software Reset
delay(10000);

//configuration dot clk, 0xE6
//10M Hz to 5M Hz
Write_Command(0xE6);
Write_Data(SSD1963_LCDC_FPR_HB);
Write_Data(SSD1963_LCDC_FPR_MB);
Write_Data(SSD1963_LCDC_FPR_LB);

//configuration LCD setting

Write_Command(0xb0);          //SET LCD MODE    SET TFT 18Bits MODE
Write_Data(0x04);
Write_Data(0x20);           //SET TFT MODE & hsync+Vsync+DEN MODE
Write_Data(0x01);           //SET horizontal size=240-1 HightByte
Write_Data(0x3f);           //SET horizontal size=240-1 LowByte
Write_Data(0x00);           //SET vertical size=320-1 HightByte
Write_Data(0xEF);           //SET vertical size=320-1 LowByte
Write_Data(0x00);           //SET even/odd line RGB seq.=RGB

Command_Write(0xf0,0x03);   //SET pixel data I/F format=16bit(565 format)
Command_Write(0x36,0x00);        // SET read from frame buffer to the display is RGB

Write_Command(0xb4);          //SET HSYNC
Write_Data(0x01);             //SET HSYNC Tatol = 440
Write_Data(0xb8);
Write_Data(0x00);             //SET HBP = 68
Write_Data(0x44);
Write_Data(0x07);             //SET VBP 16 = 15 + 1
Write_Data(0x00);             //SET Hsync pulse start position
Write_Data(0x00);             //SET Hsync pulse subpixel start position

Write_Command(0xb6);          //SET VSYNC
Write_Data(0x01);             //SET Vsync total 265 = 264 + 1
Write_Data(0x08);
Write_Data(0x00);             //SET VBP = 19
Write_Data(0x13);
Write_Data(0x07);             //SET Vsync pulse 8 = 7 + 1
Write_Data(0x00);             //SET Vsync pulse start position
Write_Data(0x00);

Write_Command(0x2a);          //SET column address
Write_Data(0x00);             //SET start column address=0
Write_Data(0x00);
Write_Data(0x01);             //SET end column address=240      Write_Data(0x00);
Write_Data(0x3F);             // Write_Data(0xEF);
```

```
    Write_Command(0x2b);        //SET page address
    Write_Data(0x00);           //SET start page address=0
    Write_Data(0x00);           //Write_Data(0x00);
    Write_Data(0x00);           //SET end page address=320        Write_Data(0x01);
    Write_Data(0xEF);           //Write_Data(0x3F);

    Write_Command(0xb8);            //SET GPIO
    Write_Data(0x0f);               //SET I/O
    Write_Data(0x01);

    Write_Command(0xba);            //SET GPIO
    Write_Data(0x01);           //SET I/O

    delay(1000);
}

void main()
{
    LCD_RST();

    SSD2119_PWR_ON_SEQUENCE();

    SSD2119_35U_SPI_INIT();

    SSD1963_INIT();

    Write_Command(0x29);

    Write_Command(0x2C);

    //start GRAM writing
    //...
    //end GTAM writing
}
```

winstar

LCM Sample Estimate Feedback Sheet

Module Number： _____ **Page: 1**

1、Panel Specification：

1. Panel Type： ☐ Pass ☐ NG ,_____
2. View Direction： ☐ Pass ☐ NG ,_____
3. Numbers of Dots： ☐ Pass ☐ NG ,_____
4. View Area： ☐ Pass ☐ NG ,_____
5. Active Area： ☐ Pass ☐ NG ,_____
6. Operating Temperature： ☐ Pass ☐ NG ,_____
7. Storage Temperature： ☐ Pass ☐ NG ,_____
8. Others：_____

2、Mechanical Specification：

1. PCB Size： ☐ Pass ☐ NG ,_____
2. Frame Size： ☐ Pass ☐ NG ,_____
3. Material of Frame： ☐ Pass ☐ NG ,_____
4. Connector Position： ☐ Pass ☐ NG ,_____
5. Fix Hole Position： ☐ Pass ☐ NG ,_____
6. Backlight Position： ☐ Pass ☐ NG ,_____
7. Thickness of PCB： ☐ Pass ☐ NG ,_____
8. Height of Frame to PCB： ☐ Pass ☐ NG ,_____
9. Height of Module： ☐ Pass ☐ NG ,_____
10. Others： ☐ Pass ☐ NG ,_____

3、Relative Hole Size：

1. Pitch of Connector： ☐ Pass ☐ NG ,_____
2. Hole size of Connector： ☐ Pass ☐ NG ,_____
3. Mounting Hole size： ☐ Pass ☐ NG ,_____
4. Mounting Hole Type： ☐ Pass ☐ NG ,_____
5. Others： ☐ Pass ☐ NG ,_____

4、Backlight Specification：

1. B/L Type： ☐ Pass ☐ NG ,_____
2. B/L Color： ☐ Pass ☐ NG ,_____
3. B/L Driving Voltage (Reference for LED Type)： ☐ Pass ☐ NG ,_____
4. B/L Driving Current： ☐ Pass ☐ NG ,_____
5. Brightness of B/L： ☐ Pass ☐ NG ,_____
6. B/L Solder Method： ☐ Pass ☐ NG ,_____
7. Others： ☐ Pass ☐ NG ,_____

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5、Electronic Characteristics of Module：

1.	Input Voltage：	☐ Pass	☐ NG ,_____
2.	Supply Current：	☐ Pass	☐ NG ,_____
3.	Driving Voltage for LCD：	☐ Pass	☐ NG ,_____
4.	Contrast for LCD：	☐ Pass	☐ NG ,_____
5.	B/L Driving Method：	☐ Pass	☐ NG ,_____
6.	Negative Voltage Output：	☐ Pass	☐ NG ,_____
7.	Interface Function：	☐ Pass	☐ NG ,_____
8.	LCD Uniformity：	☐ Pass	☐ NG ,_____
9.	ESD test：	☐ Pass	☐ NG ,_____
10.	Others：	☐ Pass	☐ NG ,_____

6、Summary：

Sales signature：_____

Customer Signature：_____ **Date：** / /