RClamp1011ZC

Femto Farad RailClamp®
1-Line, 200fF ESD Protection

PROTECTION PRODUCTS

Description

RClamp®1011ZC is an ultra low capacitance FemtoClamp™ ESD protection device specifically designed to protect high-speed differential lines. It offers desirable characteristics for board level protection including fast response time, low operating and clamping voltage, and no device degradation.

RClamp1011ZC features excellent ESD protection characteristics highlighted by low peak ESD clamping voltage, and high ESD withstand voltage per IEC 61000-4-2 (±10kV contact). RClamp1011ZC has a maximum capacitance of only 0.2pF and extremely low insertion loss allowing it to be used on high speed lines such as Thunderbolt 4 and USB4.

RClamp1011ZC is in a DFN 0.60 x 0.30 x 0.25 mm 2-Lead package. The small package gives the designer the flexibility to protect single lines in applications where arrays are not practical.

Features

- ESD withstand voltage
  - IEC 61000-4-2 (ESD) ±10kV (contact)
- Low ESD Clamping
- Ultra-Low capacitance: 0.2pF Maximum
- Protects one high-speed data line
- Working voltage: 1.0V
- Low reverse leakage current: 500nA max at V_R=1.0V
- Solid-state silicon-avalanche technology

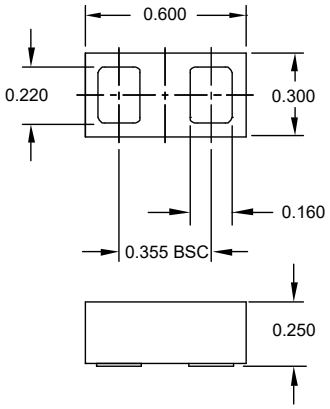
Mechanical Characteristics

- Package: DFN 0.60 x 0.30 x 0.25 mm 2-Lead
- Pb-Free, Halogen Free, RoHS/WEEE Compliant
- Lead Finish: Pb-Free
- Marking : Marking Code
- Packaging : Tape and Reel

Applications

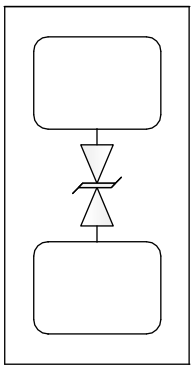
- Thunderbolt 3
- Thunderbolt 4
- USB Type-C
- USB 3.2 Gen 2
- USB4

Nominal Dimensions



Nominal Dimensions in mm

Schematic and Pin Configuration



RClamp1011ZC (Bottom View)

Absolute Maximum Ratings

Rating	Symbol	Value	Units
Peak Pulse Current (tp = 8/20µs)	I_{PP}	2.5	A
ESD per IEC 61000-4-2 (Contact)(1) ESD per IEC 61000-4-2 (Air)(1)(2)	V_{ESD}	±10 ±15	kV
Operating Temperature	T_{OP}	-40 to +85	°C
Junction Temperature and Storage Temperature	T_J and T_{STG}	-55 to +150	°C

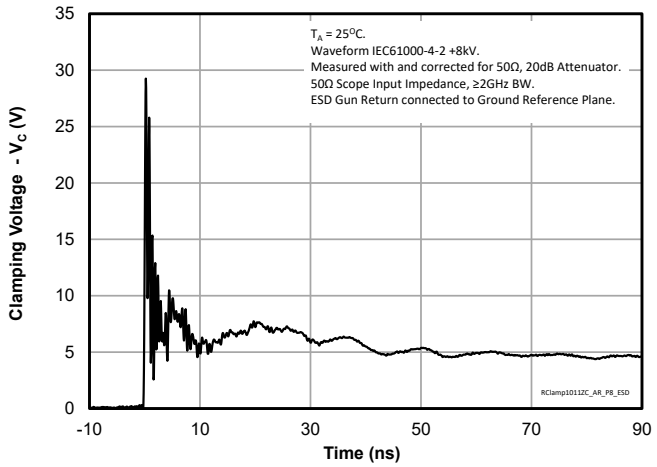
Electrical Characteristics (T=25°C unless otherwise specified)

Parameter	Symbol	Conditions		Min.	Typ.	Max.	Units
Reverse Stand-Off Voltage	V_{RWM}	-40°C to 85°C				1.0	V
Reverse Breakdown Voltage	V_{BR}	I_t = 1mA		1.3	1.5	2.3	V
Reverse Leakage Current	I_R	V_{RWM} = 1.0V			30	500	nA
Clamping Voltage(3)	V_C	tp = 8/20µs	I_{PP} = 2.5A		2.77	4.0	V
ESD Clamping Voltage(4)	V_C	tp = 0.2/100ns (TLP)	I_{PP} = 4A		3.4		V
			I_{PP} = 8A		4.7		
Dynamic Resistance(4)(5)	R_{DYN}	tp = 0.2/100ns (TLP)			0.32		Ohms
Junction Capacitance	C_J	V_R = 0V, f = 1MHz			0.17	0.2	pF
Insertion Loss	S_{21}	f = 5 GHz			0.17		dB
		f= 10 GHz			0.33		
		f= 13 GHz			0.39		

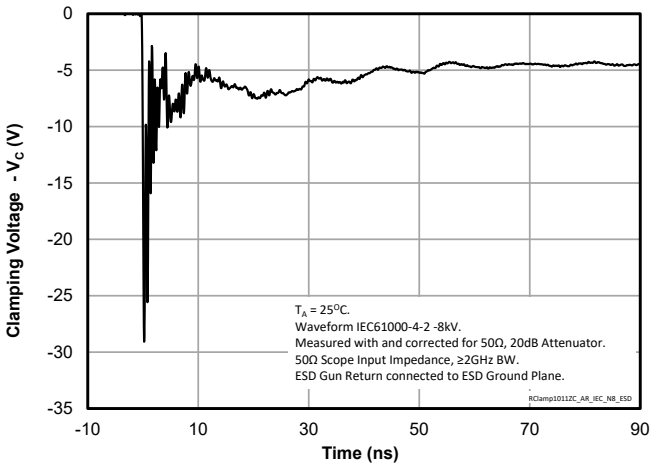
Notes:
(1): ESD gun return path connected to Ground Reference Plane (GRP).
(2): Air discharge rated for in system withstand voltage
(3): Measured using a 1.2/50µs voltage, 8/20µs current combination waveform, R_S = 12 Ohms. Clamping is defined as the peak voltage across the device after the device snaps back to a conducting state.
(4): Transmission Line Pulse Test (TLP) Settings: tp = 100ns, tr = 0.2ns, I_{TLP} and V_{TLP} averaging window: t_1 = 70ns to t_2 = 90ns.
(5): Dynamic resistance calculated from I_{TLP} = 4A to I_{TLP} = 8A

Typical Characteristics

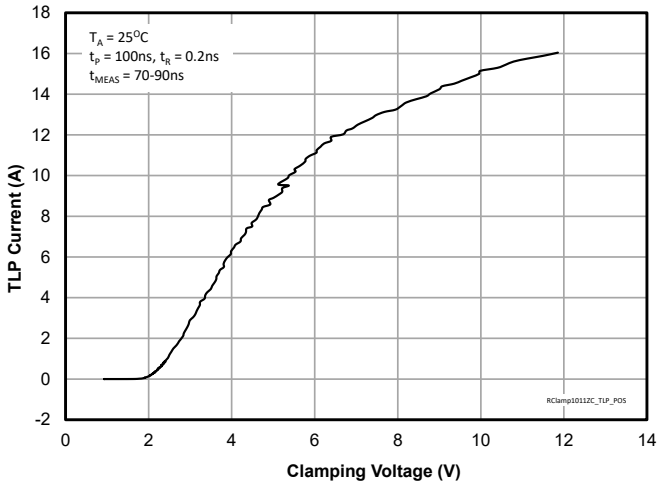
ESD Clamping (+8kV Contact per IEC 61000-4-2)



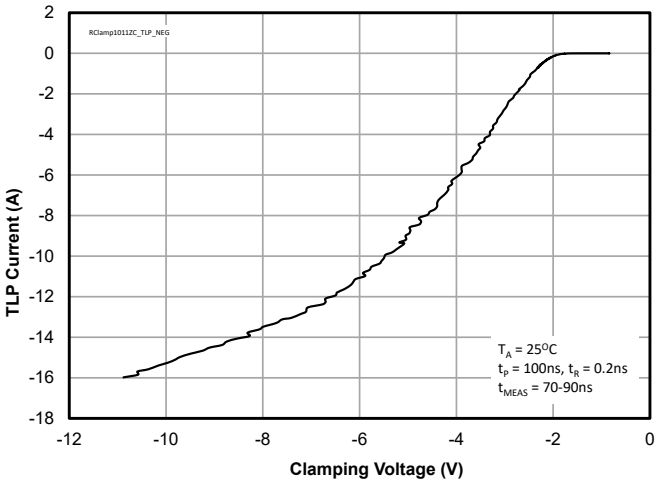
ESD Clamping (-8kV Contact per IEC 61000-4-2)



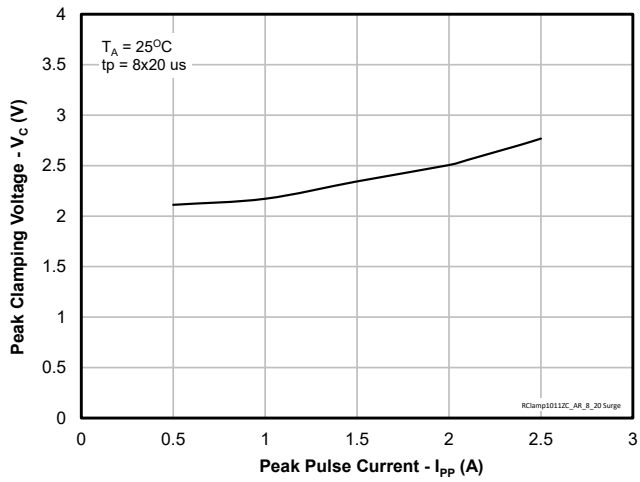
TLP Characteristic (Positive Pulse)



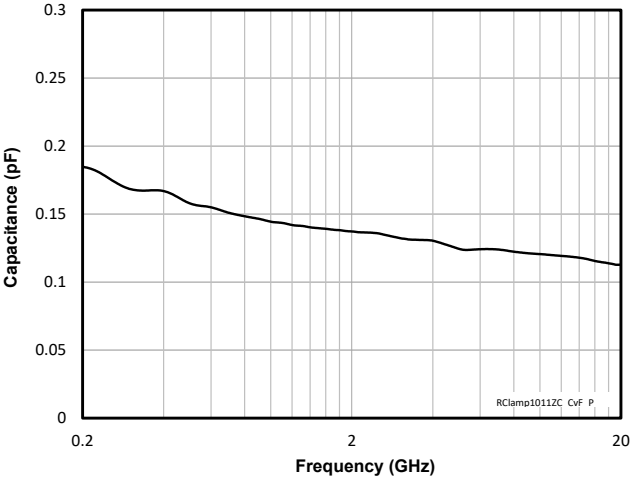
TLP Characteristic (Negative Pulse)



Clamping Voltage vs. Peak Pulse Current (t_p=8/20µs)

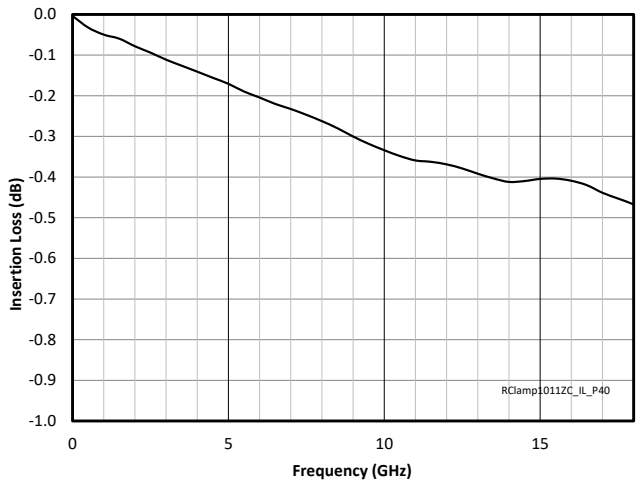


Capacitance vs. Frequency

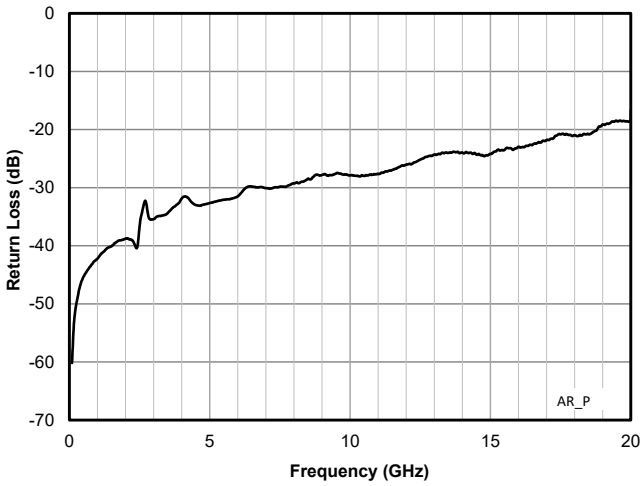


Typical Characteristics

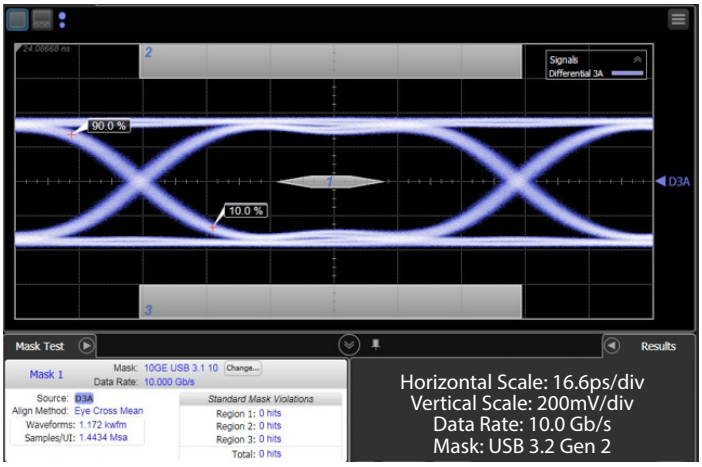
Insertion Loss (S21)



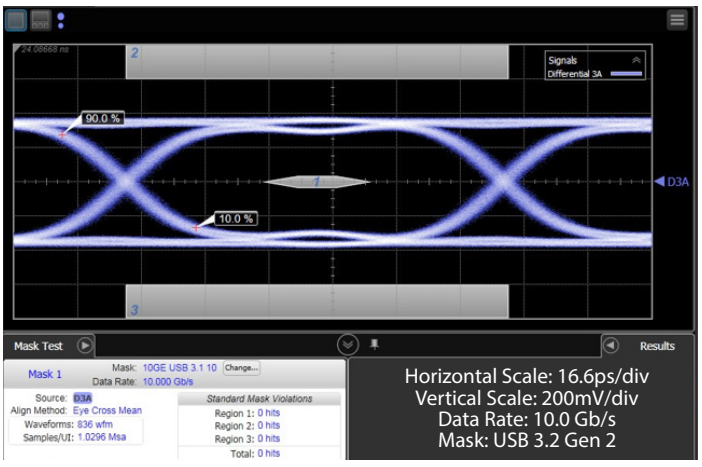
Return Loss (S11)



10Gb/s (USB 3.2 Gen 2) Eye Diagram with RClamp1011ZC



10Gb/s (USB 3.2 Gen 2) Eye Diagram without RClamp1011ZC

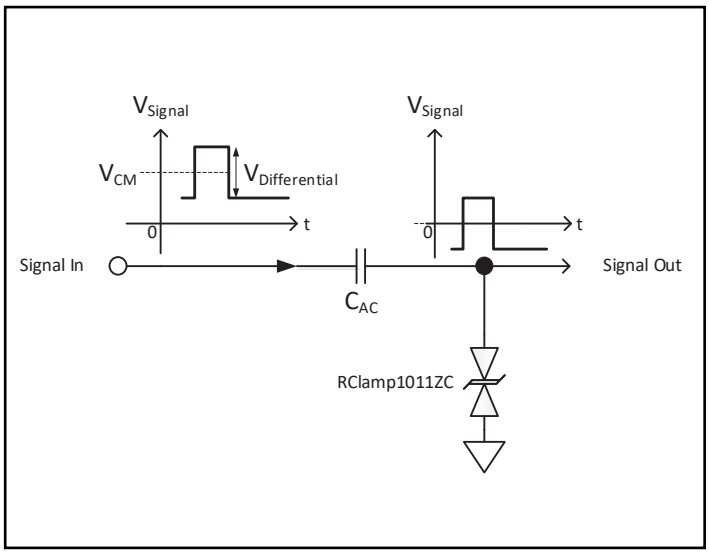


Application Information

Device Placement for High Speed Applications

RClamp1011ZC is specifically designed for ESD protection of Thunderbolt 3 and USB 3.x high speed data lines. It features low maximum capacitance of 0.2pF and operates with a maximum working voltage of 1V. In applications where the common mode voltage is higher than 1V, placement of the RClamp1011ZC with respect to the AC coupling capacitors is critical. A general diagram for the placement of the RClamp1011ZC with respect to the AC coupling capacitors is shown in Figure 1. If the line to be protected operates at a voltage higher than the 1V working voltage, the TVS should be placed on the AC coupled side of the signal. This will block the common mode voltage and restrict the voltage across the TVS to the differential signal voltage. For differential signal voltages less than the 1V working voltage maximum, RClamp1011ZC will be operational and effectively protect the line.

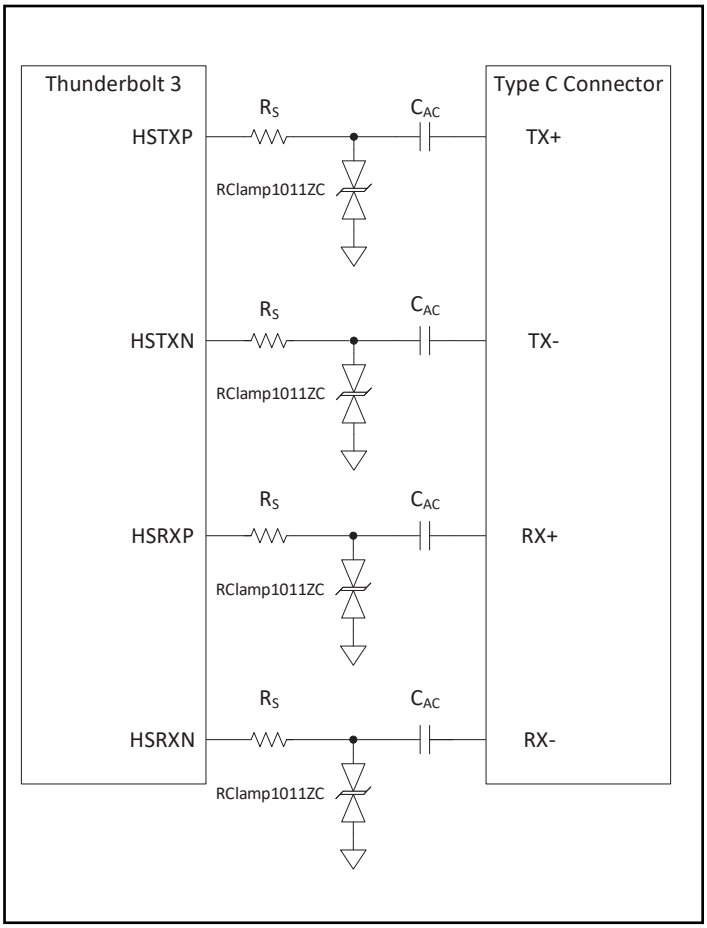
Figure 1 - RClamp1011ZC and AC Coupling Capacitor



Thunderbolt 3 Protection

A typical protection scheme for a differential pair of Thunderbolt 3 high speed data lines is shown in Figure 2. In this configuration the high speed Thunderbolt 3 lines are transmitting with a maximum output voltage of less than 1V, therefore the TVS can be placed on the transceiver side of the AC coupling capacitor. By placing RClamp1011ZC on the transceiver side of AC coupling capacitors on the RX line, the voltage across the TVS is restricted to the differential signal voltage, even when operating in alternate modes interfacing to DisplayPort 1.4a and HDMI. These interfaces can transmit at higher common mode voltages, and their maximum differential signal voltages are within the operating range of the RClamp1011ZC.

Figure 2 - Thunderbolt 3 Protection



Application Information Continued

DisplayPort Line Protection

When RClamp1011ZC is used to protect a dedicated DisplayPort signal line, AC coupling capacitors should be used on both TX and RX lines as shown in Figure 3. In this case, the TVS should be placed on the connector side of the AC coupling capacitor to block the common mode voltage from TX signals. On the RX line the TVS should be placed on the transceiver side of the AC coupling capacitor to block the common mode voltages of incoming signals.

USB 3.2 and USB4 Protection

RClamp1011ZC can also be used to protect USB SuperSpeed lines. Figure 4 shows an example of four SuperSpeed lines which are protected by RClamp1011ZC. As per the USB specifications, AC coupling capacitors are required on TX lines. In this case, the RClamp1011ZC should be placed on the connector side of the AC coupling capacitor as shown in Figure 3. It is recommended that AC coupling capacitors are used for RX lines. In that case, the TVS should be placed on the transceiver side of the capacitor.

Figure 3 - DisplayPort Line Protection

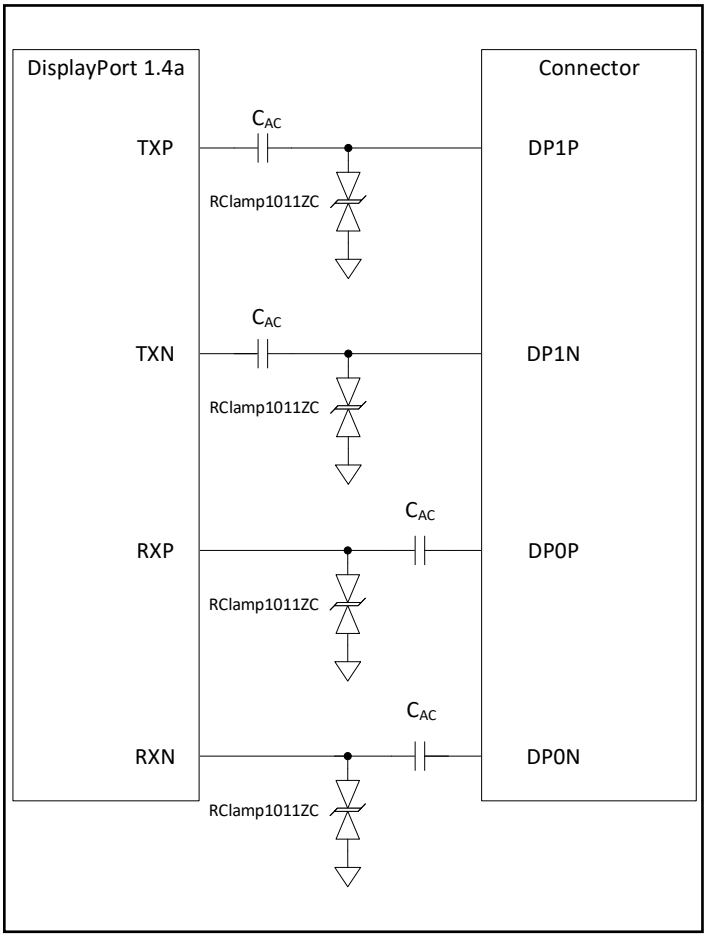
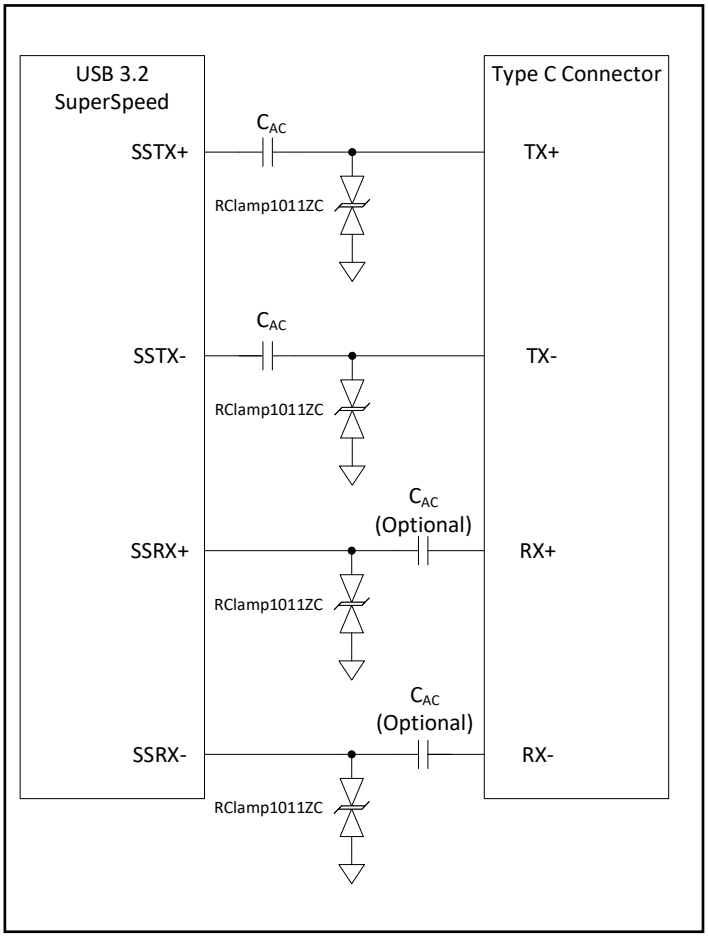


Figure 4 - USB 3.2 Protection



Application Information

Assembly Guidelines

The figure at the right details Semtech's recommended mounting pattern. Recommended assembly guidelines are shown in Table 1. Note that these are only recommendations and should serve only as a starting point for design since there are many factors that affect the assembly process. Exact manufacturing parameters will require some experimentation to get the desired solder application.

Solder Stencil

Stencil design is one of the key factors which will determine the volume of solder paste which is deposited onto the land pad. The area ratio of the stencil aperture will determine how well the stencil will print. The area ratio takes into account the aperture shape, aperture size, and stencil thickness. A minimum area ratio of 0.66 is preferred for the subject package. The area ratio of a rectangular aperture is given as:

Area Ratio = (L * W)/ (2 * (L + W) * T)

Where:

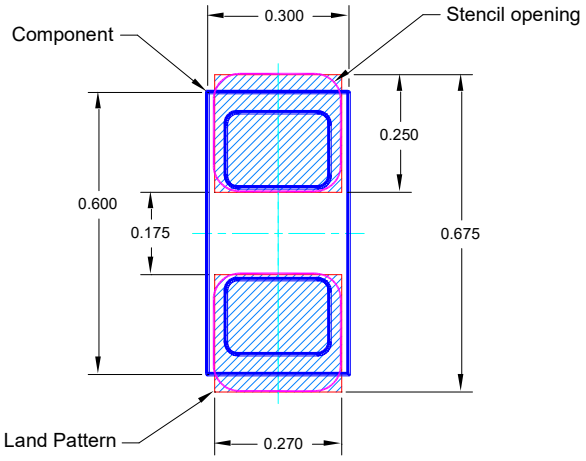
L = Aperture Length

W = Aperture Width

T = Stencil Thickness

Semtech recommends a stencil with square aperture and rounded corners for consistent solder release. The stencil should be laser cut with electro-polished finish. A stencil thickness of 0.075mm (0.003") is recommended. A 0.100mm (0.004") stencil may be used, however the stencil opening may need to be increased slightly to achieve the desired area ratio to ensure proper solder coverage on the pad.

Recommended Mounting Pattern



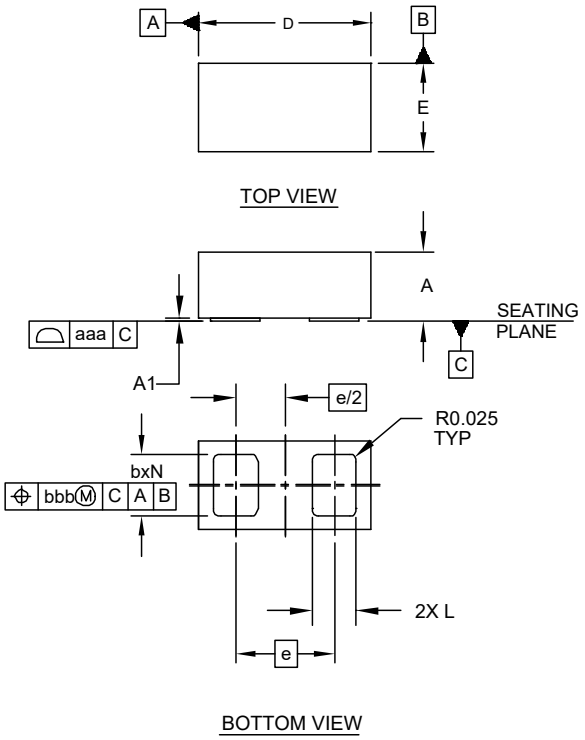
All Dimensions are in mm.

Land Pad. Stencil opening Component

Table 1 - Assembly Guidelines

Assembly Parameter	Recommendation
Solder Stencil Design	Laser Cut, Electro-Polished
Aperture Shape	Rectangular with Rounded Corners
Solder Stencil Thickness	0.075mm (0.003") or 0.100mm (0.004")
Solder Paste Type	Type 4 Size Sphere or Smaller
Solder Reflow Profile	Per JEDEC J-STD-020
PCB Solder Pad Design	Solder Mask Defined or Non Solder Mask Defined
PCB Pad Finish	OSP or NiAu

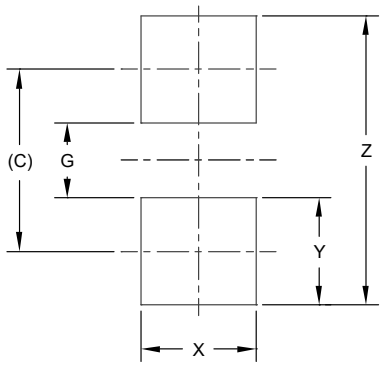
Outline Drawing - DFN 0.60 x 0.30 x 0.25mm 2-Lead



DIMENSIONS			
DIM	MILLIMETERS		
	MIN	NOM	MAX
A	0.235	0.250	0.265
A1	0.000	0.010	0.050
b	0.200	0.220	0.240
D	0.580	0.600	0.620
E	0.280	0.300	0.320
e	0.355 BSC		
L	0.140	0.160	0.180
N	2		
aaa	0.08		
bbb	0.10		

NOTES:
1. CONTROLLING DIMENSIONS ARE IN MILLIMETERS (ANGLES IN DEGREES).

Land Pattern - DFN 0.60 x 0.30 x 0.25mm 2-Lead



DIMENSIONS	
DIM	MILLIMETERS
(C)	(0.425)
G	0.175
X	0.270
Y	0.250
Z	0.675

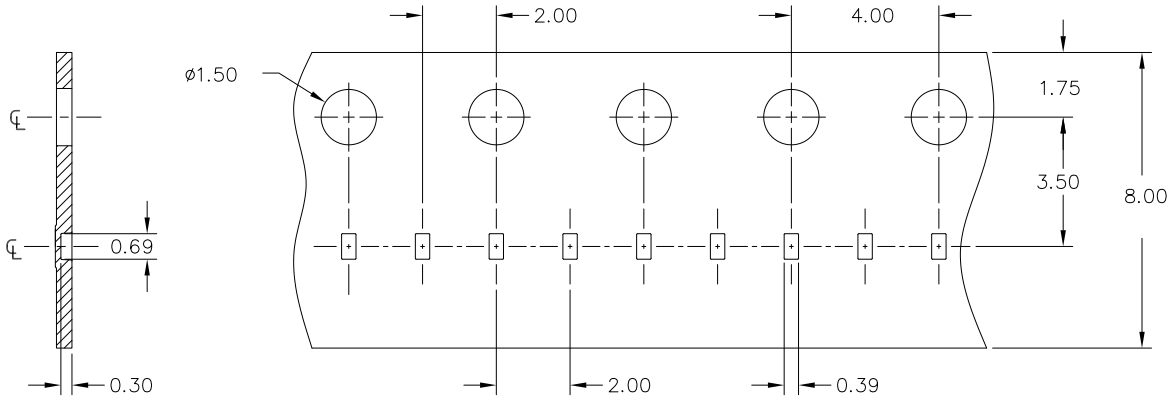
NOTES:
1. CONTROLLING DIMENSIONS ARE IN MILLIMETERS (ANGLES IN DEGREES).
2. THIS LAND PATTERN IS FOR REFERENCE PURPOSES ONLY. CONSULT YOUR MANUFACTURING GROUP TO ENSURE YOUR COMPANY'S MANUFACTURING GUIDELINES ARE MET.

Marking Code

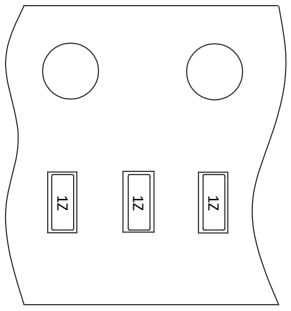
1Z

Notes: Device is electrically symmetrical.

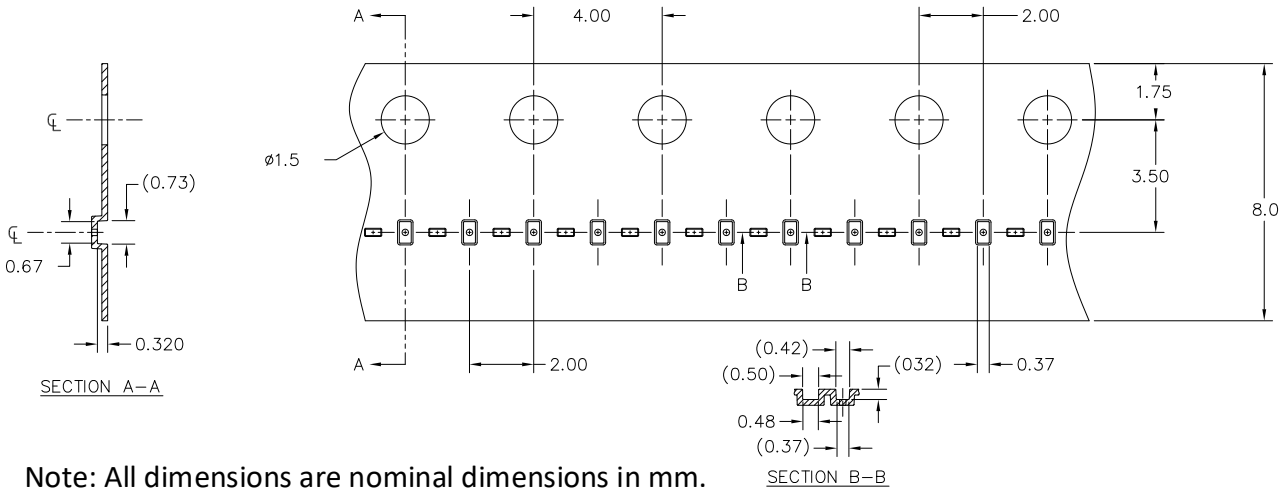
Tape and Reel Specification- Paper Tape



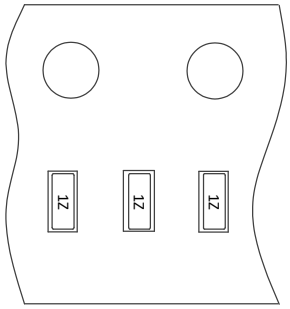
Note: All dimensions are nominal dimensions in mm.



Tape and Reel Specification - Plastic Tape



Note: All dimensions are nominal dimensions in mm.



Ordering Information

Part Number	Tape Material	Qty per Reel	Reel Size
RClamp1011ZCTFT	Paper	15000	7 Inch
RClamp1011ZCTNT	Plastic	10000	7 Inch
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