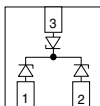


Bidirectional Symmetrical (BiSy) Low Capacitance, Dual-Line ESD Protection Diode in DFN1110-3A


DFN1110-3A

MARKING (example only)



Dot = pin marking

X = date code

Y = type code (see table below)

FEATURES

- For CAN FD Bus applications
- Small DFN1110-3A
- 2-line ESD protection
- Working range ± 33 V
- Low leakage current $I_R < 0.05 \mu A$
- Low load capacitance $C_D < 6$ pF (at $V_R = 5$ V)
- ESD immunity acc. IEC 61000-4-2
 ± 20 kV contact discharge
 ± 20 kV air discharge
- ESD capability according to AEC-Q101:
human body model: class H3B: > 8 kV
- e3 - pins side wall plated with tin (Sn)
- AOI capable
- AEC-Q101 qualified available
- Material categorization: for definitions of compliance please see www.vishay.com/doc?99912



LINKS TO ADDITIONAL RESOURCES



3D Models



Application Notes



SPICE Models

ORDERING INFORMATION					
PART NUMBER (EXAMPLE)	ENVIRONMENTAL AND QUALITY CODE			PACKAGING CODE	ORDERING CODE (EXAMPLE)
	AEC-Q101 QUALIFIED	RoHS-COMPLIANT + LEAD (Pb)-FREE TERMINATIONS	TIN PLATED	10K PER 7" REEL (8 mm TAPE) 10K = MOQ	
		GREEN			
VCAN33A2-HT5	-	G	3	-08	VCAN33A2-HT5-G3-08
VCAN33A2-HT5	H	G	3	-08	VCAN33A2-HT5HG3-08

PACKAGE DATA						
DEVICE NAME	PACKAGE NAME	TYPE CODE	WEIGHT	MOLDING COMPOUND FLAMMABILITY RATING	MOISTURE SENSITIVITY LEVEL	SOLDERING CONDITIONS
VCAN33A2-HT5	DFN1110-3A	B	1.43 mg	UL 94 V-0	MSL level 1 (according J-STD-020)	Peak temperature max. 260 °C

ABSOLUTE MAXIMUM RATINGS				
PARAMETER	TEST CONDITIONS	SYMBOL	VALUE	UNIT
Peak pulse current	$T_A = 25$ °C, acc. IEC 61000-4-5; $t_p = 8/20$ μs ; single shot	I_{PPM}	1.6	A
Peak pulse power	$T_A = 25$ °C; pin 1 or 2 to pin 3; acc. IEC 61000-4-5; $t_p = 8/20$ μs ; single shot	P_{PP}	82	W
ESD immunity	Contact discharge acc. IEC 61000-4-2; 10 pulses, $T_A = 25$ °C	V_{ESD}	± 20	kV
	Air discharge acc. IEC 61000-4-2; 10 pulses, $T_A = 25$ °C		± 20	kV
Operating temperature	Junction temperature	T_J	-55 to +150	°C
Storage temperature		T_{STG}	-55 to +150	°C

ELECTRICAL CHARACTERISTICS (pin 1 to 3, 3 to 1, 2 to 3, or 3 to 2)

($T_{amb} = 25\text{ }^{\circ}\text{C}$, unless otherwise specified)

PARAMETER	TEST CONDITIONS/REMARKS	SYMBOL	MIN.	TYP.	MAX.	UNIT
Protection paths	Number of lines which can be protected	$N_{channel}$	-	-	2	lines
Reverse stand-off voltage	Max. reverse working voltage	V_{RWM}	-	-	33	V
Reverse voltage	At $I_R = 0.05\text{ }\mu\text{A}$	V_R	33	-	-	V
Reverse current	At $V_{RWM} = 33\text{ V}$	I_R	-	-	0.05	μA
Reverse breakdown voltage	At $I_R = 1\text{ mA}$	V_{BR}	36	38	40	V
Reverse clamping voltage	At $I_{PP} = 1\text{ A}$; $t_p = 8/20\text{ }\mu\text{s}$	V_C	-	-	48	V
	At $I_{PP} = I_{PPM} = 1.6\text{ A}$; $t_p = 8/20\text{ }\mu\text{s}$	V_C	-	47	52	V
	Diode capacitance matching at $V_R = 5\text{ V}$, C_{D13} vs. C_{D23}	dC_D	-	-	0.12	pF
Capacitance	At $V_R = 0\text{ V}$, $f = 1\text{ MHz}$	C_D	-	6	8	pF
	At $V_R = 5\text{ V}$, $f = 1\text{ MHz}$		-	4.1	6	pF

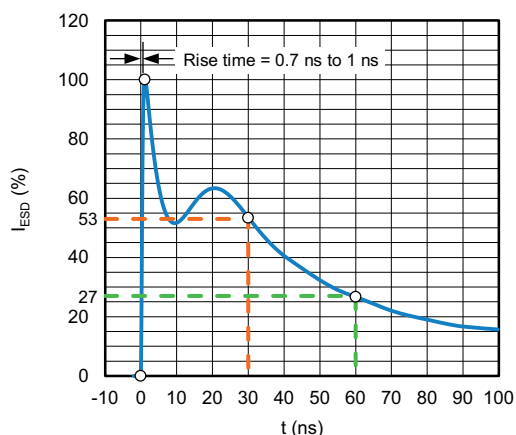
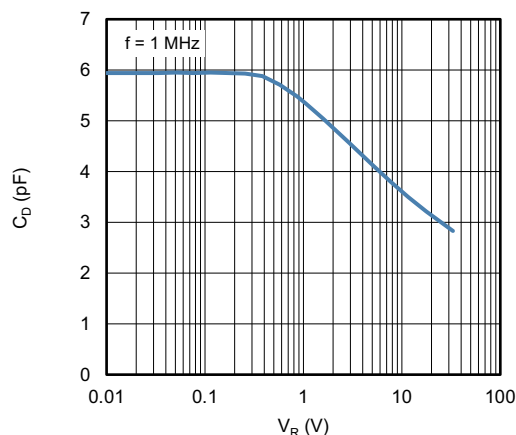

Fig. 1 - ESD Discharge Current Wave Form acc. IEC 61000-4-2 (330 Ω /150 pF)


Fig. 3 - Typical Capacitance vs. Reverse Voltage

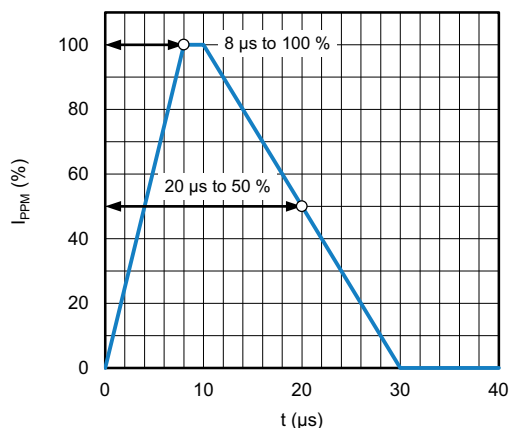
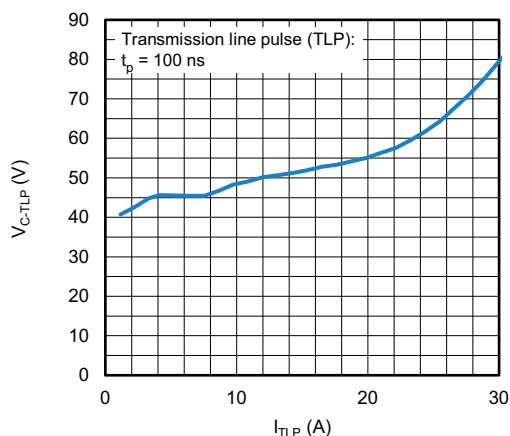

Fig. 2 - 8/20 μs Peak Pulse Current Wave Form acc. IEC 61000-4-5


Fig. 4 - Typical Clamping Voltage vs. Peak Pulse Current

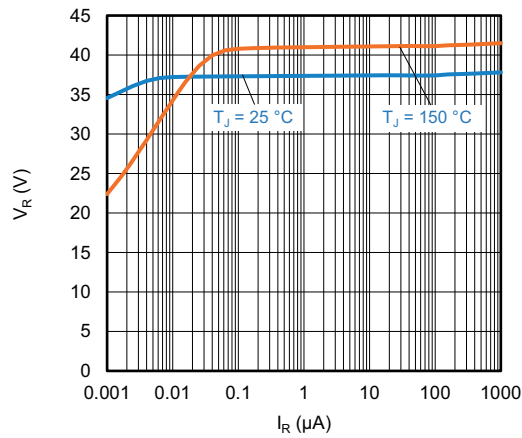


Fig. 5 - Typical Reverse Voltage vs. Reverse Current

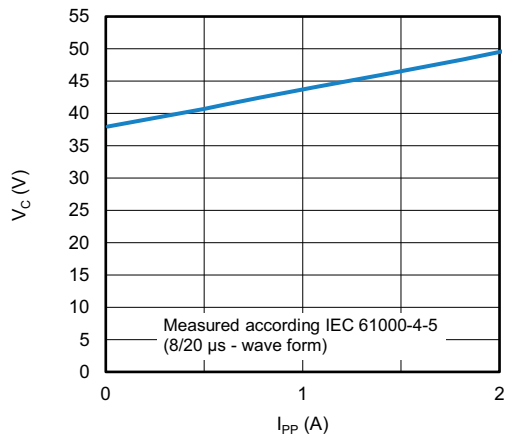
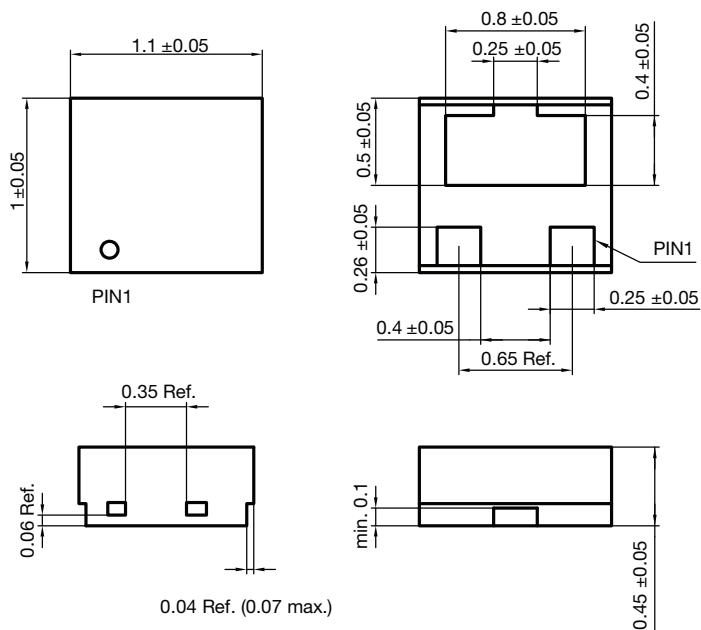
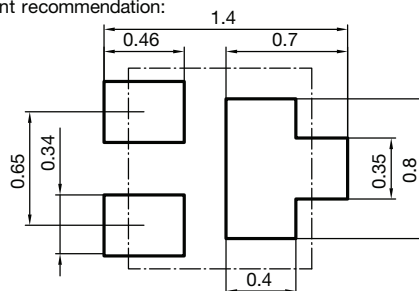


Fig. 6 - Typical Peak Clamping Voltage vs. Peak Pulse Current

PACKAGE DIMENSIONS in millimeters (inches)


foot print recommendation:

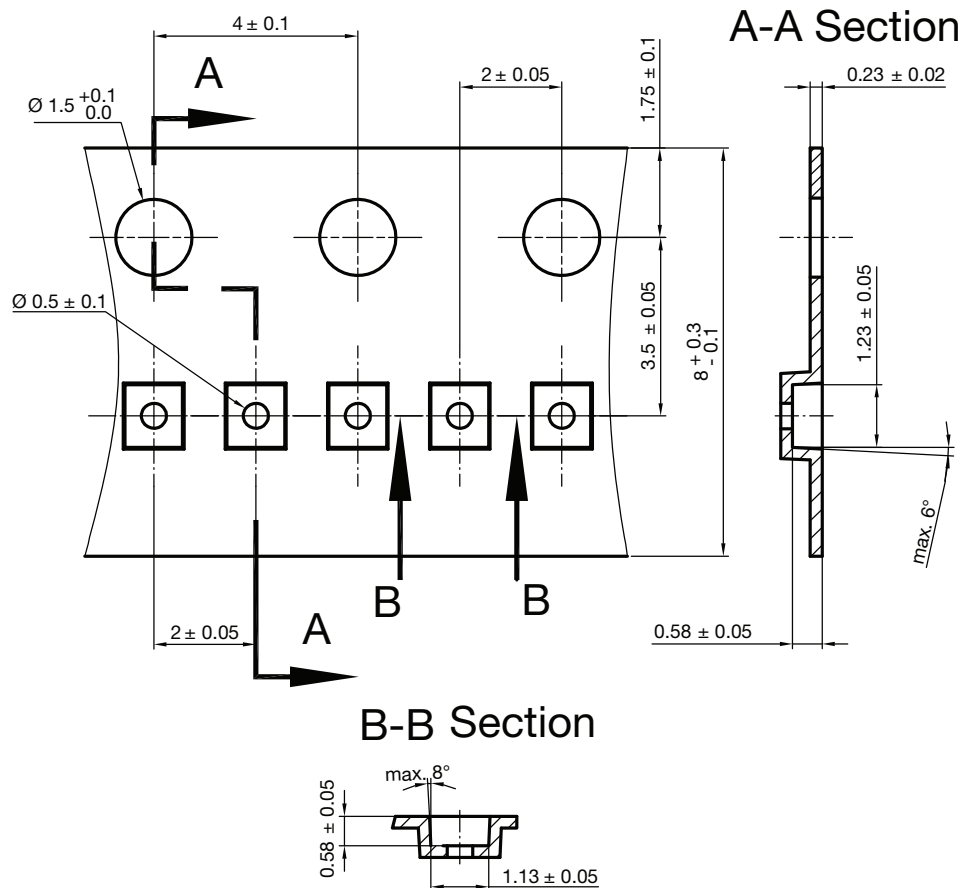


Document no.: S8-V-3906.04-062 (4)

Package name: DFN1110-3A

Created - Date: 04-Apr-2019

CARRIER TAPE DFN1110-3A

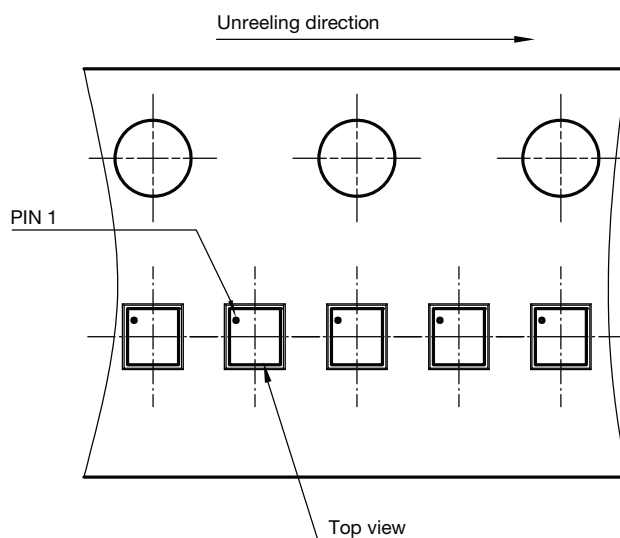


Document no: S8-V-3906.04-065 (4)
Package name: DFN1110-3A
Created date: 28.10.2019

surface resistance: $10^5 - 10^{11} \frac{\text{OHMS}}{\text{SQ}}$

Cummulative tolerances of 10 sprocket holes is ± 0.2 mm

ORIENTATION IN CARRIER TAPE DFN1110-3A



Document no: S8-V-3906.04-066 (4)
Package name: DFN1110-3A
Created date: 28.10.2019



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