PEC2000-54-074NA

AC-DC CRPS Front-End Power Supply

PEC2000-54-074NA is a 2000 Watt, CRPS AC to DC switching power supply module with a +54.5 V single DC output. The power supply operates as a single supply, or N+1 parallel configuration. PEC2000-54-074NA utilizes full digital control architecture for greater efficiency, control and functionality.
This power supply meets international safety standards and displays the CE-Mark for the European Low Voltage Directive (LVD).

Key Features & Benefits

- Input Voltage Range 90 – 136 / 180 – 264 VAC; 180 – 310 VDC
- Single Output Voltage +54.5 VDC
- Output Power up to 2000 W
- Intel Standard CRPS Form Factor
- Dimensions: 185 x 73.5 x 40 mm (7.28 x 2.89 x 1.57 in)
- High Power Density
- UL/CSA 62368-1, EN/IEC 62368-1 Certified
- Supports N+1 Redundancy, Internal ORing
- Clockwise and Counter-Clockwise Fan Rotation
- Supports Power Management Bus Communication Protocol

Applications

- Networking Switches
- Servers & Routers
- Telecommunications

1 ORDERING INFORMATION

PEC	2000	-	54	-	074	N	A
Product Family	**Power Level**	**Dash**	**V1 Output**	**Dash**	**Width**	**Airflow**	**Input**
PEC Front-Ends	2000 W		54.5 V		73.5 mm	N: Normal	A: AC

2 INPUT

PARAMETER	DESCRIPTION / CONDITION	MIN	NOM	MAX	UNIT
Input Voltage Ranges	Low Line Voltage AC Range (1000 W)	90	100-127	136	V_{RMS}
	Start-up (V_{BROWN_IN})	85		90	VAC
	Power Off (V_{BROWN_OUT})	75		85	VAC
	High Line Voltage AC Range (2000 W)	180	200-240	264	V_{RMS}
	HVDC (2000 W)	180	240	310	VDC
	Start-up (V_{BROWN_IN})	170		180	VDC
	Power Off (V_{BROWN_OUT})	160		170	VDC
Input Current	AC Low Line			13	A_{RMS}
	AC High Line			10	
	HVDC		10		
AC Line Inrush Current	for up to 1/4 of the AC cycle			55	A_{pk}
Input Frequency		47	50/60	63	Hz
Power Factor	230 VAC and 115 VAC / 50/60 Hz, 20% load	0.75			
	230 VAC and 115 VAC / 50/60 Hz, 50% load	0.90			
	230 VAC and 115 VAC / 50/60 Hz, 100% load	0.97			
Efficiency	230 VAC / 50 Hz, 20% load	90			%
	230 VAC / 50 Hz, 50% load	94			%
	230 VAC / 50 Hz, 100% load	91			%
Hold-up Time	80% of rated load	12			ms
AC Line Sag	0 to 1/2 AC cycle (nom AC voltage ranges, 50/60 Hz) No loss of function or performance.		95		%
	> 1 AC cycle (nom AC voltage ranges, 50/60 Hz) Loss of function acceptable, self-recoverable (0 ~ 50% load)	30			%
AC Line Surge	Continuous (nom AC voltage ranges, 50/60 Hz) No loss of function or performance		10		%
	0 to 1/2 AC cycle (mid-point of nom VAC ranges, 50/60 Hz) No loss of function or performance		30		%
AC Line Isolation	Primary to secondary; reinforced insulation per IEC 62368-1	3000 4242			VAC VDC

Notes: The Brown IN/OUT Hysteresis min is 3 VAC.
1. Maximum input current at low input voltage range shall be measured at 90 VAC, at max load.
2. Maximum input current at high input voltage range shall be measured at 180 VAC, at max load.
3.This requirement is not to be used for determining agency input current markings.

3 OUTPUT

PARAMETER	DESCRIPTION / CONDITION	MIN	NOM	MAX	UNIT
Output Voltage [1]			54.5		VDC
Voltage Regulation Limits	± 3 % tolerance	+52.865	+54.5	+56.135	V_{RMS}
Max Continuous Output Power	Low line: 1000 W			2000	W
Output Current	@ 90 – 136 VAC @ 180 – 220 VAC / 180 – 220 VDC (see power derating curve 1) @ 220 – 264 VAC / 220 – 310 VDC (see power derating curve 2)	0 0 0		18.35 29.36 36.70	A
Transient Load	Δ Step Load Size, 60% of max. load, 1000 µF			0.5	A/µs
Dynamic Load	@ +54.5 V min loading is 10% of max load Voltage regulation limit tolerance ± 5 %	+51.775	+54.5	+57.225	V_{RMS}
Capacitive Loading	@ +54.5 V	100		3000	µF
Ripple & Noise	10 Hz to 20 MHz BW @ +54.5 V			540	mVpp
Line Regulation	@ +54.5 V		±1		%
Load Regulation	@ +54.5 V		± 3		%
Hot-swap	Available				

[1] +54.5 V main output voltage should be adjusted to 54.5 ± 0.3 V at 18.35 A load

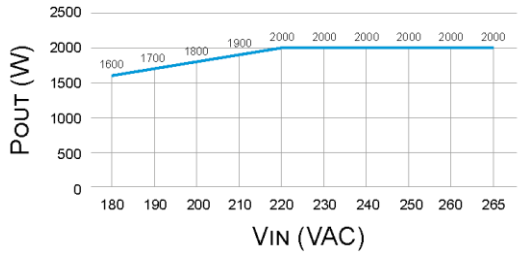


Figure 1. Power Derating Curve 1

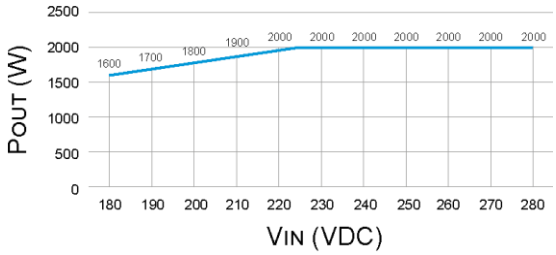


Figure 2. Power Derating Curve 2

3.1 FORCED LOAD SHARING

The +54.5 V output has active load sharing. The output will share within 5% at full load. The failure of a power supply should not affect the load sharing or output voltages of the other supplies still operating. The supplies must be able to load share in parallel and operate in a hot-swap / redundant 1+1 configurations.
The VLS pins are connected together at user system board for load sharing function of two or more units.

The Ishare voltage (+54.5V VIBUS) corresponding to 100% load is 8 V.
10% - 24% of Rated load of single power supply, current sharing accuracy has to be ± 15%
25% - 50% of Rated load of single power supply, current sharing accuracy has to be ± 10%
51% - 100% of Rated load of single power supply, current sharing accuracy has to be ± 5%

NOTE: Current sharing has to meet following accuracy at different load range running in 1+1 configuration.
In N+1 configuration total load current should be multiplication N times total rated output current of single supply.

3.2 TIMING

These are the timing requirements for the power supply operation. The output voltages must rise from 10% to within regulation limits (Tvout_rise) within 2 to 70 ms. All outputs must rise monotonically. The table below shows the timing requirements for the power supply being turned on and off via the AC input, with PSON held low and the PSON signal, with the AC input applied.

ITEM	DESCRIPTION	MIN	MAX
Tvout_rise	Output voltage rise time	2.0	70
TAC_ON Delay	Delay from AC being applied to all output voltages being within regulation. (Vin:100~240Vac)	-	3000
TVout_Holdup	Time +54.5V output voltage stays within regulation after loss of AC at 80% load. (fall to 46Vdc)	13	-
TPW_OK Holdup	Delay from loss of AC to de-assertion of PW_OK	12	-
TPS_ON# delay	Delay from PS_ON# active to output voltages within regulation limits.	5	400
TPS_ON#_PW_OK	Delay from PS_ON# deactivate to PW_OK being de-asserted.	-	5
TPW_OK On	Delay from output voltages within regulation limits to PW_OK asserted at turn on.	100	500
TPW_OK Off	Delay from PW_OK de-asserted to output voltages dropping out of regulation limits.	1	-
TPW_OK Low	Duration of PW_OK being in the de-asserted state during an off/on cycle using AC or the PSON signal.	100	-
TAC_OK On	Delay from AC input on to ACOK signal goes high	1	-
TAC_OK Off	Delay from AC input off to ACOK signal goes low , psu with at least 20% load	-	10

Units in ms.

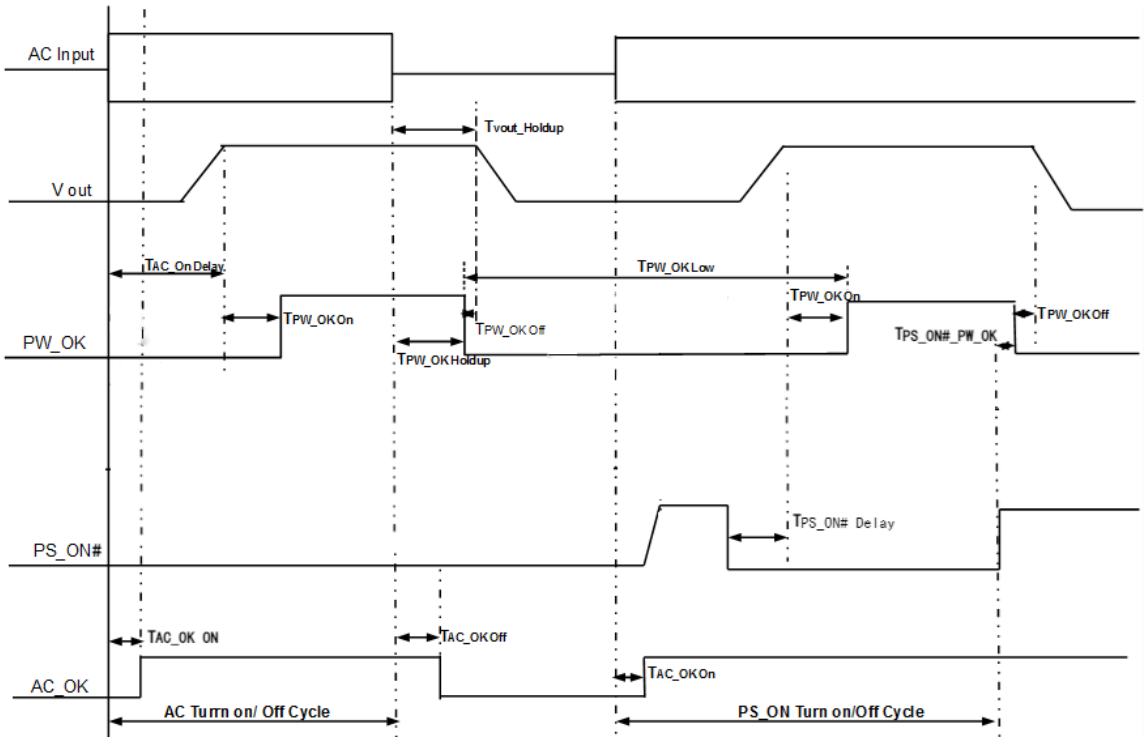


Figure 3. Turn On/Off Timing (Power Supply Signals)

4 PROTECTIONS

4.1 CURRENT LIMIT (OCP)

The power supply has a current limit to prevent the outputs from exceeding the values shown in the table below. If the current limits are exceeded the power supply shuts down, the power supply will not be damaged from repeated power cycling in this condition.

OUTPUT	INPUT VOLTAGE RANGE	OVER CURRENT LIMITS
+54.5 V	90 – 136 VAC	20.2 - 27.5 A
+54.5 V	180 – 264 VAC	40.3 – 55.0 A

4.2 OVER VOLTAGE PROTECTION (OVP)

The power supply will shut down and latch off after an over voltage condition occurs. This latch will be cleared by toggling the PS_ON# signal or by an AC power interruption. The values are measured at the output of the power supply's connectors. The voltage shall never trip any lower than the minimum levels when measured at the power connector.

OUTPUT	MIN	MAX
+54.5 V	57.3 V	60 V

4.3 OVER TEMPERATURE PROTECTION (OTP)

The power supply is protected against over temperature conditions caused by loss of fan cooling or excessive ambient temperature. In an OTP condition the PSU will shut down. When the power supply temperature drops to within specified limits, the power supply will restore power automatically, while the VSSO remains always on. The OTP circuit must have built in margin such that the power supply will not oscillate on and off due to temperature recovering condition. The OTP trip level has a minimum of 4 °C of ambient temperature margin.

4.4 SHORT CIRCUIT PROTECTION (SCP)

Short circuit of the power supply output will not result in fire hazard, shock hazard, or damage to the power supply. The power supply will shut down after an over current condition occurs. After PSU shut down the main output will auto recover.

5 CONTROL AND INDICATOR FUNCTIONS

The following sections define the input and output signals from the power supply. Signals that can be defined as low true use the following convention: Signal# = low true

Periodic and Random Deviation ripple / noise must be less than 260 mV in Output Signal, “PW_OK”, “AC_OK” and “PS-ALERT” at all specified input voltage condition, all specified output loading and any operating environmental requirements.

5.1 AC_OK (S2)

Each module has two LED status indicators on the front panel. The AC at 90 VAC – 264 VAC, AC_OK (S2) is high. So, when the AC is below 90 VAC AC_OK (S2) is low.

The AC_OK has not done (shutdown or abnormal power down) can notify the system early.

SIGNAL TYPE	PARAMETER
Logic level low voltage	0 V ~ 0.4 V
Logic level high voltage	2.1 V ~ 3.46 V
Sink current	400 µA (Max)
Source current	4 mA (Max)

Table 1. AC_OK Signal Characteristics

5.2 PS_ALERT SIGNAL (S4)

This signal indicates that the power supply is experiencing a problem that the user should investigate. This needs to be asserted due to Critical events or Warning events. The signal is activated if critical component temperature reached a warning threshold, general failure, over-current, over-voltage, failed fan. This signal may also indicate the power supply is reaching its end of life or is operating in an environment exceeding the specified limits. This signal is to be asserted in parallel with LED turning solid Amber or blink Amber.

SIGNAL TYPE (ACTIVE HIGH)	PULL-UP TO 3.3 VSB LOCATED IN PSU	
PS_ALERT = High	OK	
PS_ALERT = Low	Power Alert to system	
	MIN	MAX
Logic level low voltage	0 V	0.4 V
Logic level high voltage	2.1 V	3.46 V
Source current	-	4 mA
Sink current	-	400 µA

Table 2. PS_ALERT Signal Characteristics

5.3 SDA & SCL SIGNAL (S5 / S6)

SDA and SCL signals are used for communication with user system. The Power Management Bus operation frequency is 100 kHz.
Inner parameters:

1. Inner Pulled up Resistor to internal 3.3 V = 10 kohm / 0603.
2. Inner Filter capacitor = 100 pF
3. Inner serial Resistor (Rs) = 100 ohm / 0603.

Note: The manufacturer reserves the right to change inner parameters for matching user system.

SIGNAL TYPE	I2C CONFIGURATION
Logic level low voltage	0 V ~ 0.4 V
Logic level high voltage	2.0 V ~ 3.46 V
Sink current	1 mA
Source current	0.5 mA
Signal rise and fall time	Risetime: 1000 ns, Fall time: 300 ns

Table 3. SDA / SCL Signal Characteristics

5.4 PS_KILL# INPUT SIGNAL (S7)

PS_KILL# signal is required to remotely turn on/off the power supply unit.
If PS_KILL# signal is LOW, it means that +54.5 V is turned on.
If PS_KILL# signal is pulled HIGH, it means that +54.5 V is turned off.

Signal Type	Accepts an open collector/drain input from the system. Pull-up to 3.3VSB located in power supply.	
PS_KILL# = Low	ON	
PS_KILL# = High or Open	OFF	
	MIN	MAX
Logic level low (power supply ON)	0 V	0.4 V
Logic level high (power supply OFF)	2.1 V	3.46 V
Source current, VPS_KILL# = high	-	0.5 mA

Table 4. PS_KILL# Signal Characteristics

5.5 PS_ON# INPUT SIGNAL (S8)

The PS_ON# signal is required to remotely turn on/off the power supply. PS_ON# is an active low signal that turns on the +54.5 V power rail. When this signal is not pulled low by the system, or left open, the outputs (except the VSSO) turn off. This signal is pulled to a Standby voltage by a pull-up resistor internal to the power supply.

Signal Type	Accepts an open collector/drain input from the system. Pull-up to 3.3VSB located in power supply.	
PS_ON# = Low	ON	
PS_ON# = High or Open	OFF	
	MIN	MAX
Logic level low (power supply ON)	0 V	0.4 V
Logic level high (power supply OFF)	2.1 V	3.46 V
Source current, VPS_ON# = high	-	0.5 mA

Table 5. PS_ON# Signal Characteristics

5.6 PW_OK (POWER OK) OUTPUT SIGNAL (S9)

PW_OK is a power OK signal and will be pulled high by the power supply to indicate that all the outputs are within the regulation limits of the power supply. When any output voltage falls below regulation limits or when AC power has been removed for a time sufficiently long so that power supply operation is no longer guaranteed, PW_OK will be de-asserted to a LOW state.

See table for a representation of the timing characteristics of PW_OK.
The start of the PW_OK delay time is inhibited as long as any power supply output is in current limit.

Signal Type	Open collector/drain output from power supply.	
PW_OK = High	Power OK	
PW_OK = Low	Power Not OK	
	MIN	MAX
Logic level low voltage	0 V	0.4 V
Logic level high voltage	2.1 V	3.46 V
Sink current	-	400 µA
Source current	-	4 mA

Table 6. PW_OK Signal Characteristics

5.7 POWER MANAGEMENT BUS ADDRESS SIGNALS (S10 / S15)

User system use "PS_A0 (S15) / PS_ A1 (S10)" to allocate address of power supply unit in particular slot location for Power Management Bus communication.

Note: This signal has internal pull high resistor to inner 3.3 V. The address of power supply unit must be set by user system for Power Management Bus communication reliability.

Signal Type	Input pin, No inner pull-high / Low Resistor	
PS_A0 / PS_A1 = High	Address 1	
PS_A0 / PS_A1 = Low	Address 0	
	MIN	MAX
Logic level low voltage	0 V	0.4 V
Logic level high voltage	2.1 V	3.46 V
Source current	-	0.5 mA

Table 7. PS_A0/PS_A1 Signal Characteristics

5.8 PS_ PRESENT# SIGNAL (S14)

PS_PRESENT# signal is used to indicate that the power supply unit presence in user system.

When power supply unit is present in card-edge receptacle, the PS_PRESENT# signal is in LOW level. (This signal is connected to inner RTN by an internal 100 ohm / 0805 resistor. In user system, this signal must be pulled up to outside 3.3 V an external 4.7 kohm pull-up resistor.)

Signal Type	Input pin, No inner pull-high / Low Resistor
PS_PRESENT# = Low	PSU is Present
PS_PRESENT# = High	PSU is not Present

Table 8. PS_Present# Signal Characteristics

5.9 VSSO SIGNAL (S17)

Each module provides +12 V auxiliary power for micro controller Vdd device of redundant power supply. VSSO pins should be linked together and closer.

Signal Type	Power
System minimum requirement	12 V / 1 A (max)

Table 9. VSSO Signal Characteristics

5.10 EEPROM-WP SIGNAL (S18)

PSU write the EEPROM data only using, pull down this pin at PDB.

6 ELECTROMAGNETIC COMPATIBILITY

6.1 IMMUNITY

The power supply complies with the limits defined in EN 55024.

PARAMETER	DESCRIPTION / CONDITION	CRITERION
Electrostatic Discharge	IEC / EN 61000-4-2	
Radiated Immunity	IEC / EN 61000-4-3	
Fast Transient / Burst	IEC / EN 61000-4-4	
Surge Immunity	IEC / EN 61000-4-5	
Conducted Susceptibility	IEC / EN 61000-4-6	
Power Frequency Magnetic Immunity	IEC / EN 61000-4-8	
Voltage Dips and Interruptions	IEC / EN 61000-4-11	

6.2 EMISSION

PARAMETER	DESCRIPTION / CONDITION	CRITERION
Conducted & Radiated Emissions	EN 55032 / CISPR32	Class A 6 dB margin
Power Harmonics	EN 61000-3-2	Class A
Voltage Fluctuation and Flicker	EN 61000-3-3	Class A

7 ENVIRONMENTAL

PARAMETER	DESCRIPTION / CONDITION	MIN	NOM	MAX	UNIT
Ambient Temperature	Operating	-5		+50	°C
	Non-Operating (max. rate of change of 20°C/h)	-40		+70	
Humidity	Operating, relative (non-condensing)	5		90	%
	Non-Operating, relative (non-condensing)	5		95	
Altitude	Operating			5 000	m
	Non-Operating			15 200	m
Mechanical Shock (non-operating)	50 G Trapezoidal Wave, Velocity change = 170 in. / sec				
Vibration (non-operating)	**Sine sweep:** 5 Hz to 200 Hz @ 1 g_{RMS} at 1 octave/min; dwell 15 min at each of 3 resonant points **Random:** 5 Hz @ 0.0 1g^2/Hz to 20 Hz @ 0.02 g^2/Hz (slope up); 20 Hz to 500 Hz @ 0.02 g^2/Hz (flat); Input acceleration = 3.13 g_{RMS}; 10 min. per axis for 3 axis on all samples				
Thermal Shock (non-operating)	50 cycles, 30°C/min ≥ transition time ≤ 15°C/min, Duration of exposure to temperature extremes for each 1/2 cycle = 30 min	-40		+70	°C
Audible Noise	@ T_A = 25°C / @ T_A = 50°C			60 / 70	dB

8 SAFETY / APPROVALS

PARAMETER	DESCRIPTION / CONDITION	STATUS
Agency Approvals	• UL / CSA 62368-1 (USA / Canada) • EN / IEC 62368-1 (Europe / International) • CB Certificate & Report, IEC 62368-1 (Report includes all country national deviations)) • CE – Low Voltage Directive 2006/95/EC (Europe) • Nordics – EMKO-TSE (74-SEC) 207/94 • GB4943.1 – CNCA Certification (China)	
Leakage Current	< 1.6 mA @ 1+1 redundant, 250 VAC, 60 Hz	

9 RELIABILITY

PARAMETER	DESCRIPTION / CONDITION	MIN	NOM	MAX	UNIT
MTBF	@ T_A = 25°C, 100% load	200			kh

10 MECHANICAL

PARAMETER	DESCRIPTION / CONDITION	MIN	NOM	MAX	UNIT
Dimensions (W x H x L)			39.8 x 73 x 185		mm in
Weight			TBD		g

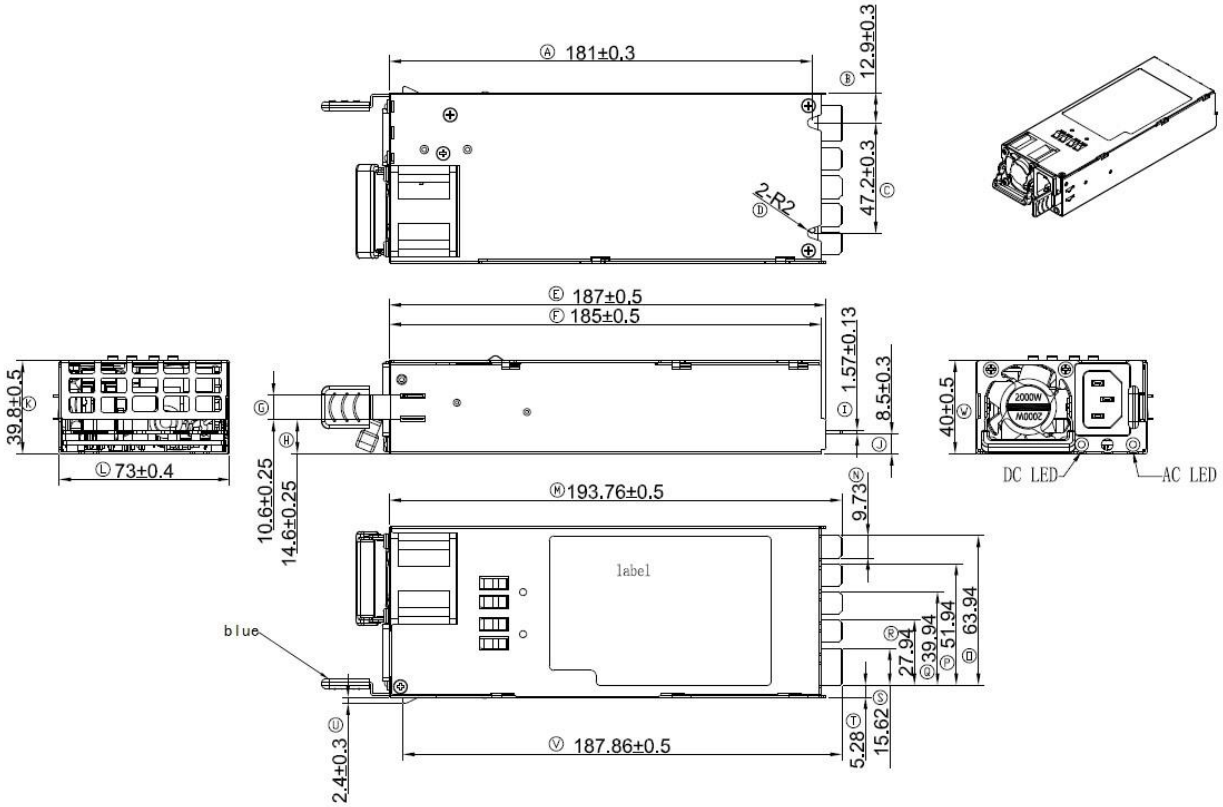


Figure 4. Mechanical Drawing

10.1 HANDLE RETENTION

The power supply has a handle to assist extraction. The module can be inserted and extracted without the assistance of tools. The power supply has a latch which retains the power supply into the system and prevents the power supply from being inserted or extracted from the system when the AC power cord is pulled into the power supply.
The handle protects the operator from any burn hazard through the use of the Customer Corporation Industrial designed plastic handle.

10.2 LED MARKING AND IDENTIFICATION

The power supply has two bi-colored LEDs for indication of the power supply status.
The LED is driven by an internal circuitry and should even illuminate in an 1+1 configuration even without AC power.

POWER SUPPLY CONDITION	LED STATUS	
PSU STATUS	**DC OK (left side)**	**AC OK (right side)**
AC present /Only VSSO on	Green / 0.5 Hz flashing	Green
Power supply DC outputs on and OK	Green	Green
Power supply failure, PSU shut down [1]	Red	Green
AC no present	Green	Red / 0.5 Hz flashing
AC loss	Green	Red / 0.5 Hz flashing

[1] Power supply DC fail : OCP, OVP, OTP, FAN

11 CONNECTORS

11.1 AC INPUT CONNECTOR

The AC input connector shall be an IEC 320 C-14/C-16 power inlet.

11.2 DC OUTPUT CONNECTOR PIN LOCATIONS

The power supply uses a card edge output connection for power and signal that is compatible with a 12x2 + 4x2 Power Card Edge connector (equivalent to 12 x 2 + 4 x 2 pin configuration of the OUPIN PN 9392-4SP08S24N12CB30DT-U545 (24 signal)).

BACK SIDE				TOP SIDE			
PIN	SIGNAL NAME	FUNCTION	H/L SIDE	PIN	SIGNAL NAME	FUNCTION	H/L SIDE
P1	SGND	Ground for signal using only	L	P5	SGND	Ground for signal using only	L
P2	NC	NC without gold finger	-	P6	NC	NC without gold finger	-
P3	+54.5V_VRTN	+54.5V return	H	P7	+54.5V_VRTN	+54.5V return	H
P4	+54.5V	+54.5V main output	H	P8	+54.5V	+54.5V main output	H
S1	NC	NC without gold finger	-	S13	NC	NC without gold finger	-
S2	AC_OK	AC good signal output	L	S14	PS_PRESENT#	Power supply present	L
S3	NC	NC without gold finger	-	S15	PS_A0	2C address bit 0	L
S4	PS_ALERT	Power supply Alert to system	L	S16	NC	NC without gold finger	-
S5	SDA	I2C serial data	L	S17	VSSO	+12V auxiliary power output with ORing-diode	L
S6	SCL	I2C serial clock	L	S18	EEPROM-WP	PSU write the EEPROM data only using	L
S7	PS_KILL#	For PSU hot swap signal	L	S19	NC	NC without gold finger	-
S8	PS_ON#	Power enable input signal	L	S20	NC	NC with gold finger	L
S9	PW_OK	Power good signal output	L	S21	NC	Isolation pin, without gold finger	-
S10	PS_A1	I2C address bit 1	L	S22	NC	Isolation pin, without gold finger	-
S11	NC	Isolation pin, without gold finger	-	S23	NC	Isolation pin, without gold finger	-
S12	NC	Isolation pin, without gold finger	-	S24	+54.5V VIBUS	+54.5V main output current share bus	H

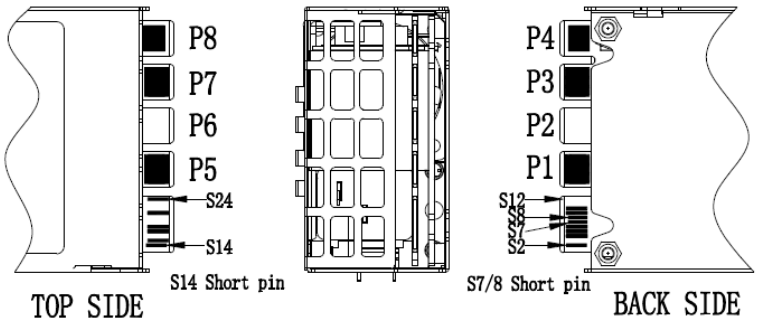


Figure 5. DC Output Connector

12 POWER MANAGEMENT BUS

12.1 OVERVIEW

The Power Management Bus features included in this specification are requirements for ac/dc golden box power supply for use in server systems. This specification is based on the Power Management Bus™ specifications parts I and II, revision 1.2.

12.2 RELATED DOCUMENTS

Power Management Bus Power System Management Protocol Specification Part I – General Requirements, Transport and Electrical Interface; Revision 1.2. Power Management Bus Power System Management Protocol Specification Part II – Command Language; Revision 1.2. SMBus 2.0.

12.3 HARDWARE

12.3.1 OVERVIEW

The device in the power supply shall be compatible with both SMBus 2.0 'high power' specification for I2C Vdd based power and drive (for Vdd = 3.3V). This bus shall operate at 3.3V.

12.3.2 POWER MANAGEMENT BUS POWER SOURCING

The circuits inside the power supply shall derive their power from the standby output. For redundant power supplies the device(s) shall be powered from the system side of the or'ing device. The Power Management Bus device shall be on whenever AC power is applied to the power supply or a parallel redundant power supply in the system.

12.3.3 PULL UPS

Only weak pull-up resistors shall be on SCL or SDA inside the power supply. The main pull-up resistors are provided by the system and may be connected to 3.3Vsb. For the system design, the main pull-ups shall be located external to the power supply and derive their power from the standby rail.

12.3.4 DATA SPEED

The POWER MANAGEMENT BUS device in the power supply shall operate at the full 100 kbps SMBus speed and avoid using clock stretching that can slow down the bus. For example, the power supply can clock stretch while parsing a command or a power supply servicing multiple internal interrupts or NACK may require some use of clock stretching.

The Power Management Bus device shall support SMBus cumulative clock low extend time (Tlow:sext) if < 25msec. This requires the device to extend the clock time no more than 25msec between START and STOP for any given message.

12.4 ACCURACY

The sensor commands shall meet the following accuracy requirements.
The accuracies shall be met over the specified ambient temperature and the full range of rated input voltage.

Output Loading	10% - 20%	> 20% - 50%	> 50% -100%
READ_VIN		+/-5%	
READ_PIN	+/-10%	+/-8%	+/-5%
READ_VOUT		+/- 5%	
READ_IOUT	+/-10%	+/-5%	+/-5%
READ_TEMPERATURE		+/- 5℃	

Table 10. Required Accuracy

12.5 POWER MANAGEMENT BUS COMMAND SET

Via the Power Management Bus the computer system can communicate with the power supply to access currents, voltages, fan control and speed and temperatures. As soon as AC Power is connected to the PSU the Power Management Bus functionality must be available.
Following Table shows mandatory Power Management Bus commands to be supported by the PSU

Command Code	Command Name	SMBus Transaction Type:		Number Of Data Bytes	Comment
		Writing Data	Reading Data		
00h	PAGE	Write Byte	Read Byte	1	
01h	OPERATION	Write Byte	Read Byte	1	0x80 ON; 0x00 OFF Default: 0x80
02h	ON_OFF_CONFIG	Write Byte	Read Byte	1	0x1D
03h	CLEAR_FAULTS	Send Byte	N/A	0	
05h	PAGE_PLUS_WRITE	Block Write	N/A	Variable	
06h	PAGE_PLUS_READ	N/A	Block Write – Block Read	Variable	
19h	CAPABILITY	N/A	Read Byte	1	0xB0
1Ah	QUERY	N/A	Block Write – Block Read	1	
1Bh	PS_ALERT_MASK	Write Word	Block Write – Block Read	2	
20h	VOUT_MODE		Read Byte	1	0x17 (n=-9)
21h	VOUT_COMMAND	Write Word	Read Word	2	
30h	COEFFICIENTS	N/A	Block Write – Block Read	5	Use for Ein/Eout
31h	POUT_MAX	N/A	Read Word	2	
3Ah	FAN_CONFIG_1_2	Write Byte	Read Byte	1	Default is Duty
3Bh	FAN_COMMAND_1	Write Word	Read Word	2	
4Ah	IOUT_OC_WARN_LIMIT		Read Word	2	
51h	OT_WARN_LIMIT		Read Word	2	
5Dh	IIN_OC_WARN_LIMIT		Read Word	2	
6Ah	POUT_OP_WARN_LIMIT		Read Word	2	
6Bh	PIN_OP_WARN_LIMIT		Read Word	2	
78h	STATUS_BYTE	Write Byte	Read Byte	1	
Bit 6	OFF				
Bit 5	VOUT_OV_FAULT				
Bit 4	IOUT_OC				
Bit 3	VIN_UV				
Bit 2	TEMPERATURE				
Bit 1	CML				
Bit 0	NON OF THE ABOVE				
79h	STATUS_WORD	Write Word	Read Word	2	
Bit 7(H)	VOUT				
Bit 6	IOUT/POUT				
Bit 5	INPUT				
Bit 3	POWER_GOOD#				
Bit 2	FANS				
Bit 6(L)	OFF				
Bit 5	VOUT_OV_FAULT				
Bit 4	IOUT_OC_FAULT				
Bit 3	VIN_UV_FAULT				
Bit 2	TEMPERATURE				
Bit 1	CML				
Bit 0	NON OF THE ABOVE				
7Ah	STATUS_VOUT	Write Byte	Read Byte	1	
Bit 7	VOUT_OV_FAULT				

Bit 4	VOUT_UV_FAULT				
7Bh	STATUS_IOUT	Write Byte	Read Byte	1	
Bit 7	Iout OC fault				
Bit 5	Iout OC warning				
Bit 1	Pout OP fault				
Bit 0	Pout OP warning				
7Ch	STATUS_INPUT	Write Byte	Read Byte	1	
Bit 5	Vin UV warning				
Bit 4	Vin UV fault				
Bit 3	Unit off for insufficient input				
Bit 1	Iin over current warning				
Bit 0	Pin over power warning				
7Dh	STATUS_TEMPERATURE	Write Byte	Read Byte	1	
Bit 7	OT fault				
Bit 6	OT warning				
7Eh	STATUS_CML	Write Byte	Read Byte	1	
Bit 7	Invalid COMMAND				
Bit 6	Invalid DATA				
Bit 5	PEC Failed				
81h	STATUS_FANS_1_2	Write Byte	Read Byte	1	
Bit 7	Fan 1 fault				
Bit 5	Fan 1 warning				
Bit 3	Fan1 speed overridden				
86h	READ_EIN	N/A	Block Read	6	DIRECT Data Format
87h	READ_EOUT	N/A	Block Read	6	DIRECT Data Format
88h	READ_VIN	N/A	Read Word	2	Linear
89h	READ_IIN	N/A	Read Word	2	Linear
8Bh	READ_VOUT	N/A	Read Word	2	Linear16
8Ch	READ_IOUT	N/A	Read Word	2	Linear
8Dh	READ_TEMPERATURE_1	N/A	Read Word	2	Ambient
8Eh	READ_TEMPERATURE_2	N/A	Read Word	2	SR Hotspot
8Fh	READ_TEMPERATURE_3	N/A	Read Word	2	PFC Hotspot
90h	READ_FAN_SPEED_1	N/A	Read Word	2	In RPM
96h	READ_POUT	N/A	Read Word	2	Linear
97h	READ_PIN	N/A	Read Word	2	Linear
98h	POWER MANAGEMENT BUS_REVISION	N/A	Read Byte	1	1.2
99h	MFR_ID	Block Write	Block Read	Variable (3)	“bel”
9Ah	MFR_MODEL	Block Write	Block Read	Variable (16)	“PEC2000-54-074NA”
9Bh	MFR_REVISION	Block Write	Block Read	Variable (3)	"VXX"
9Ch	MFR_LOCATION	Block Write	Block Read	Variable (8)	"DONGGUAN"
9Dh	MFR_DATE	Block Write	Block Read	Variable (8)	"YYYYMMDD"
9Eh	MFR_SERIAL	Block Write	Block Read	Variable (19)	Serial Number
9Fh	APP_PROFILE_SUPPORT	N/A	Block Read	Variable (2)	Power Management Bus 1.2
A0h	MFR_VIN_MIN	N/A	Read Word	2	90V
A1h	MFR_VIN_MAX	N/A	Read Word	2	264V
A2h	MFR_IIN_MAX	N/A	Read Word	2	13.0A
A3h	MFR_PIN_MAX	N/A	Read Word	2	2500W
A4h	MFR_VOUT_MIN	N/A	Read Word	2	51.77V
A5h	MFR_VOUT_MAX	N/A	Read Word	2	57.22V
A6h	MFR_IOUT_MAX	N/A	Read Word	2	36.7A
A7h	MFR_POUT_MAX	N/A	Read Word	2	2000W
A8h	MFR_TAMBIENT_MAX	N/A	Read Word	2	50℃
A9h	MFR_TAMBIENT_MIN	N/A	Read Word	2	-5℃

AAh	MFR_EFFICIENCY_LL	N/A	Block Read	14	At 20%/50%/100%
ABh	MFR_EFFICIENCY_HL	N/A	Block Read	14	At 20%/50%/100%
C0h	MFR_MAX_TEMP_1	N/A	Read Word	2	
C1h	MFR_MAX_TEMP_2	N/A	Read Word	2	
C2h	MFR_MAX_TEMP_3	N/A	Read Word	2	
D4h	MFR_HW_COMPATIBILITY	N/A	Read Word	2	
D5h	MFR_FWUPLOAD_CAPABILITY	N/A	Read Byte	1	
D6h	MFR_FWUPLOAD_MODE	Write Byte	Read Byte	1	
D7h	MFR_FWUPLOAD	Block Write	N/A		
D8h	MFR_FWUPLOAD_STATUS	N/A	Read Word	21	
D9h	MFR_FW_REVISION	N/A	Block Read	3	

Note: Write protocol must include PEC (Packet Error Checking).

Table 11. Supported Power Management Bus Command Set

12.6 STATUS COMMANDS

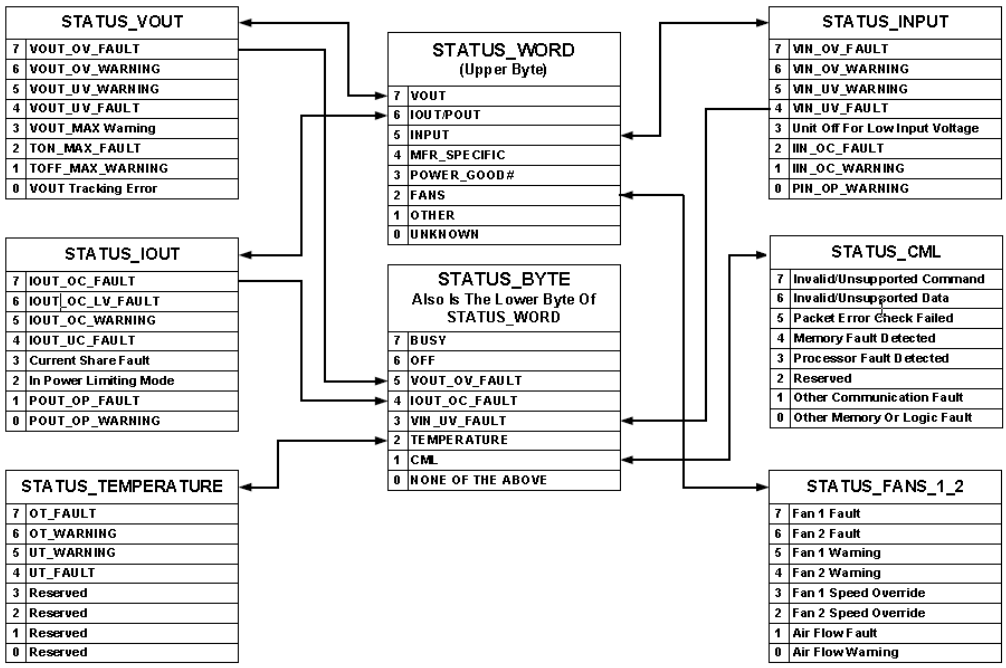


Figure 6. Summary Of The Status Registers

The following Power Management Bus STATUS commands shall be supported. All STATUS commands stated in Table Supporting PAGE instances shall support the PAGE_PLUS_WRITE and PAGE_PLUS_READ commands since they are used by both the BMC and ME. The BMC and ME refer to the two instances of the commands accessed via the PAGE_PLUS_WRITE and PAGE_ PLUS_READ commands. The status bits shall assert whenever the event driving the status bit is present. Once a bit is asserted it shall stay asserted until cleared

The STATUS commands that are supported with the PAGE_PLUS_READ and PAGE_PLUS_W RITE commands shall still support direct access of the base STATUS_XXX commands using the read word, write word, read byte, and write byte protocols.

STATUS_FAN_1_2 command is only accessed by the system BMC. It uses the standard read byte protocol to read status and write byte protocol to clear bits.

The STATUS events are also used to control the PS_ALERT signal. The new PS_ALERT_MASK command is used to define which status event control the PS_ALERT signal. Default values for these mask bits are shown in the table below.

Power Management Bus	Bit location	PSU state when bit	Instances	PS_ALERT_MASK defaults for each of the

command		is asserted ('1')	No PAGE'ing [2] PAGE 00h = BMC PAGE 01h = ME	three instances (No PAGE, PAGE 00h, PAGE 01h) 0 = causes assertion of PS_ALERT 1 = does not cause assertion of PS_ALERT
STATUS_WORD			No PAGE, 00h, 01h	
OFF	6 (lower)	OFF		NA
IOUT_OC_FAULT	4 (lower)	Refer to STATUS_IOUT		NA
VIN_UV_FAULT	3 (lower)	Refer to STATUS_INPUT		NA
TEMPERATURE	2 (lower)	Refer to STATUS_TEMPERATURE		NA
CML	1 (lower)	ON		NA
VOUT	7 (upper)	Refer to STATUS_VOUT		NA
IOUT/POUT	6 (upper)	Refer to STATUS_IOUT		NA
INPUT	5 (upper)	Refer to STATUS_INPUT		NA
FANS	2 (upper)	Refer to STATUS_FANS		NA
STATUS_VOUT			No PAGE'ing	
VOUT_OV_FAULT	7	OFF		1, 1, 1
VOUT_UV_FAULT	4	OFF		1, 1, 1
STATUS_IOUT			No PAGE'ing, 00h,01h	
IOUT_OC_FAULT	7	OFF		1, 1, 1
IOUT_OC_WARNING	5	ON		1, 1, 0
POUT_OP_FAULT	1	OFF		1, 1, 1
POUT_OP_WARNING	0	ON		1, 1, 1
STATUS_INPUT			No PAGE'ing, 00h,01h	
VIN_UV_WARNING	5	ON		1, 1, 1
VIN_UV_FAULT 1	4	OFF		1, 1, 0
Unit off for low input voltage	3	OFF		1, 1, 1
IIN_OC_WARNING	1	ON		1, 1, 1
PIN_OP_WARNING	0	ON		1, 1, 1
STATUS_TEMPERATURE			No PAGE'ing, 00h,01h	
OT_FAULT	7	OFF		1, 1,1
OT_WARNING	6	ON		1, 1, 0
STATUS_FANS_1_2			No PAGE'ing	
Fan 1 fault 3	7	OFF		1, 1, 1
Fan 1 warning 3	5	ON		1, 1, 1

Table 12. Power Management Bus Status Commands Summary

1 The Vin Fault bit in STATUS_INPUT shall get asserted if the input power has dropped below the PSU's operating range for any duration of time; even if the PSU continues to operate normally through a momentary input dropout event.
2 'No PAGE' is the standard STATUS_ commands accessed directly without using the PAGE_PLUS commands.
3 All fans in the PSU shall be OR'ed into a single fan status bit for fault and warning conditions.

12.7 POWER MANAGEMENT BUS TEMPERATURE READ COMMANDS

The following temperature read commands as documented by the Power Management Bus specification Part II version 1.2 should be supported.
READ_TEMPERATURE_1(8Dh), should provide the PSU inlet temperature. READ_TEMPERATURE_2(8Eh), should provide the temperature of the SR heat sink in the PSU. READ_TEMPERATURE_3(8Fh), should provide the temperature of the PFC heat sink in the PSU.

12.8 PAGE (00h)

Setting a PAGE value of FFh is used to clear all status bits in all PAGEs with the CLEAR_FAULT command.

12.9 OPERATION (01h)

The OPERATION command is used to configure the operational state of the converter, in conjunction with input from the CONTROL pin. The OPERATION command is used to Turn the Power Management Bus device output on and off.
Bit [7] controls whether the Power Management Bus device output is on or off.
If Bit [7] is cleared (equals 0) then the output is off. If Bit [7] is set (equals 1), then the output is on.

12.10 ON_OFF_CONFIG (02h)

The ON_OFF_CONFIG command configures the combination of CONTROL pin input and serial bus commands needed to turn the unit on and off. This includes how the unit responds when power is applied. The default response for any Power Management Bus device is specified by the device manufacturer. The details of the ON_OFF_CONFIG data byte are shown in Table ON_OFF_CONFIG Data Byte.

Example conditions:

- If bit [4] is cleared, then the unit powers up and operates any time bias power is available regardless of the setting of bits [3:0].
- If bit [4] is set, bit [3] is set, and bit [2] is cleared, then the unit is turned on and off only by commands received over the serial bus.
- If bit [4] is set, bit [3] is cleared, and bit [2] is set, then the unit is turned on and off only by the CONTROL pin.

If bit [4] is set, bit [3] is set, and bit [2] is set, then the unit is turned on and off only when both the commands received over the serial bus AND the CONTROL pin are commanding the device to be on. If either a command from the serial bus OR the CONTROL pin commands the unit to be off, the unit turns off.

BIT NUMBER	PURPOSE	BIT VALUE	MEANING
[7:5]		000	Reserved For Future Use
4	Sets the default to either operate any time power is present or for the on/off to be controlled by CONTROL pin and serial bus commands	0	Unit powers up any time power is present regardless of state of the CONTROL pin
		1	Unit does not power up until commanded by the CONTROL pin and OPERATION command (as programmed in bits [3:0]).
3	Controls how the unit responds to commands received via the serial bus	0	Unit ignores the on/off portion of the OPERATION command from serial bus
		1	To start, the unit requires that that the on/off portion of the OPERATION command is instructing the unit to run. Depending on bit [2], the unit may also require the CONTROL pin to be asserted for the unit to start and energize the output.
2	Controls how the unit responds to the CONTROL pin	0	Unit ignores the CONTROL pin (on/off controlled only the OPERATION command)
		1	Unit requires the CONTROL pin to be asserted to start the unit. Depending on bit [3], the OPERATION command may also be required to instruct the device to start before the output is energized.
1	The CONTROL pin	0	Active low (Pull pin low to start the unit)
		1	Active high (Pull high to start the unit)
0	CONTROL pin action when commanding the unit to turn off	0	Use the programmed turn off delay and fall time
		1	Turn off the output and stop transferring energy to the output as fast as possible. The device's product literature shall specify whether or not the device sinks current to decrease the output voltage fall time.

Table 13: ON_OFF_CONFIG Data Byte

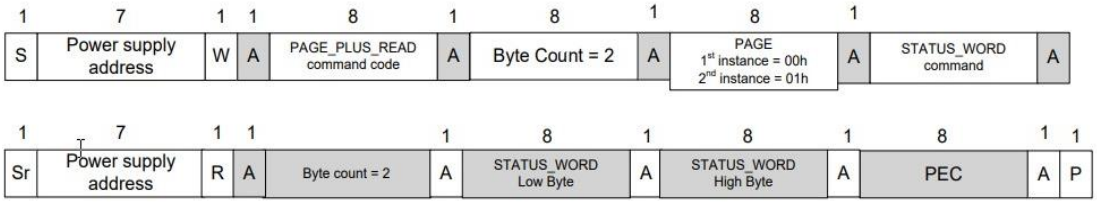
12.11 CLEAR_FAULTS COMMAND (03H)

The CLEAR_FAULTS command is used to clear any fault bits that have been set. This command clears all bits in all status registers simultaneously. At the same time, the device negates (clears, releases) its PS_ALERT signal output if the device is asserting the PS_ALERT signal.

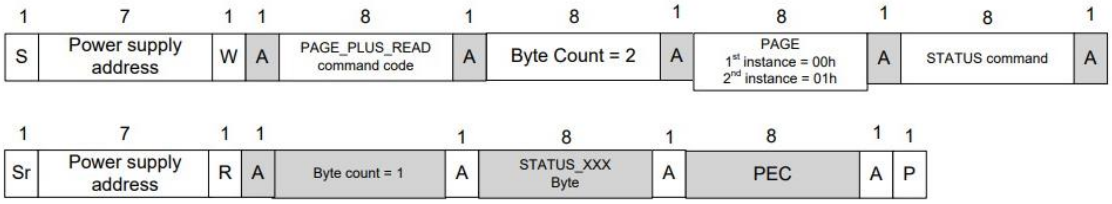
12.12 NEW PAGE_PLUS_WRITE / PAGE_PLUS_READ COMMANDS (05H/06H)

The new PAGE_PLUS_WRITE and PAGE_PLUS_READ commands are used with the STATUS_WORD, STATUS_INPUT, STATUS_TEMPERATURE, STATUS_IOUT, and STATUS_CML to create two instances of the same command. Each instance is set by the same events but cleared by their own master in the system. The instances at PAGE 00h are controlled by the system BMC and the instances at PAGE 01h are controlled by the system ME. Below are the protocols used to read and clear the STATUS_ commands using the PAGE_PLUS_WRITE and PAGE_PLUS_READ commands.

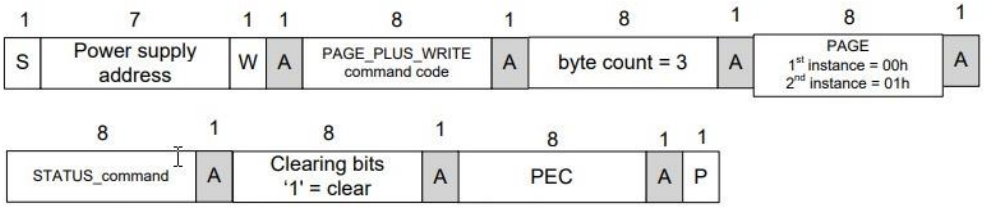
Reading STATUS_WORD
Block Write – Block Read Process Call with PEC



Reading STATUS_TEMPERATURE, STATUS_IOUT, STATUS_INPUT, STATUS_CML
Block Write – Block Read Process Call with PEC



Clearing STATUS commands (write '1' to clear a bit) STATUS_TEMPERATURE, STATUS_IOUT, STATUS_INPUT, STATUS_CML
Block Write with PEC



STATUS_WORD cannot be cleared directly It is cleared based on lower level status commands

12.13 CAPABILITY (19h)

This command provides a way for a host system to determine some key capabilities of a Power Management Bus device. There is one data byte formatted as shown in Table 12.2. This command is read only.

BITS	DESCRIPTION	VALUE	MEANING
7	Packet Error Checking	0	Packet Error Checking not supported
		1	Packet Error Checking is supported
6:5	Maximum Bus Speed	00	Maximum supported bus speed is 100 kHz
		01	Maximum supported bus speed is 400 kHz
		10	Reserved
		11	Reserved
4	PS_ALERT	0	The device does not have a PS_ALERT pin and does not support the PS_ALERT Response protocol
		1	The device does have a PS_ALERT pin and does support the PS_ALERT Response protocol
3:0	Reserved	X	Reserved

Table 14: CAPABILITY COMMAND Data Byte Format

12.14 QUERY (1Ah)

The QUERY command is used to ask a Power Management Bus device if it supports a given command, and if so, what data formats it supports for that command. This command uses the Block Write-Block Read Process Call described in the SMBus specification

BITS	VALUE	MEANING
7	1	Command is supported
	0	Command is not supported
6	1	Command is supported for write
	0	Command is not supported for write
5	1	Command is supported for read
	0	Command is not supported for read
4:2	000	Linear Data Format used
	001	16 bit signed number
	010	Reserved
	011	Direct Mode Format used
	100	8 bit unsigned number
	101	VID Mode Format used
	110	Manufacturer specific format used
	111	Command does not return numeric data. This is also used for commands that return blocks of data.
1:0	XX	Reserved for future use

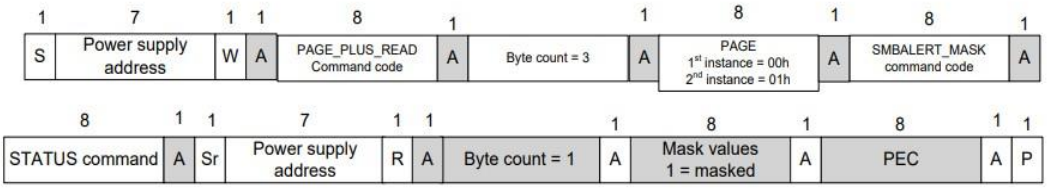
If bit [7] is zero, then the rest of the bits are “don’t care”.

Table 15. QUERY Command Returned Data Byte Format

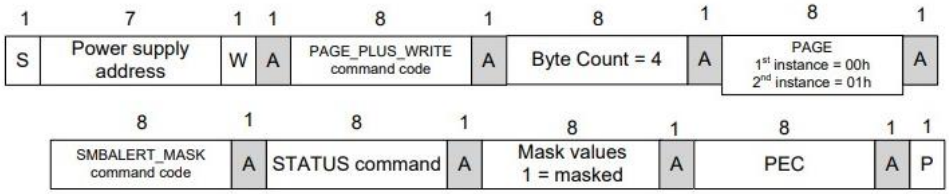
12.15 PS_ALERT_MASK (1Bh)

This allows the system to mask events from asserting the PS_ALERT signal and to read back this information from the PSU. PS_ALERT_MASK command can be used with any of the supported STATUS events. The events are masked from asserting PS_ALERT by writing a ‘1’ to the associated STATUS bits. The PS_ALERT_MASK command is used in conjunction with the PAGE_PLUS command and STATUS_ commands. It is not supported for masking the Non-PAGE’d STATUS_ commands. Below are the protocols.

Reading mask values using PAGE_PLUS
Block Write – Block Read Process Call with PEC



Writing mask values using PAGE_PLUS
Block Write with PEC

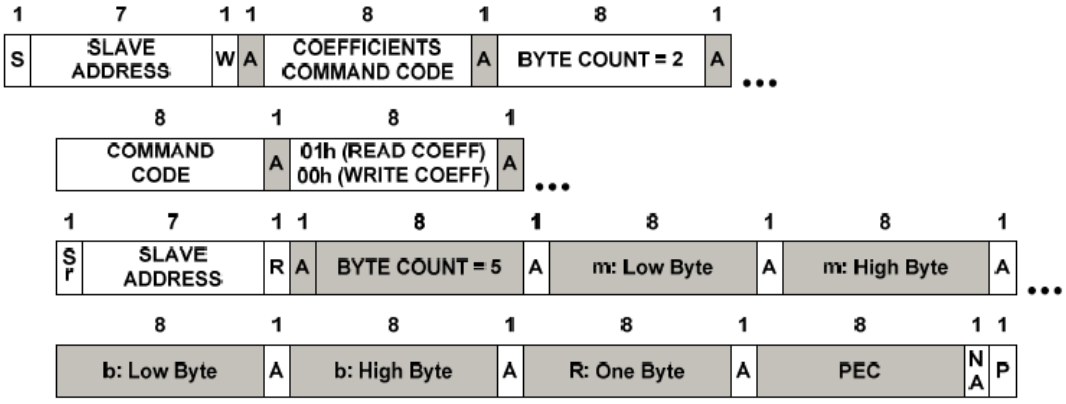


STATUS_WORD is not used with SMBALERT_MASK. Only the 'root' event bits are used to control the SMBAlert signal

12.16 COEFFICIENT (30h)

The power supply shall support the Power Management Bus COEFFICIENT command. The system shall use this to read the values of m, b, and R used to determine READ_EIN and READ_EOUT accumulated power values.

COMMAND	COEFFICIENTS SUPPORT	m	B	R
READ_EIN	Yes	01h	00h	00h
READ_EOUT	Yes	01h	00h	00h



12.17 FAN_CONFIG_1_2 (3Ah)

The FAN_CONFIG_1_2 command is used to define the presence of a fan and the method it is controlled (by duty cycle or RPM).

The first of the configuration tells the Power Management Bus device whether or not a fan associated with position 1 (or 2) is installed. Any combination of fan installation is permitted.

The second part of the configuration tells the device whether the fan speed commands are in RPM or PWM duty cycle (in percent). These settings do not have to be the same for Fan 1 and Fan 2.

The third part of the configuration data tells the Power Management Bus device the number of tachometer pulses per revolution each fan provides. This information is needed to be commanding and reporting fan speed in RPM. Two bits are provided for each fan. These settings do not have to be the same for Fan 1 and Fan 2. The binary values of these bits map to pulses per revolution as follows:

- 00b = 1 pulse per revolution,
- 01b = 2 pulses per revolution,
- 10b = 3 pulses per revolution,
- 11b = 4 pulses per revolution.

This command has one data byte formatted as follows:

BITS	VALUE	MEANING
7	1	Fan in position 1
6	0	Fan 1 commanded in Duty Cycle
	1	Fan 1 commanded in RPM
5:4	00b-11b	Fan 1 Tachometer Pulses Per Revolution
3	0	No fan in position 2
2	Not used	
1:0	Not used	

Table 16. FAN_CONFIG_1_2 Command

12.18 FAN_COMMAND_1 (3Bh)

The system may increase the power supplies fan speed through using the FAN_COMMAND_1 command. This command can only increase the power supplies fan speed; it cannot decrease the PSU fan speed below what the PSU minimum speed of the thermal requirement.

The default control mode of fan is duty (0-100).

12.19 READ_FAN_SPEED_1 (90h)

The system will read the fan speed by using the READ_FAN_SPEED_1 command. This data shall return the fan speed in the Power Management Bus linear format.

12.20 POWER MANAGEMENT BUS_REVISION (98h)

This is a correction to the table in the Power Management Bus part II specification regarding the POWER MANAGEMENT BUS_REVISION command.

Bits [7:4]	Part I revision	Bits [3:0]	Part II Revision
0000	1.0	0000	1.0
0001	1.1	0001	1.1
0010	1.2	0010	1.2
0011	1.3	0011	1.3

Table 17. POWER MANAGEMENT BUS_REVISION Command

12.21 MFR_EFFICIENCY_LL (AAh)

The MFR_EFFICIENCY_LL command sets or retrieves information about the efficiency of the device while operating at a low line condition. Not including the PEC byte, if used, and the byte count byte, there are fourteen data bytes as described below. The efficiency is specified at one input voltage and three data points consisting of output power and the efficiency at that output power. The three power ratings are typically referred as low, medium and high output power and are transmitted in that order. For example, the low, medium and high output power might correspond to 20%, 50% and 100% of the rated output power. The exact values of the output power is specified is left to the Power Management Bus device manufacturer. Each value (voltage, power or efficiency) is transmitted as two bytes in linear format.

BYTE NUMBER	BYTE ORDER	DESCRIPTION
0	Low Byte	The input voltage, in volts, at which the low line efficiency data is applicable. Note that byte 0 is the first data byte transmitted as part of the block transfer.
1	High Byte	
2	Low Byte	Power, in watts, at which the low power efficiency is specified
3	High Byte	
4	Low Byte	The efficiency, in percent, at the specified low power.
5	High Byte	
6	Low Byte	Power, in watts, at which the medium power efficiency is specified
7	High Byte	
8	Low Byte	The efficiency, in percent, at the specified medium power.
9	High Byte	
10	Low Byte	Power, in watts, at which the high power efficiency is specified
11	High Byte	
12	Low Byte	
13	High Byte	The efficiency, in percent, at the specified high power. Note that byte 13 is the last data byte transmitted as part of the block transfer.

Table 18. MFR_EFFICIENCY_LL

12.22 MFR_EFFICIENCY_HL (ABh)

The MFR_EFFICIENCY_HL command sets or retrieves information about the efficiency of the device while operating at a high line condition. Not including the PEC byte, if used, and the byte count byte, there are fourteen data bytes as described below. The efficiency is specified at one input voltage and three data points consisting of output power and the efficiency at that output power. The three power ratings are typically referred as low, medium and high output power and are transmitted in that order. For example, the low, medium and high output power might correspond to 20%,50% and 100% of the rated output power. The exact values of the output power is specified is left to the Power Management Bus device manufacturer. Each value (voltage, power or efficiency) is transmitted as two bytes in linear format.

BYTE NUMBER	BYTE ORDER	DESCRIPTION
0	Low Byte	The input voltage, in volts, at which the high line efficiency data is applicable. Note that byte 0 is the first data byte transmitted as part of the block transfer.
1	High Byte	
2	Low Byte	Power, in watts, at which the low power efficiency is specified
3	High Byte	
4	Low Byte	The efficiency, in percent, at the specified low power.
5	High Byte	
6	Low Byte	Power in watts, at which the medium power efficiency is specified
7	High Byte	
8	Low Byte	The efficiency, in percent, at the specified medium power.
9	High Byte	
10	Low Byte	Power, in watts, at which the high power efficiency is specified
11	High Byte	
12	Low Byte	The efficiency, in percent, at the specified high power. Note that byte 13 is the last data byte transmitted as part of the block transfer.
13	High Byte	

Table 19. MFR_EFFICIENCY_HL

12.23 READ_EIN (86h)

The new READ_EIN command is used to allow the system to apply its own input power filtering. This will allow the system to get faster input power data while preventing aliasing. The command returns an accumulated power value and an associated sample count of number of accumulated power values. This allows the system to calculate its own average power value each time the system polls the PSU.

	MIN	MAX	DESCRIPTION
Format	Power Management Bus Direct format m = 01h, R = 00h, b = 00h		Power Management Bus data format; refer to Power Management Bus specification for details.
Psample averaging period	4 AC cycles		Period instantaneous input power is averaged over to calculate Psample.
READ_EIN update period	80 / 66.7 ms (50/60 Hz)		Period at which the power accumulator and sample counter are updated
Accuracy (Pin>1000W Load)	+/-5%		The input power data shall meet these accuracy requirements over 100-127 VAC / 200-240 VAC and under the defined system polling rate.
Accuracy (Pin<1000 W Load)	+/-10 W		
Range of System polling period	1 sec	100 ms	The PSU shall be polled over this range of rates while testing accuracy.

IMPORTANT:
The PSU READ_EIN update period MUST always be less than the system polling period. To make sure the PSU is compatible with all possible system polling periods; the PSU must update the READ_EIN power accumulator and sample counter at a period less than 100msec (required period is 4 AC cycles 80/67msec).

Table 20. READ_EIN REQUIREMENTS SUMMARY

12.24 READ_EOUT (87h)

The new READ_EOUT command is used to allow the system to apply its own output power filtering. This will allow the system to get faster output power data while preventing aliasing. The command returns an accumulated power value and an associated sample count of number of accumulated power values. This allows the system to calculate its own average power value each time the system polls the PSU.

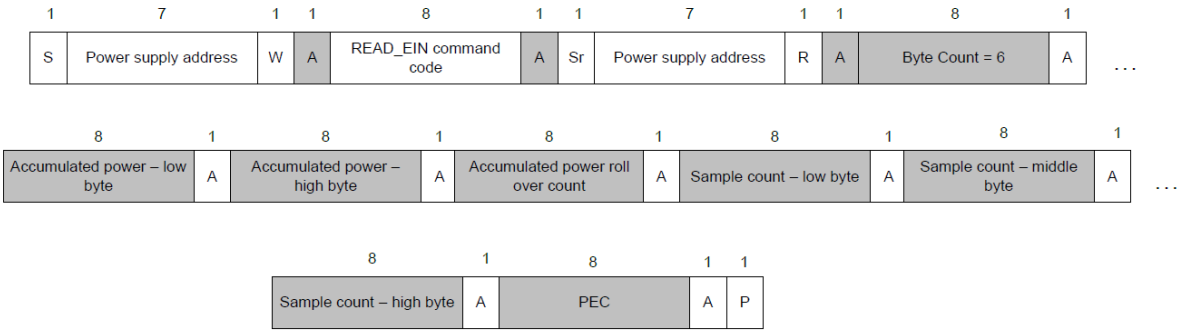
	MIN	MAX	DESCRIPTION
Format	Power Management Bus Direct format m = 01h, R = 00h, b = 00h		Power Management Bus data format; refer to Power Management Bus specification for details.
Psample averaging period	Nominal 50 msec		Period instantaneous input power is averaged over to calculate Psample.
Sampling period	Nominal 50 msec		Period at which the power accumulator and sample counter are updated
[Paccum / N] Accuracy (50% to 100% load)	±5%		The calculated output power data shall meet these accuracy requirements over 100-240VAC and under the defined system polling rate.
[Paccum / N] Accuracy (20% to 50% load)	±5%		
System polling rate	1 sample/s	10 samples /s	The PSU shall be polled over this range of rates while testing accuracy.

Table 21. READ_EOUT REQUIREMENTS SUMMARY

12.25 READ_EIN & READ_EOUT FORMATS

The READ_EIN and READ_EOUT commands shall use the Power Management Bus direct format to report an accumulated power value and the sample count. The Power Management Bus coefficients m, R, and b shall be fixed values and the PSU shall report these values using the Power Management Bus COEFFICIENT command. The coefficient m shall be set to 01h, coefficient R shall be set to 00h, and coefficient b shall be set to 00h.

READ_EIN and READ_EOUT shall use the SMBus Block Read with PEC protocol in the below format.



12.26 READ_EIN AND READ_EOUT ACCUMULATORS

The accumulated power data shall be the sum of input power values averaged over 4 AC cycles (or over 50ms for READ_EOUT). The value shall automatically roll-over when the 15 bit maximum value is reached (> 7FFFh). The sample count should increment 1 for each accumulated power value. The system shall calculate average power by dividing the accumulated power value by the sample count. The system must sample READ_EIN and READ_EOUT faster than the roll-over period to get an accurate power calculation. Below is a block diagram depicting the accumulator function in the PSU.

Important note: When the PSU responds to the system requesting READ_EIN or READ_EOUT data; the data in the sample count must always alignment with the number of samples accumulated in the power accumulator. To achieve this power accumulator, power rollover counter, and sample counter shall be loaded into a READ_EIN and READ_EOUT register at the same time.

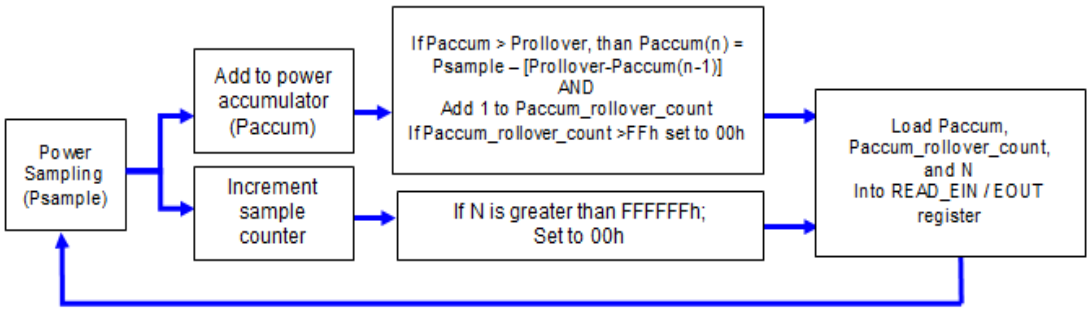


Figure 7. READ_EIN PSU Functional Diagram

VALUE	DESCRIPTION
Psample:	The sampled power value in linear or direct format
Paccum:	2 bytes in Power Management Bus linear or direct format. The accumulated power values made up of Psample(0) + Psample(1) + … + Psample(n)
N:	3 byte unsigned integer value. The number of accumulated power values summed in Paccum
Prollover:	The max value of Paccum before a rollover will occur
Paccum_rollover_count:	1 byte unsigned integer counting the number of times Paccum rolls over. Once this reaches FFh; it will automatically get reset to 00h

12.27 LINEAR DATA FORMAT

The Linear Data Format is typically used for commanding and reporting the parameters such as (but not only) the following:

- Output Current,
- Input Voltage,
- Input Current,
- Operating Temperatures,
- Time (durations), and Energy Storage capacitor Voltage.

The Linear Data Format is a two byte value with:

- An 11 bit, two's complement mantissa and,
- A 5 bit, two's complement exponent (scaling factor),
- The format of the two data bytes is illustrated in Figure 5.1 as show below.

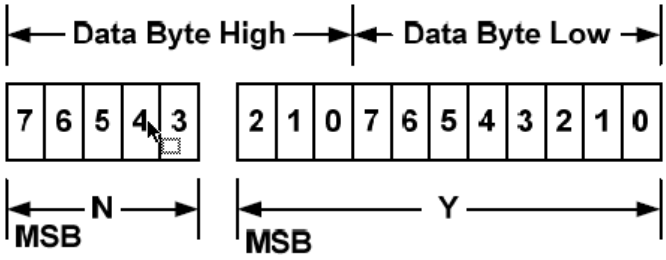


Figure 8. Linear Data Format Data Bytes

The relation between *Y*, *N* and the "real world" value is:

$X = Y \cdot 2^N$

Where, as described above:

X is the "real world" value;

Y is an 11 bit, two's complement integer; and

N is a 5 bit, two's complement integer.

Devices that use the linear format must accept and be able to process any value of *N*.

12.28 VOUT_MODE (20h)

The data byte for the VOUT_MODE command is one byte that consists of a three bit Mode and a five bit exponent. The three bit Mode shall be set to indicate the LINEAR mode for output voltage related commands. The five bit Exponent shall be set to indicate the value of the five bit two's complement exponent for the mantissa delivered as the data bytes for an output voltage related command.

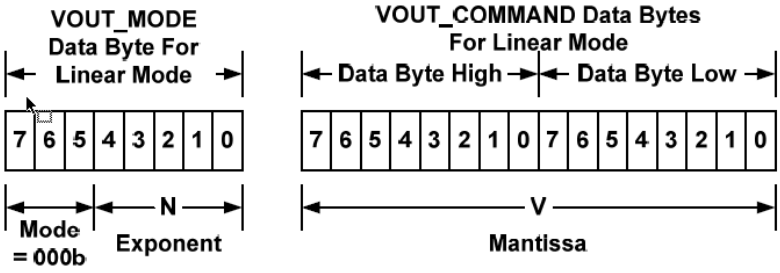


Figure 9. Linear Format Data Bytes

The voltage, in volts, is calculated from the equation Voltage = V·2N, where:

- V is a 16 bit unsigned binary integer
- N is a 5 bit two's complement binary integer

Sending the VOUT_MODE command with the address set for writing is not supported. If the system sends a VOUT_MODE command for a write, the power supply shall reject the command, and set the Invalid/Unsupported Data bit in the STATUS_CML register.

13 FRU SPECIFICATION

13.1 FRU DATA

The FRU data format is compliant with the IPMI ver.1.0 (per rev.1.1 from Sept.25, 1999) specification. The following is the exact listing of the EEPROM content. During testing this listing shall be followed and verified.

13.2 FRU DEVICE PROTOCOL

The FRU device will implement the same protocols, including the Byte Read, Sequential Read, Byte Write, and Page Read protocols.

Four pins will be allocated for the FRU information on the Power Supply connector. One pin is the serial clock (SCL). The second pin is used for serial data (SDA). Two pins are for address lines to indicate to the power supply's EEPROM which position the power supply is located in the system. The SCL and SDA signals are pulled up by system, the address lines are also pulled up by system.

A1 LOGICAL VOLTAGE	A0 LOGICAL VOLTAGE	PSU ADDRESS	FRU ADDRESS
0	0	0xB0	0xA0
0	1	0xB2	0xA2
1	0	0xB4	0xA4
1	1	0xB6	0xA6

13.3 PEC2000-54-074NA FRU DATA

ITEM	01	BYTE VALUE		DESCRIPTION	BLOCK TITLE
		DEC	HEX		
1	0000H	1	01	COMMON HEADER FORMAT VERSION	COMMON HEADER
2	0001H	0	00	INTERNAL USE AREA STARTING OFFSET (In Multiples Of 8 Bytes). 00H Indicates That This Area Is Not Present	
3	0002H	0	00	CHASSIS INFO AREA STARTING OFFSET (In Multiples Of 8 Bytes). 00H Indicates That This Area Is Not Present.	
4	0003H	0	00	BOARD AREA STARTING OFFSET (In Multiples Of 8 Bytes). 00H Indicates That This Area Is Not Present.	
5	0004H	1	01	PRODUCT INFO AREA STARTING OFFSET (In Multiples Of 8 Bytes).	
6	0005H	11	0B	MULTIRECORD AREA STARTING OFFSET (In Multiples Of 8 Bytes).	
7	0006H	0	00	PAD, Write As 00H	
8	0007H	243	F3	COMMON HEADER CHECKSUM (ZERO CHECKSUM)	
1	0008H	1	01	PRODUCT AREA FORMAT VERSION 7:4 - Reserved, Write As 0000B 3:0 - Format Version Number = 1H	PRODUCT INFORMATION AREA
2	0009H	10	0A	PRODUCT AREA LENGTH (In multiples of 8 bytes)	
3	000AH	25	19	LANGUAGE CODE (ENGLISH)Z	
4	000BH	200	C8	MANUFACTURER NAME TYPE / LENGTH (C8H) 7:6 - Type Code 5:0 - Number Of Data Bytes.	
5	000CH	98	62	b	
6	000DH	101	65	e	
7	000EH	108	6C	l	
8	000FH	32	20		
9	0010H	32	20		
10	0011H	32	20		
11	0012H	32	20		
12	0013H	32	20		
13	0014H	208	D0	PRODUCT NAME Type/Length (CEh) 7:6 - Type Code 5:0 - Number Of Data Bytes.	MANUFACTURER'S MODEL NUMBER
14	0015H	80	50	P	

15	0016H	69	45	E	
16	0017H	67	43	C	
17	0018H	50	32	2	
18	0019H	48	30	0	
19	001AH	48	30	0	
20	001BH	48	30	0	
21	001CH	45	2D	-	
22	001DH	53	35	5	
23	001EH	52	34	4	
24	001FH	45	2D	-	
25	0020H	48	30	0	
26	0021H	55	37	7	
27	0022H	52	34	4	
28	0023H	78	4E	N	
29	0024H	65	41	A	
30	0025H	212	D4	PRODUCT PART/MODEL NUMBER Type/Length (D4h)	CUSTOMER PART NUMBER
31	0026H	71	47	G	
32	0027H	78	4E	N	
33	0028H	48	30	0	
34	0029H	65	41	A	
35	002AH	32	20		
36	002BH	32	20		
37	002CH	32	20		
38	002DH	32	20		
39	002EH	32	20		
40	002FH	32	20		
41	0030H	32	20		
42	0031H	32	20		
43	0032H	32	20		
44	0033H	32	20		
45	0034H	32	20		
46	0035H	32	20		
47	0036H	32	20		
48	0037H	32	20		
49	0038H	32	20		
50	0039H	32	20		
51	003AH	195	C3	PRODUCT VERSION NUMBER Type/Length (C3h)	CUSTOMER CURRENT REVISION
52	003BH	86	56	V	To be updated
53	003CH	48	30	0	To be updated
54	003DH	48	30	0	To be updated
55	003EH	211	D3	PRODUCT SERIAL NUMBER type/length byte (D3)	
56	003FH	80	50	P	To be updated
57	0040H	69	45	E	To be updated
58	0041H	67	43	C	To be updated
59	0042H	50	32	2	To be updated
60	0043H	48	30	0	To be updated
61	0044H	48	30	0	To be updated
62	0045H	48	30	0	To be updated
63	0046H	78	4E	N	To be updated
64	0047H	65	41	A	To be updated
65	0048H	89	59	Y	To be updated
66	0049H	89	59	Y	To be updated

67	004AH	77	4D	M	To be updated
68	004BH	77	4D	M	To be updated
69	004CH	88	58	X	To be updated
70	004DH	88	58	X	To be updated
71	004EH	88	58	X	To be updated
72	004FH	88	58	X	To be updated
73	0050H	88	58	X	To be updated
74	0051H	0	00		To be updated
75	0052H	192	C0	FRU FILE ID Type/Length Byte	Not used, code is zero length byte
76	0053H	192	C0	FRU FILE ID Type/Length Byte	Not required
77	0054H	193	C1	ENCODED TO INDICATE NO MORE INFO FIELDS	
78	0055H	0	00	PAD (Always Zero)	
79	0056H	0	00	PAD (Always Zero)	
80	0057H	78	56	CHECKSUM(100H-(LOWER BYTE(SUM OF BYTES)))	To be updated
1	0058H	0	00	RECORD TYPE ID 0x00 = POWER SUPPLY INFORMATION	MULTI RECORD AREA
2	0059H	2	02	7:7 END OF LIST, 6:4 = 000B, 3:0 RECORD FORMAT VERSION = 2	
3	005AH	24	18	RECORD LENGTH OF MULTIRECORD	
4	005BH	134	86	RECORD CHECKSUM (ZERO CHECKSUM)	
5	005CH	96	60	HEADER CHECKSUM (ZERO CHECKSUM)	
1	005DH	208	D0	15-12:RESERVED,WRITE AS 0000B	2000W
2	005EH	7	07	11-0:OVERALL CAPACITY(WATTS)	
3	005FH	196	C4	PEAK VALUE	2500W
4	0060H	9	09	LSB FIRST	
5	0061H	55	37	INRUSH CURRENT ,FFH IF NOT SPECIFIED	55A
6	0062H	5	05	INRUSH INTERVAL IN MS.	5mS
7	0063H	16	10	LOW END INPUT VOLTAGE RANGE 1 100V = 2710H	100V
8	0064H	39	27		
9	0065H	156	9C	HIGH END INPUT VOLTAGE RANGE 1 127V=319CH	127V
10	0066H	49	31		
11	0067H	32	20	LOW END INPUT VOLTAGE RANGE 2 200V = 4E20H	200V
12	0068H	78	4E		
13	0069H	192	C0	HIGH END INPUT VOLTAGE RANGE 2 240V = 5DC0H	240V
14	006AH	93	5D		
15	006BH	50	32	LOW END INPUT FREQUENCY RANGE 50HZ=32H	50Hz
16	006CH	60	3C	HIGH END INPUT FREQUENCY RANGE 60HZ = 3CH	60Hz
17	006DH	12	0C	A/C DROPOUT TOLERANCE IN mS 10mS=0CH	12mS
18	006EH	30	1E	7-5:RESERVED,WRITE AS 000B 4:TACHOMETER PULSES PER POTATION/PREDICTIVE FALL POLARITY YES=1(FAIL=1,PASS=0) 3:HOT SWAP/REDUNDANCY SUPPORT YES=1 2:AUTOSWITCH YES=1 1:POWER FACTOR CORRECTION YES=1 0:PREDICTIVE FALL SUPPLY YES=1	
19	006FH	108	6C	PEAK WATTAGE 15-12:HOLD UP TIME IN SECONDS 1S=1H	
20	0070H	247	F7	11-0 PEAK CAPACITY (WATTS)(LSB FIRST) 2100W=0834H	15S
21	0071H	0	00	COMMBINED WATTAGE 7-4:Voltage 1 3-0:Voltage 2=00H	
22	0072H	0	00	BYTE 2:3 TOTAL COMBINED WATTAGE (LSB FIRST) W=0000H	0
23	0073H	0	00	BYTE 2:3 TOTAL COMBINED WATTAGE (LSB FIRST) W=0000H	
24	0074H	16	10	PREDICTIVE FAIL TACHOMETER LOWER THRESHOLD (PRM/60)1000/60=16	
1	0075H	10	0A	RECORD TYPE ID 0X01 =DC OUTPUT Record	MULTIRECORD

2	0076H	130	82	7:7 END OF LIST 6:4=000 3:0 RECORD FORMAT VERSION=2	HEADER
3	0077H	13	0D	RECORD LENGTH OF MULTIRECORD	
4	0078H	97	61	RECORD CHECKSUM	
5	0079H	6	06	HEADER CHECKSUM	
1	007AH	1	01	+54.5V 7:STANDBY =0, 6-4:RESERVED 000B, 3-0:OUTPUT NUMBER=0001B	+54.5V
2	007BH	74	4A	NOMINAL VOLTAGE (10mV)1220=04C4H	54.5V
3	007CH	21	15		
4	007DH	57	39	MAXIMUM NEGATIVE VOLTAGE DEVIATION (10mV) 1159=0487H	51.77V
5	007EH	20	14		
6	007FH	90	5A	MAXIMUM POSITIVE VOLTAGE DEVIATION (10mV) 1281=0501H	57.22V
7	0080H	22	16		
8	0081H	28	1C	RIPPLE AND NOISE PK-PK 10Hz TO 20MHz(mV) 120mV=0078H	540mV
9	0082H	2	02		
10	0083H	0	00	MINIMUM CURRENT DRAW(10mA)	0A
11	0084H	0	00		
12	0085H	86	56	MAXIMUM CURRENT DRAW(10mA)	36.7A
13	0086H	14	0E		
1	0087H	0	00	Unused Area	
2	0088H	0	00	Unused Area	
3	0089H	0	00	Unused Area	
4	008AH	0	00	Unused Area	
5	008BH	0	00	Unused Area	
1	008CH	0	00	Unused Area	
2	008DH	0	00	Unused Area	
3	008EH	0	00	Unused Area	
4	008FH	0	00	Unused Area	
5	0090H	0	00	Unused Area	
6	0091H	0	00	Unused Area	
7	0092H	0	00	Unused Area	
8	0093H	0	00	Unused Area	
9	0094H	0	00	Unused Area	
10	0095H	0	00	Unused Area	
11	0096H	0	00	Unused Area	
12	0097H	0	00	Unused Area	
13	0098H	0	00	Unused Area	
1	0099H	0	00	Unused Area	
2	009AH	0	00	Unused Area	
3	009BH	0	00	Unused Area	
4	009CH	0	00	Unused Area	
5	009DH	0	00	Unused Area	
6	009EH	0	00	Unused Area	
7	009FH	0	00	Unused Area	
8	00A0H	0	00	Unused Area	
9	00A1H	0	00	Unused Area	
10	00A2H	0	00	Unused Area	
11	00A3H	0	00	Unused Area	
12	00A4H	0	00	Unused Area	
13	00A5H	0	00	Unused Area	
14	00A6H	0	00	Unused Area	
15	00A7H	0	00	Unused Area	

16	00A8H	0	00	Unused Area	
17	00A9H	0	00	Unused Area	
18	00AAH	0	00	Unused Area	
19	00ABH	0	00	Unused Area	
20	00ACH	0	00	Unused Area	
21	00ADH	0	00	Unused Area	
22	00AEH	0	00	Unused Area	
23	00AFH	0	00	Unused Area	
24	00B0H	0	00	Unused Area	
25	00B1H	0	00	Unused Area	
26	00B2H	0	00	Unused Area	
27	00B3H	0	00	Unused Area	
28	00B4H	0	00	Unused Area	
29	00B5H	0	00	Unused Area	
30	00B6H	0	00	Unused Area	
31	00B7H	0	00	Unused Area	
32	00B8H	0	00	Unused Area	
33	00B9H	0	00	Unused Area	
34	00BAH	0	00	Unused Area	
35	00BBH	0	00	Unused Area	
36	00BCH	0	00	Unused Area	
37	00BDH	0	00	Unused Area	
38	00BEH	0	00	Unused Area	
39	00BFH	0	00	Unused Area	
40	00C0H	0	00	Unused Area	
41	00C1H	0	00	Unused Area	
42	00C2H	0	00	Unused Area	
43	00C3H	0	00	Unused Area	
44	00C4H	0	00	Unused Area	
45	00C5H	0	00	Unused Area	
46	00C6H	0	00	Unused Area	
47	00C7H	0	00	Unused Area	
48	00C8H	0	00	Unused Area	
49	00C9H	0	00	Unused Area	
50	00CAH	0	00	Unused Area	
51	00CBH	0	00	Unused Area	
52	00CCH	0	00	Unused Area	
53	00CDH	0	00	Unused Area	
54	00CEH	0	00	Unused Area	
55	00CFH	0	00	Unused Area	
56	00D0H	0	00	Unused Area	
57	00D1H	0	00	Unused Area	
58	00D2H	0	00	Unused Area	
59	00D3H	0	00	Unused Area	
60	00D4H	0	00	Unused Area	
61	00D5H	0	00	Unused Area	
62	00D6H	0	00	Unused Area	
63	00D7H	0	00	Unused Area	
64	00D8H	0	00	Unused Area	
65	00D9H	0	00	Unused Area	
66	00DAH	0	00	Unused Area	
67	00DBH	0	00	Unused Area	

68	00DCH	0	00	Unused Area	
69	00DDH	0	00	Unused Area	
70	00DEH	0	00	Unused Area	
71	00DFH	0	00	Unused Area	
72	00E0H	0	00	Unused Area	
73	00E1H	0	00	Unused Area	
74	00E2H	0	00	Unused Area	
75	00E3H	0	00	Unused Area	
76	00E4H	0	00	Unused Area	
77	00E5H	0	00	Unused Area	
78	00E6H	0	00	Unused Area	
79	00E7H	0	00	Unused Area	
80	00E8H	0	00	Unused Area	
81	00E9H	0	00	Unused Area	
82	00EAH	0	00	Unused Area	
83	00EBH	0	00	Unused Area	
84	00ECH	0	00	Unused Area	
85	00EDH	0	00	Unused Area	
86	00EEH	0	00	Unused Area	
87	00EFH	0	00	Unused Area	
88	00F0H	0	00	Unused Area	
89	00F1H	0	00	Unused Area	
90	00F2H	0	00	Unused Area	
91	00F3H	0	00	Unused Area	
92	00F4H	0	00	Unused Area	
93	00F5H	0	00	Unused Area	
94	00F6H	0	00	Unused Area	
95	00F7H	0	00	Unused Area	
96	00F8H	0	00	Unused Area	
97	00F9H	0	00	Unused Area	
98	00FAH	0	00	Unused Area	
99	00FBH	0	00	Unused Area	
100	00FCH	0	00	Unused Area	
101	00FDH	0	00	Unused Area	
102	00FEH	0	00	Unused Area	
103	00FFH	0	00	Unused Area	

Table showing PEC2000-54-074NA HEX Information

Addr	0	1	2	3	4	5	6	7	8	9	A	B	C	D	E	F
00	01	00	00	00	01	0B	00	F3	01	0A	19	C8	62	65	6C	20
10	20	20	20	20	D0	50	45	43	32	30	30	30	2D	35	34	2D
20	30	37	34	4E	41	D4	47	4E	30	41	20	20	20	20	20	20
30	20	20	20	20	20	20	20	20	20	20	C3	56	30	30	D3	50
40	45	43	32	30	30	30	4E	41	59	59	4D	4D	58	58	58	58
50	58	00	C0	C0	C1	00	00	56	00	02	18	86	60	D0	07	C4
60	09	37	05	10	27	9C	31	20	4E	C0	5D	32	3C	0C	1E	6C
70	F7	00	00	00	10	0A	82	0D	61	06	01	4A	15	39	14	5A
80	16	1C	02	00	00	56	0E	00	00	00	00	00	00	00	00	00
90	00	00	00	00	00	00	00	00	00	00	00	00	00	00	00	00
A0	00	00	00	00	00	00	00	00	00	00	00	00	00	00	00	00
B0	00	00	00	00	00	00	00	00	00	00	00	00	00	00	00	00
C0	00	00	00	00	00	00	00	00	00	00	00	00	00	00	00	00
D0	00	00	00	00	00	00	00	00	00	00	00	00	00	00	00	00
E0	00	00	00	00	00	00	00	00	00	00	00	00	00	00	00	00
F0	00	00	00	00	00	00	00	00	00	00	00	00	00	00	00	00