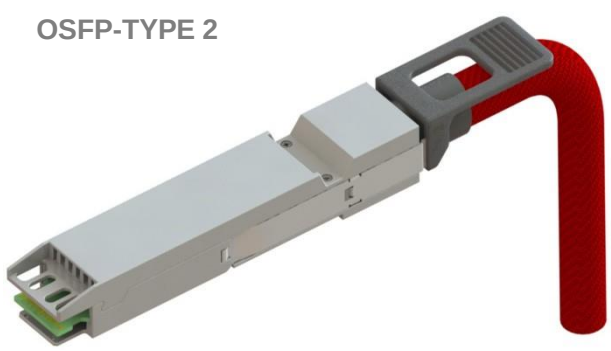
# Hairtail+ 800G OSFP TO 2xOSFP-RHS Active Direct Attached Cable





## FEATURES

- Module compliant to OSFP MSA
- Transmission data rate up to PAM4 112Gbps per channel
- Low power consumption, meeting 1.5W module LP mode
- Linear PAM4 programmable equalizer optimized for 56GBaud copper link up to max length 5M on 25AWG
- Enables a transparent ACC solution meeting all IEEE 400GBASE-CR4 Auto-Negotiation and Link Training
- Low latency
- Supports device programming by MCU with I2C
- Operates from a single 3.3V power supply with an integrated Power on reset (POR)
- Operating case temperature 0°C to +70°C
- RoHS2.0 compliant

## Absolute Maximum Ratings

| Parameter | Symbol | Min | Typical | Max | Unit |
|---|---|---|---|---|---|
| Supply Voltage | Vcc | -0.3 | 3.3 | 3.6 | V |
| Storage temperature | Ts | -40 | | 85 | ºC |
| Operating Case temperature | Tc | 0 | | 70 | ºC |
| Humidity | Rh | 5 | | 85 | % |
| Data Rate | | | 800 | | Gbps |

## Physical Characteristics

| Parameter | Symbol | Min | Typical | Max | Unit |
|---|---|---|---|---|---|
| Length | L | 2 | | 5 | M |
| AWG | | 32 | | 25 | AWG |
| Jacket material | | HAIRTAIL+ Technology Net, Red | | | |

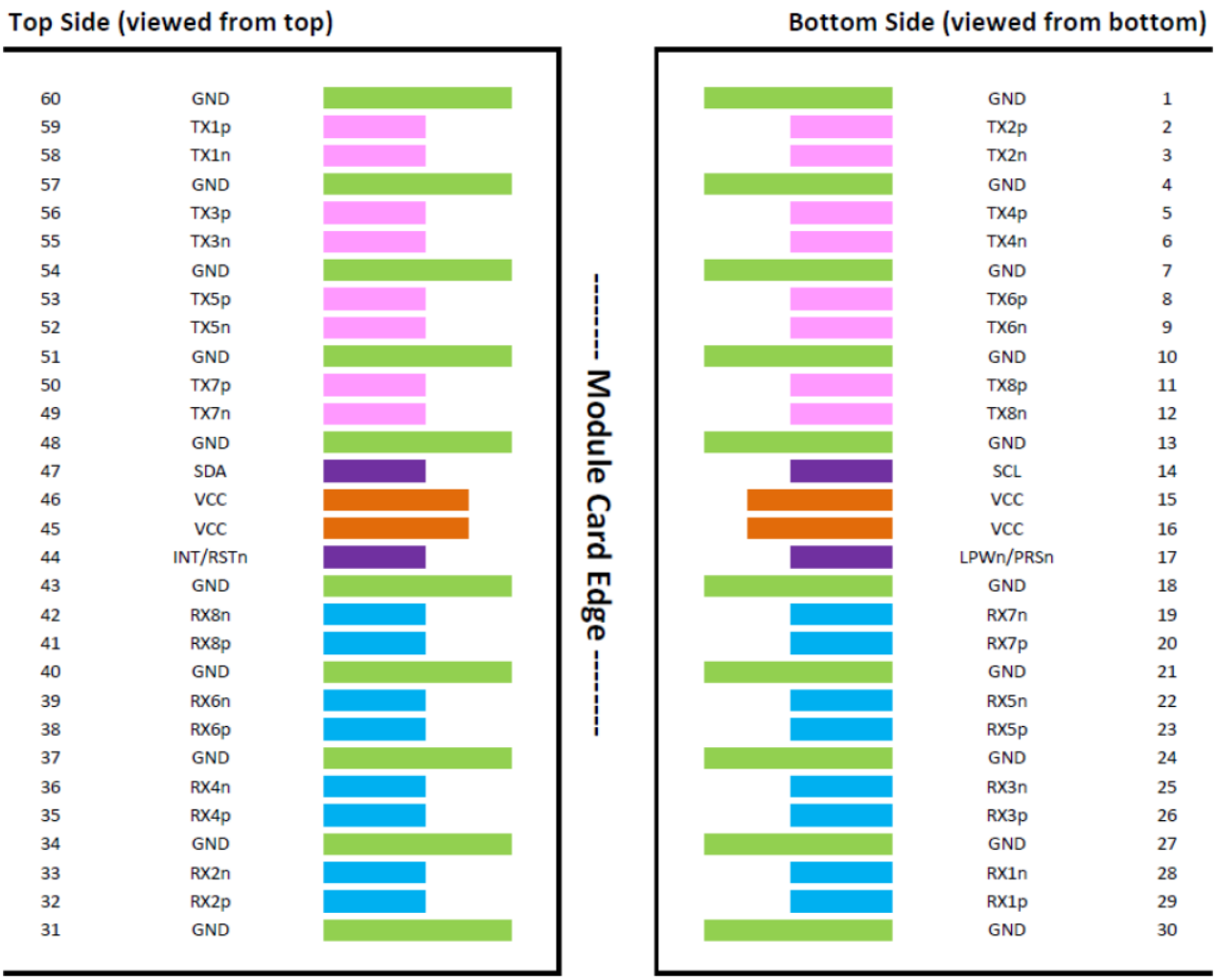
## Electrical Specifications

| Parameter | Symbol | Min | Typical | Max | Unit |
|---|---|---|---|---|---|
| Input Amplitude | | 800 | | 1200 | mVpp |
| Control Logic Input LOW Voltage | $V_{IL}$ | -0.3 | | 0.35*$V_{CC}$ | V |
| Control Logic Input HIGH Voltage | $V_{IH}$ | 0.65* VCC | | VCC +0.3 | V |
| Control Logic Input LOW Current | $I_{IL}$ | -100 | | +100 | uA |
| Control Logic Input HIGH Current | $I_{IH}$ | -100 | | +100 | uA |
| Output Logic LOW | $V_{OL}$ | | | 0.25* VCC | V |
| I2C Master Mode Output Frequency | | | 400 | | kHz |

## High-Speed Specifications

| Parameter | Symbol | Min | Typical | Max | Unit |
|---|---|---|---|---|---|
| Raw cable impedance | Zca | 90 | 100 | 110 | ohm |
| Mated connector Impedance | Zmated | 85 | | 110 | ohm |
| Maximum insertion loss at 26.56 GHz | SDD21 | 11 | | 19.75 | dB |
| Differential to common-mode return loss | SCD11/22 | $RLcd(f) \geq \begin{cases} 22-10(f/26.56) & 0.05 \leq f < 26.56 \\ 15-3(f/26.56) & 26.56 \leq f \leq 40 \end{cases}$ For 0.05 ≤f ≤40 GHz, Where f is the frequency in GHz | | | dB |
| Differential to common-mode conversion loss | SCD21-SDD21 | $Conversion\_loss(f) - IL(f) \geq \begin{cases} 10 & 0.05 \leq f < 12.89 \\ 14-0.3108f & 12.89 \leq f \leq 40 \end{cases}$ For 0.05 ≤f ≤40 GHz, Where f is the frequency in GHz | | | dB |
| Common-mode to common-mode return loss | SCC11/22 | $RLcc(f) \geq 1.8$ For 0.05 ≤f ≤40 GHz, Where f is the frequency in GHz | | | dB |
| Minimum COM | COM | 3 | | | dB |
| Minimum cable assembly ERL[a] | ERL | 8.25 | | | dB |
| BER With FEC | | | | $2.4x10^{-4}$ | |

## Pin Description



**Electrical Pin-out Details for OSFP**

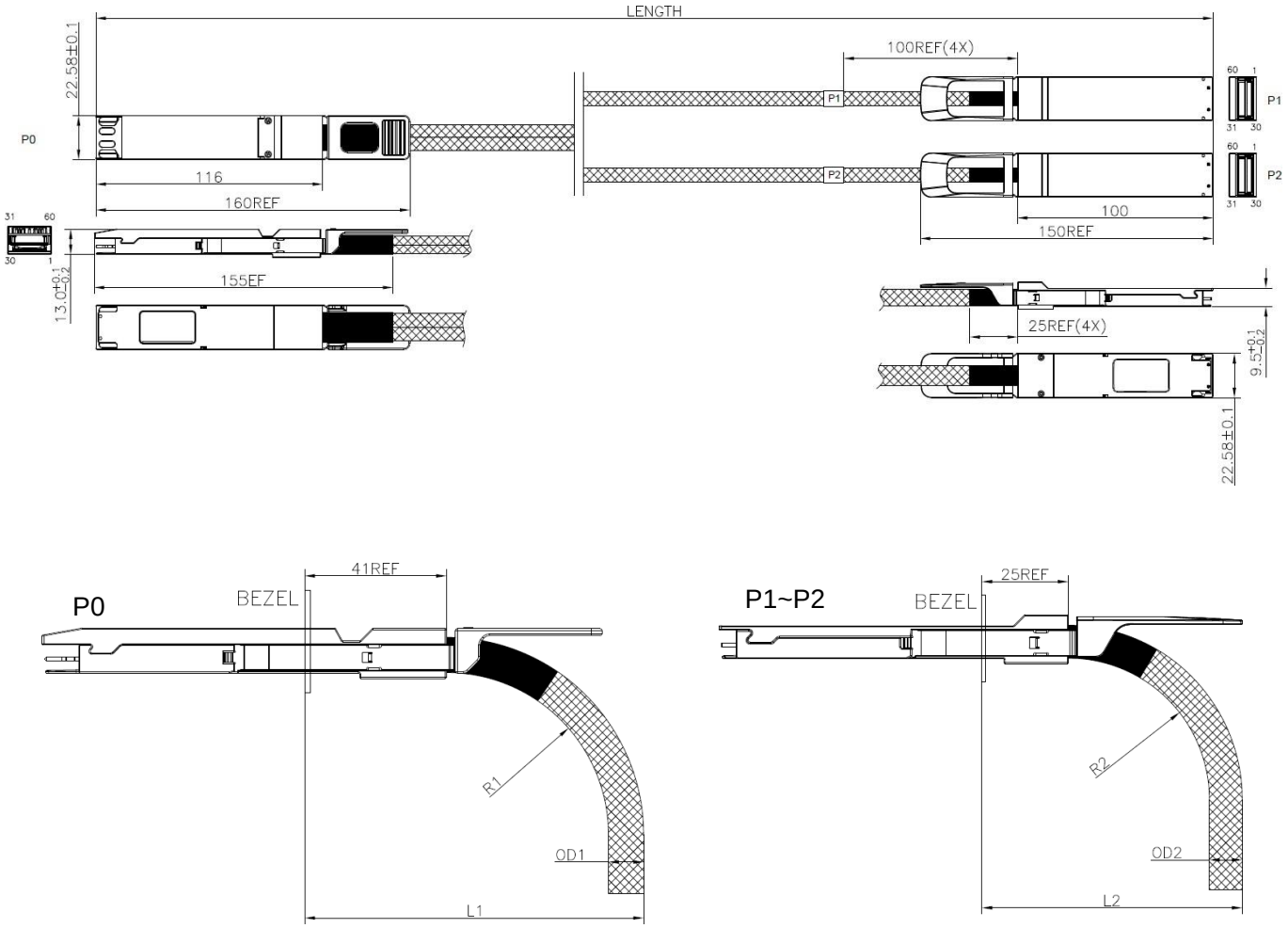
| Pin# | Symbol | Description | Logic | Direction | Plug Sequence | Notes |
|---|---|---|---|---|---|---|
| 1 | GND | Ground | | | 1 | |
| 2 | TX2p | Transmitter Data Non-Inverted | CML-I | Input from Host | 3 | |
| 3 | TX2n | Transmitter Data Inverted | CML-I | Input from Host | 3 | |
| 4 | GND | Ground | | | 1 | |
| 5 | TX4p | Transmitter Data Non-Inverted | CML-I | Input from Host | 3 | |
| 6 | TX4n | Transmitter Data Inverted | CML-I | Input from Host | 3 | |
| 7 | GND | Ground | | | 1 | |
| 8 | TX6p | Transmitter Data Non-Inverted | CML-I | Input from Host | 3 | |
| 9 | TX6n | Transmitter Data Inverted | CML-I | Input from Host | 3 | |
| 10 | GND | Ground | | | 1 | |
| 11 | TX8p | Transmitter Data Non-Inverted | CML-I | Input from Host | 3 | |
| 12 | TX8n | Transmitter Data Inverted | CML-I | Input from Host | 3 | |
| 13 | GND | Ground | | | 1 | |
| 14 | SCL | 2-wire Serial interface clock | LVCMOS-I/O | Bi-directional | 3 | Open-Drain with pull-up resistor on Host |
| 15 | VCC | +3.3V Power | | Power from Host | 2 | |
| 16 | VCC | +3.3V Power | | Power from Host | 2 | |
| 17 | LPWn/PRSn | Low-Power Mode / Module Present | Multi-Level | Bi-directional | 3 | See pin description for required circuit |
| 18 | GND | Ground | | | 1 | |
| 19 | RX7n | Receiver Data Inverted | CML-O | Output to Host | 3 | |
| 20 | RX7p | Receiver Data Non-Inverted | CML-O | Output to Host | 3 | |
| 21 | GND | Ground | | | 1 | |
| 22 | RX5n | Receiver Data Inverted | CML-O | Output to Host | 3 | |
| 23 | RX5p | Receiver Data Non-Inverted | CML-O | Output to Host | 3 | |
| 24 | GND | Ground | | | 1 | |
| 25 | RX3n | Receiver Data Inverted | CML-O | Output to Host | 3 | |
| 26 | RX3p | Receiver Data Non-Inverted | CML-O | Output to Host | 3 | |
| 27 | GND | Ground | | | 1 | |
| 28 | RX1n | Receiver Data Inverted | CML-O | Output to Host | 3 | |
| 29 | RX1p | Receiver Data Non-Inverted | CML-O | Output to Host | 3 | |
| 30 | GND | Ground | | | 1 | |

| Pin# | Symbol | Description | Logic | Direction | Plug Sequence | Notes |
|---|---|---|---|---|---|---|
| 31 | GND | Ground | | | 1 | |
| 32 | RX2p | Receiver Data Non-Inverted | CML-O | Output to Host | 3 | |
| 33 | RX2n | Receiver Data Inverted | CML-O | Output to Host | 3 | |
| 34 | GND | Ground | | | 1 | |
| 35 | RX4p | Receiver Data Non-Inverted | CML-O | Output to Host | 3 | |
| 36 | RX4n | Receiver Data Inverted | CML-O | Output to Host | 3 | |
| 37 | GND | Ground | | | 1 | |
| 38 | RX6p | Receiver Data Non-Inverted | CML-O | Output to Host | 3 | |
| 39 | RX6n | Receiver Data Inverted | CML-O | Output to Host | 3 | |
| 40 | GND | Ground | | | 1 | |
| 41 | RX8p | Receiver Data Non-Inverted | CML-O | Output to Host | 3 | |
| 42 | RX8n | Receiver Data Inverted | CML-O | Output to Host | 3 | |
| 43 | GND | Ground | | | 1 | |
| 44 | INT/RSTn | Module Interrupt / Module Reset | Multi-Level | Bi-directional | 3 | See pin description for required circuit |
| 45 | VCC | +3.3V Power | | Power from Host | 2 | |
| 46 | VCC | +3.3V Power | | Power from Host | 2 | |
| 47 | SDA | 2-wire Serial interface data | LVCMOS-I/O | Bi-directional | 3 | Open-Drain with pull-up resistor on Host |
| 48 | GND | Ground | | | 1 | |
| 49 | TX7n | Transmitter Data Inverted | CML-I | Input from Host | 3 | |
| 50 | TX7p | Transmitter Data Non-Inverted | CML-I | Input from Host | 3 | |
| 51 | GND | Ground | | | 1 | |
| 52 | TX5n | Transmitter Data Inverted | CML-I | Input from Host | 3 | |
| 53 | TX5p | Transmitter Data Non-Inverted | CML-I | Input from Host | 3 | |
| 54 | GND | Ground | | | 1 | |
| 55 | TX3n | Transmitter Data Inverted | CML-I | Input from Host | 3 | |
| 56 | TX3p | Transmitter Data Non-Inverted | CML-I | Input from Host | 3 | |
| 57 | GND | Ground | | | 1 | |
| 58 | TX1n | Transmitter Data Inverted | CML-I | Input from Host | 3 | |
| 59 | TX1p | Transmitter Data Non-Inverted | CML-I | Input from Host | 3 | |
| 60 | GND | Ground | | | 1 | |

## Module Memory Map

Compatible with CMIS rev 5.0 or further CMIS revisions and customer spec.

## Mechanical Dimensions




**Mechanical Drawing**

### Bending radius

| Wire gauge | OD1 (Ref) | Min. bend radius (R1) | Min. Bend space(L1) | OD2 (Ref) | Min. bend radius (R2) | Min. Bend space(L2) |
|---|---|---|---|---|---|---|
| 28AWG | 10.2mm | 30mm | 80mm | 7.0mm | 25mm | 60mm |
| 25AWG | 13.0mm | 40mm | 95mm | 9.0mm | 30mm | 65mm |

## Ordering Information

| Model Number | Part Number | Description |
|---|---|---|
| A-100N-O-2OR-040B | 1190107014028 | 800G OSFP to 2XOSFP ACC,IB NDR,HAIRTAIL+, 4.0M,25AWG, RED |
| A-100N-O-2OR-050B | 1190107014030 | 800G OSFP to 2XOSFP ACC,IB NDR,HAIRTAIL+, 5.0M,25AWG, RED |

## References

1. IEEE802.3ck
2. OSFP MSA Rev5.0
3. Common Management Interface Specification (CMIS) Rev5.0
4. IB NDR

## Revision Records

| REV. | Description | Designed | Checked | Approved | Issue Date |
|---|---|---|---|---|---|
| X1 | Initial Released | SHAN CHEN | XICHUN TAN | RYAN LEI | 2023.02.24 |
| X2 | Change the P1~P4 connector models & Cable Spec. | SHAN CHEN | XICHUN TAN | RYAN LEI | 2023.08.15 |