Hairtail 400G HDR OSFP TO 2xQSFP56

Active Direct Attached Cable

FEATURES

- Module compliant to OSFP MSA & QSFP MSA
- InfiniBand HDR compatible
- Transmission data rate up to PAM4 53.125Gbps per channel
- Enable 400Gb/s Transmission
- Supporting 28Gbaud line rate with highly liner equalization
- Maximum link length up to 7m
- Enable Auto-Negotiation and Link Training
- Low latency<10ps
- Supports device programming by MCU with I2C
- 3.3V Power supply
- Low power consumption
- Operating case temperature 0°C to +70°C
- RoHS2.0 compliant

Absolute Maximum Ratings

Parameter	Symbol	Min	Typical	Max	Unit
Supply Voltage	Vcc	-0.3	3.3	3.6	V
Storage temperature	Ts	-40		85	ºC
Operating Case temperature	Tc	0		70	ºC
Humidity	Rh	5		85	%
Data Rate			400		Gbps

Physical Characteristics

Parameter	Symbol	Min	Typical	Max	Unit
Length	L	2		7	M
AWG		32		26	AWG
Jacket material		HAIRTAIL Technology Net, Red			

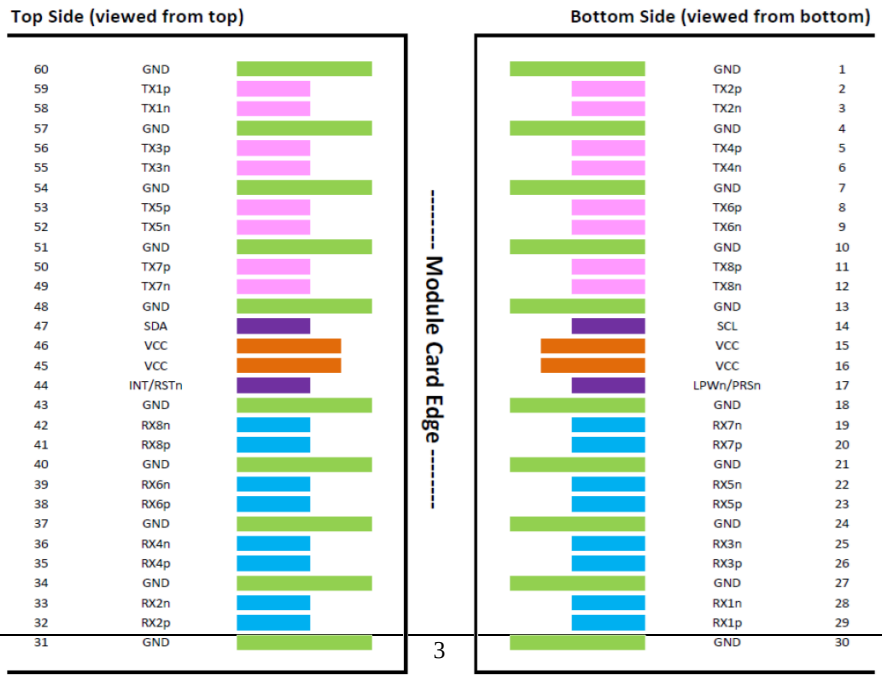
Electrical Specifications

Parameter	Symbol	Min	Typical	Max	Unit
Power supply voltage	VCC	3.1	3.3	3.5	V
Input Amplitude		800		1200	mVpp
Input LOW Voltage	V_{IL}	-0.3		0.35*V_{CC}	V
Input HIGH Voltage	V_{IH}	0.65* VCC		VCC +0.3	V
Output Logic LOW	V_{OL}			0.25* VCC	V
I2C Master Mode Output Frequency			400		kHz
400G end Power consumption			1.2	1.5	W
200G end Power consumption			0.6	0.7	W

High-Speed Specifications

Parameter	Symbol	Min	Typical	Max	Unit
Raw cable impedance	Zca	90	100	110	ohm
Mated connector Impedance	Zmated	85	100	115	ohm
Insertion loss at 13.28 GHz	SDD21	6		14	dB
Return loss	SDD11/22	Return_loss(f)≥ { 11, 0.05≤f < 26.5625/7.5; 6.0– 9.2lg(15f/ 5.5*7 26.5625), 26.5625/7.5≤f≤26.5 }			dB
Differential to common-mode return loss	SCD11/22	Return_loss(f)≥ { -25+(20/26.5625)f, 0.05≤f < 26.5625/2; -18+(6/26.5625)f, 26.5625/2≤f≤26.5625 }			dB
Differential to common-mode conversion loss	SCD21-SDD21	Conversion _loss(f) – IL(f)≥ { 10, 0.01≤f < 12.89; 27-(29/22)f, 12.89≤f < 15.7; 6.3, 15.7≤f≤19 }			dB
Minimum COM	COM	3			dB
BER				2.4x10-4	

OSFP Pin Description



Electrical Pin-out Details for OSFP

Pin#	Symbol	Description	Logic	Direction	Plug Sequence	Notes
1	GND	Ground			1	
2	TX2p	Transmitter Data Non-Inverted	CML-I	Input from Host	3	
3	TX2n	Transmitter Data Inverted	CML-I	Input from Host	3	
4	GND	Ground			1	
5	TX4p	Transmitter Data Non-Inverted	CML-I	Input from Host	3	
6	TX4n	Transmitter Data Inverted	CML-I	Input from Host	3	
7	GND	Ground			1	
8	TX6p	Transmitter Data Non-Inverted	CML-I	Input from Host	3	
9	TX6n	Transmitter Data Inverted	CML-I	Input from Host	3	
10	GND	Ground			1	
11	TX8p	Transmitter Data Non-Inverted	CML-I	Input from Host	3	
12	TX8n	Transmitter Data Inverted	CML-I	Input from Host	3	
13	GND	Ground			1	
14	SCL	2-wire Serial interface clock	LVCMOS-I/O	Bi-directional	3	Open-Drain with pull-up resistor on Host
15	VCC	+3.3V Power		Power from Host	2	
16	VCC	+3.3V Power		Power from Host	2	
17	LPWn/PRSn	Low-Power Mode / Module Present	Multi-Level	Bi-directional	3	See pin description for required circuit
18	GND	Ground			1	
19	RX7n	Receiver Data Inverted	CML-O	Output to Host	3	
20	RX7p	Receiver Data Non-Inverted	CML-O	Output to Host	3	
21	GND	Ground			1	
22	RX5n	Receiver Data Inverted	CML-O	Output to Host	3	
23	RX5p	Receiver Data Non-Inverted	CML-O	Output to Host	3	
24	GND	Ground			1	
25	RX3n	Receiver Data Inverted	CML-O	Output to Host	3	
26	RX3p	Receiver Data Non-Inverted	CML-O	Output to Host	3	
27	GND	Ground			1	
28	RX1n	Receiver Data Inverted	CML-O	Output to Host	3	
29	RX1p	Receiver Data Non-Inverted	CML-O	Output to Host	3	
30	GND	Ground			1	

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Pin#	Symbol	Description	Logic	Direction	Plug Sequence	Notes
31	GND	Ground			1	
32	RX2p	Receiver Data Non-Inverted	CML-O	Output to Host	3	
33	RX2n	Receiver Data Inverted	CML-O	Output to Host	3	
34	GND	Ground			1	
35	RX4p	Receiver Data Non-Inverted	CML-O	Output to Host	3	
36	RX4n	Receiver Data Inverted	CML-O	Output to Host	3	
37	GND	Ground			1	
38	RX6p	Receiver Data Non-Inverted	CML-O	Output to Host	3	
39	RX6n	Receiver Data Inverted	CML-O	Output to Host	3	
40	GND	Ground			1	
41	RX8p	Receiver Data Non-Inverted	CML-O	Output to Host	3	
42	RX8n	Receiver Data Inverted	CML-O	Output to Host	3	
43	GND	Ground			1	
44	INT/RSTn	Module Interrupt / Module Reset	Multi-Level	Bi-directional	3	See pin description for required circuit
45	VCC	+3.3V Power		Power from Host	2	
46	VCC	+3.3V Power		Power from Host	2	
47	SDA	2-wire Serial interface data	LVCMOS-I/O	Bi-directional	3	Open-Drain with pull-up resistor on Host
48	GND	Ground			1	
49	TX7n	Transmitter Data Inverted	CML-I	Input from Host	3	
50	TX7p	Transmitter Data Non-Inverted	CML-I	Input from Host	3	
51	GND	Ground			1	
52	TX5n	Transmitter Data Inverted	CML-I	Input from Host	3	
53	TX5p	Transmitter Data Non-Inverted	CML-I	Input from Host	3	
54	GND	Ground			1	
55	TX3n	Transmitter Data Inverted	CML-I	Input from Host	3	
56	TX3p	Transmitter Data Non-Inverted	CML-I	Input from Host	3	
57	GND	Ground			1	
58	TX1n	Transmitter Data Inverted	CML-I	Input from Host	3	
59	TX1p	Transmitter Data Non-Inverted	CML-I	Input from Host	3	
60	GND	Ground			1	

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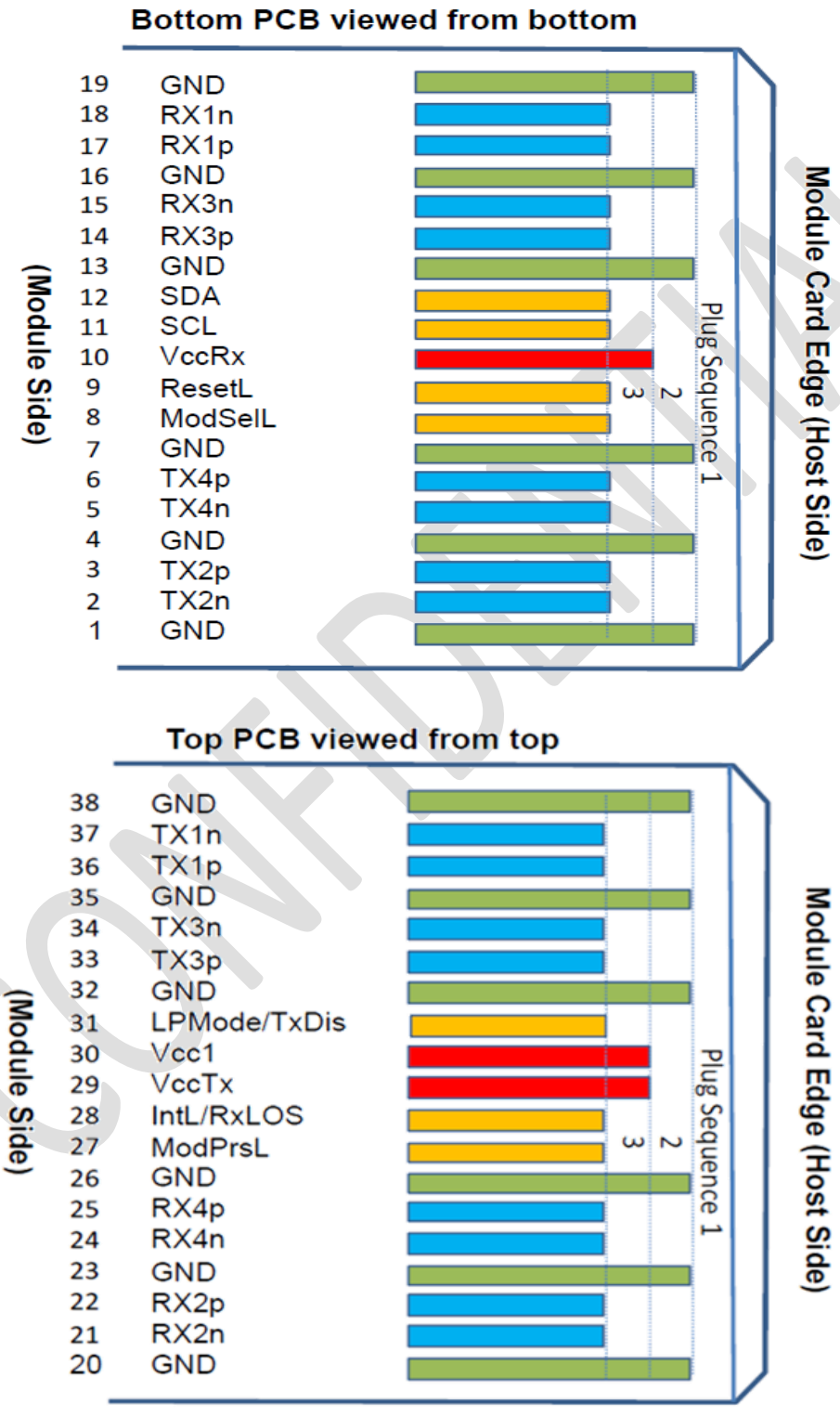
QSFP Pin Description



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Electrical Pin-out Details for QSFP

Pin	Logic	Symbol	Description	Plug Sequence	Notes
1		GND	Ground	1	1
2	CML-I	Tx2n	Transmitter Inverted Data Input	3	
3	CML-I	Tx2p	Transmitter Non-Inverted Data Input	3	
4		GND	Ground	1	1
5	CML-I	Tx4n	Transmitter Inverted Data Input	3	
6	CML-I	Tx4p	Transmitter Non-Inverted Data Input	3	
7		GND	Ground	1	1
8	LVTTL-I	ModSelL	Module Select	3	
9	LVTTL-I	ResetL	Module Reset	3	
10		Vcc Rx	+3.3V Power Supply Receiver	2	2
11	LVCMOS-I/O	SCL	2-wire serial interface clock	3	
12	LVCMOS-I/O	SDA	2-wire serial interface data	3	
13		GND	Ground	1	1
14	CML-O	Rx3p	Receiver Non-Inverted Data Output	3	
15	CML-O	Rx3n	Receiver Inverted Data Output	3	
16		GND	Ground	1	1
17	CML-O	Rx1p	Receiver Non-Inverted Data Output	3	
18	CML-O	Rx1n	Receiver Inverted Data Output	3	
19		GND	Ground	1	1
20		GND	Ground	1	1
21	CML-O	Rx2n	Receiver Inverted Data Output	3	
22	CML-O	Rx2p	Receiver Non-Inverted Data Output	3	
23		GND	Ground	1	1
24	CML-O	Rx4n	Receiver Inverted Data Output	3	
25	CML-O	Rx4p	Receiver Non-Inverted Data Output	3	
26		GND	Ground	1	1
27	LVTTL-O	ModPrsL	Module Present	3	
28	LVTTL-O	IntL	Interrupt	3	
29		Vcc Tx	+3.3V Power supply transmitter	2	2
30		Vcc1	+3.3V Power supply	2	2
31	LVTTL-I	LPMode	Low Power Mode	3	
32		GND	Ground	1	1
33	CML-I	Tx3p	Transmitter Non-Inverted Data Input	3	
34	CML-I	Tx3n	Transmitter Inverted Data Input	3	
35		GND	Ground	1	1
36	CML-I	Tx1p	Transmitter Non-Inverted Data Input	3	
37	CML-I	Tx1n	Transmitter Inverted Data Input	3	
38		GND	Ground	1	1
Note 1: GND is the symbol for signal and supply (power) common for the QSFP+ module. All are common within the QSFP+ module and all module voltages are referenced to this potential unless otherwise noted. Connect these directly to the host board signal-common ground plane.					
Note 2: Vcc Rx, Vcc1 and Vcc Tx are the receiver and transmitter power supplies and shall be applied concurrently. Requirements defined for the host side of the Host Edge Card Connector are listed in Table 6. Recommended host board power supply filtering is shown in Figures 3 and 4. Vcc Rx Vcc1 and Vcc Tx may be internally connected within the QSFP+ Module in any combination. The connector pins are each rated for a maximum current of 500 mA.					

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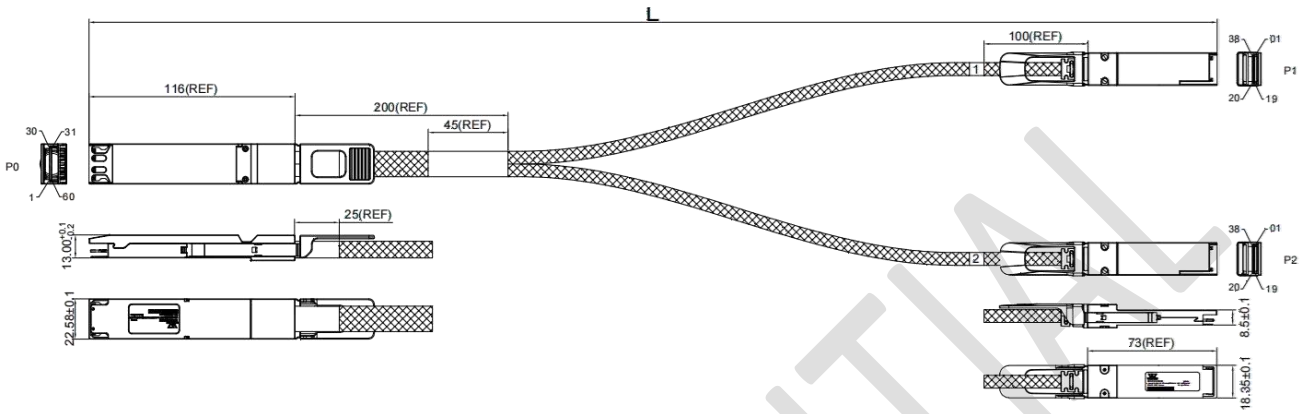
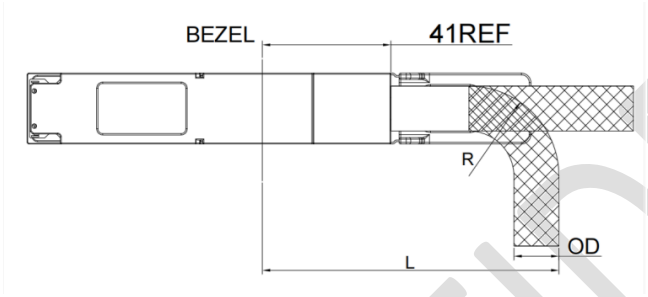
Module Memory Map

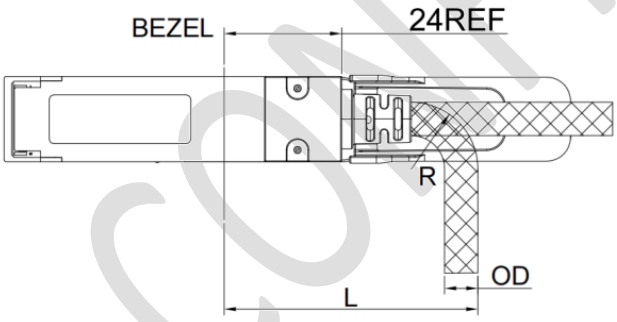
OSFP end will be compatible with CMIS rev 4.0 or further CMIS revisions and customer spec.
QSFP112 end will be compatible with SFF-8636 and customer spec.

Mechanical Dimensions





OSFP TYPE2			
GAUGE	OD	BEND RADIUS "R"	MIN. BEND RADIUS "L"
30AWG	9.5MM	19MM	60MM
28/27AWG	10.2MM	21MM	65MM



QSFP			
GAUGE	OD	BEND RADIUS "R"	MIN. BEND RADIUS "L"
30AWG	5.7MM	12MM	46MM
28/27AWG	7.0MM	14MM	50MM

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Ordering Information

Model Number	Part Number	Description
A-50H-O-2Q-030B	1190200013026	400G OSFP to 2XQSFP56 ADAC,IB HDR,HAIRTAIL, 3.0M, RED
A-50H-O-2Q-040B	1190200013028	400G OSFP to 2XQSFP56 ADAC,IB HDR,HAIRTAIL, 4.0M, RED
A-50H-O-2Q-050B	1190200013030	400G OSFP to 2XQSFP56 ADAC,IB HDR,HAIRTAIL, 5.0M, RED
A-50H-O-2Q-070B	1190200013032	400G OSFP to 2XQSFP56 ADAC,IB HDR,HAIRTAIL, 7.0M, RED

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