800G OSFP Breakout to 2xQSFP112 Hairtail+ IB NDR DAC

Features

- OSFP Module compliant to OSFP MSA
- QSFP112 Module compliant to QSFP112/QSFP-DD MSA
- Transmission data rate up to PAM4 106.25Gbps per channel
- Enable 800Gb/s to 2x400Gb/s Transmission
- Link length up to 3m
- Built-in EEPROM functions
- Operating case temperature 0°C to +70°C
- RoHS2.0 compliant

Absolute Maximum Ratings

Parameter	Symbol	Min	Typical	Max	Unit
Supply Voltage	Vcc	3.13	3.3	3.47	V
Storage temperature	Ts	-40		85	ºC
Operating Case temperature	Tc	0		70	ºC
Humidity	Rh	5		85	%
Data Rate			800		Gbps

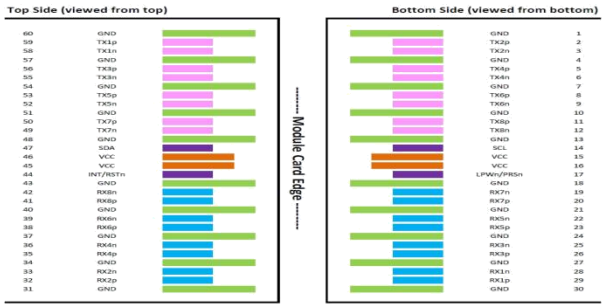
Physical Characteristics

Parameter	Symbol	Min	Typical	Max	Unit
Length	L	0.5		3.0	M
AWG		28		25	AWG
Jacket material		HAIRTAIL+ Technology Net, Sliver Gray			

Electrical Specifications

Parameter	Symbol	Min	Typical	Max		Unit
Resistance	Rcon			3		ohm
Insulation Resistance	Rins			10		Mohm
Raw cable impedance	Zca	95		110		ohm
Mated connector Impedance	Zmated	85		110		ohm
Maximum insertion loss at 26.56 GHz	SDD21	11		18	1.5M	dB
				19.75	2.0M	
				25.3	3.0M	
Differential to common-mode return loss	SCD11/22	$RLcd(f) \geq \begin{cases} 22-10(f/26.56) & 0.05 \leq f < 26.56 \\ 15-3(f/26.56) & 26.56 \leq f \leq 40 \end{cases}$ For 0.05 ≤f ≤40 GHz, Where f is the frequency in GHz				dB
Differential to common-mode conversion loss	SCD21-SDD21	$Conversion\_loss(f) - IL(f) \geq \begin{cases} 10 & 0.05 \leq f < 12.89 \\ 14-0.3108f & 12.89 \leq f \leq 40 \end{cases}$ For 0.05 ≤f ≤40 GHz, Where f is the frequency in GHz				dB
Common-mode to common-mode return loss	SCC11/22	$RLcc(f) \geq 1.8$ For 0.05 ≤f ≤40 GHz, Where f is the frequency in GHz				dB
Minimum COM	COM	3				dB

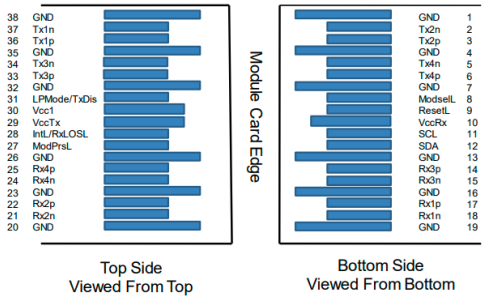
Pin Description



Electrical Pin-out Details for OSFP

Pin#	Symbol	Description	Logic	Direction	Plug Sequence	Notes
1	GND	Ground			1	
2	TX2p	Transmitter Data Non-Inverted	CML-I	Input from Host	3	
3	TX2n	Transmitter Data Inverted	CML-I	Input from Host	3	
4	GND	Ground			1	
5	TX4p	Transmitter Data Non-Inverted	CML-I	Input from Host	3	
6	TX4n	Transmitter Data Inverted	CML-I	Input from Host	3	
7	GND	Ground			1	
8	TX6p	Transmitter Data Non-Inverted	CML-I	Input from Host	3	
9	TX6n	Transmitter Data Inverted	CML-I	Input from Host	3	
10	GND	Ground			1	
11	TX8p	Transmitter Data Non-Inverted	CML-I	Input from Host	3	
12	TX8n	Transmitter Data Inverted	CML-I	Input from Host	3	
13	GND	Ground			1	
14	SCL	2-wire Serial interface clock	LVCMOS-I/O	Bi-directional	3	Open-Drain with pull-up resistor on Host
15	VCC	+3.3V Power		Power from Host	2	
16	VCC	+3.3V Power		Power from Host	2	
17	LPWn/PRSn	Low-Power Mode / Module Present	Multi-Level	Bi-directional	3	See pin description for required circuit
18	GND	Ground			1	
19	RX7n	Receiver Data Inverted	CML-O	Output to Host	3	
20	RX7p	Receiver Data Non-Inverted	CML-O	Output to Host	3	
21	GND	Ground			1	
22	RX5n	Receiver Data Inverted	CML-O	Output to Host	3	
23	RX5p	Receiver Data Non-Inverted	CML-O	Output to Host	3	
24	GND	Ground			1	
25	RX3n	Receiver Data Inverted	CML-O	Output to Host	3	
26	RX3p	Receiver Data Non-Inverted	CML-O	Output to Host	3	
27	GND	Ground			1	
28	RX1n	Receiver Data Inverted	CML-O	Output to Host	3	
29	RX1p	Receiver Data Non-Inverted	CML-O	Output to Host	3	
30	GND	Ground			1	

Pin#	Symbol	Description	Logic	Direction	Plug Sequence	Notes
31	GND	Ground			1	
32	RX2p	Receiver Data Non-Inverted	CML-O	Output to Host	3	
33	RX2n	Receiver Data Inverted	CML-O	Output to Host	3	
34	GND	Ground			1	
35	RX4p	Receiver Data Non-Inverted	CML-O	Output to Host	3	
36	RX4n	Receiver Data Inverted	CML-O	Output to Host	3	
37	GND	Ground			1	
38	RX6p	Receiver Data Non-Inverted	CML-O	Output to Host	3	
39	RX6n	Receiver Data Inverted	CML-O	Output to Host	3	
40	GND	Ground			1	
41	RX8p	Receiver Data Non-Inverted	CML-O	Output to Host	3	
42	RX8n	Receiver Data Inverted	CML-O	Output to Host	3	
43	GND	Ground			1	
44	INT/RSTn	Module Interrupt / Module Reset	Multi-Level	Bi-directional	3	See pin description for required circuit
45	VCC	+3.3V Power		Power from Host	2	
46	VCC	+3.3V Power		Power from Host	2	
47	SDA	2-wire Serial interface data	LVCMOS-I/O	Bi-directional	3	Open-Drain with pull-up resistor on Host
48	GND	Ground			1	
49	TX7n	Transmitter Data Inverted	CML-I	Input from Host	3	
50	TX7p	Transmitter Data Non-Inverted	CML-I	Input from Host	3	
51	GND	Ground			1	
52	TX5n	Transmitter Data Inverted	CML-I	Input from Host	3	
53	TX5p	Transmitter Data Non-Inverted	CML-I	Input from Host	3	
54	GND	Ground			1	
55	TX3n	Transmitter Data Inverted	CML-I	Input from Host	3	
56	TX3p	Transmitter Data Non-Inverted	CML-I	Input from Host	3	
57	GND	Ground			1	
58	TX1n	Transmitter Data Inverted	CML-I	Input from Host	3	
59	TX1p	Transmitter Data Non-Inverted	CML-I	Input from Host	3	
60	GND	Ground			1	



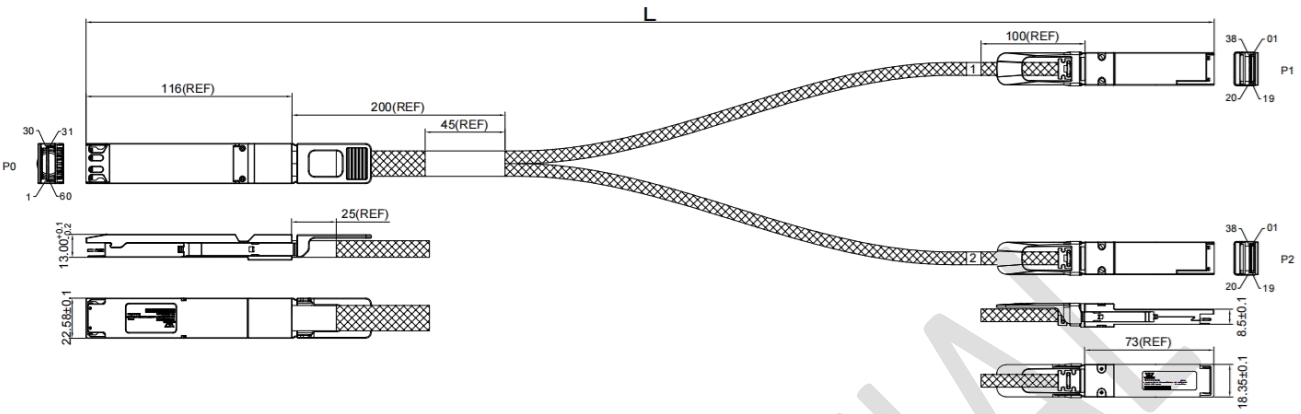
Electrical Pin-out Details for QSFP112

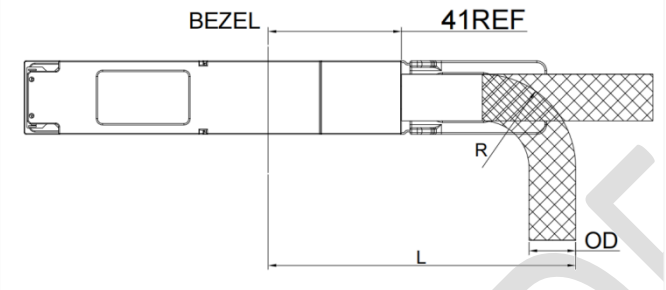
Pin	Logic	Symbol	Description	Plug Sequence	Notes
1		GND	Ground	1	1
2	CML-I	Tx2n	Transmitter Inverted Data Input	3	
3	CML-I	Tx2p	Transmitter Non-Inverted Data Input	3	
4		GND	Ground	1	1
5	CML-I	Tx4n	Transmitter Inverted Data Input	3	
6	CML-I	Tx4p	Transmitter Non-Inverted Data Input	3	
7		GND	Ground	1	1
8	LVTTL-I	ModSelL	Module Select	3	
9	LVTTL-I	ResetL	Module Reset	3	
10		Vcc Rx	+3.3V Power Supply Receiver	2	2
11	LVCMOS-I/O	SCL	2-wire serial interface clock	3	
12	LVCMOS-I/O	SDA	2-wire serial interface data	3	
13		GND	Ground	1	1
14	CML-O	Rx3p	Receiver Non-Inverted Data Output	3	
15	CML-O	Rx3n	Receiver Inverted Data Output	3	
16		GND	Ground	1	1
17	CML-O	Rx1p	Receiver Non-Inverted Data Output	3	
18	CML-O	Rx1n	Receiver Inverted Data Output	3	
19		GND	Ground	1	1
20		GND	Ground	1	1
21	CML-O	Rx2n	Receiver Inverted Data Output	3	
22	CML-O	Rx2p	Receiver Non-Inverted Data Output	3	
23		GND	Ground	1	1
24	CML-O	Rx4n	Receiver Inverted Data Output	3	
25	CML-O	Rx4p	Receiver Non-Inverted Data Output	3	
26		GND	Ground	1	1
27	LVTTL-O	ModPrsL	Module Present	3	
28	LVTTL-O	IntL	Interrupt	3	
29		Vcc Tx	+3.3V Power supply transmitter	2	2
30		Vcc1	+3.3V Power supply	2	2
31	LVTTL-I	LPMode	Low Power Mode	3	
32		GND	Ground	1	1
33	CML-I	Tx3p	Transmitter Non-Inverted Data Input	3	
34	CML-I	Tx3n	Transmitter Inverted Data Input	3	
35		GND	Ground	1	1
36	CML-I	Tx1p	Transmitter Non-Inverted Data Input	3	
37	CML-I	Tx1n	Transmitter Inverted Data Input	3	
38		GND	Ground	1	1

Note 1: GND is the symbol for signal and supply (power) common for the QSFP+ module. All are common within the QSFP+ module and all module voltages are referenced to this potential unless otherwise noted. Connect these directly to the host board signal-common ground plane.

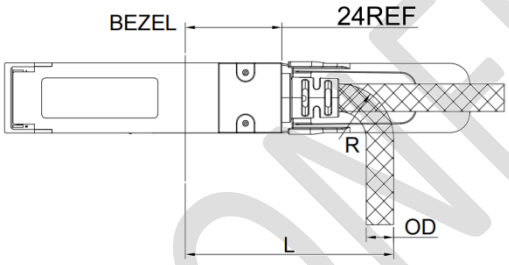
Note 2: Vcc Rx, Vcc1 and Vcc Tx are the receiver and transmitter power supplies and shall be applied concurrently. Requirements defined for the host side of the Host Edge Card Connector are listed in Table 6. Recommended host board power supply filtering is shown in Figures 3 and 4. Vcc Rx Vcc1 and Vcc Tx may be internally connected within the QSFP+ Module in any combination. The connector pins are each rated for a maximum current of 500 mA.

Mechanical Dimensions





800G OSFP			
GAUGE	OD	BEND RADIUS "R"	MIN. BEND RADIUS "L"
28AWG	10.2MM	21MM	65MM
26/25AWG	12.1MM	25MM	70MM



QSFP112			
GAUGE	OD	BEND RADIUS "R"	MIN. BEND RADIUS "L"
28AWG	7.0MM	14MM	50MM
26/25AWG	8.3MM	17MM	55MM

Ordering Information

Model Number	Part Number	Description
P-100N-O-2Q-005B	1190200004021	800G OSFP to 2xQSFP112 DAC, 28AWG, 0.5m, Hairtail+, Sliver Gray.
P-100N-O-2Q-010B	1190200003022	800G OSFP to 2xQSFP112 DAC, 28AWG, 1.0m, Hairtail+, Sliver Gray.
P-100N-O-2Q-015B	1190200004023	800G OSFP to 2xQSFP112 DAC, 26/25AWG, 1.5m, Hairtail+, Sliver Gray.
P-100N-O-2Q-020B	1190200004024	800G OSFP to 2xQSFP112 DAC, 26/25AWG, 2.0m, Hairtail+, Sliver Gray.
P-100N-O-2Q-025B	1190200004025	800G OSFP to 2xQSFP112 DAC, 25AWG, 1.5m, Hairtail+, Sliver Gray.
P-100N-O-2Q-030B	1190200004026	800G OSFP to 2xQSFP112 DAC, 25AWG, 2.0m, Hairtail+, Sliver Gray.

References

1. OSFP MSA Rev5.0
2. IB NDR&IEEE802.3ck
3. QSFP112 MSA Rev2.0
4. SFF-8636
5. QSFP-DD MSA Rev6.3
6. Common Management Interface Specification(CMIS) Rev5.0

Revision Records

REV.	Description	Designed	Checked	Approved	Issue Date
X1	NEW	XICHUN TAN	XICHUN TAN	RANY LEI	2023.10.16