Industrial

DDR3L UDIMM

Datasheet

廣 穎 電 通 股 份 有 限 公 司
Silicon Power Computer & Communications Inc.
TEL: 886-2 8797-8833 FAX: 886-2 8751-6595
台北市114內湖區洲子街106號7樓
7F, No.106, ZHO-Z ST. NEIHU DIST, 114, TAIPEI, TAIWAN,

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Revision History

Revision No.	Date	Remarks
1.0	2016/10/18	First release
1.1	2017/12	Modify description.
1.2	2018/3	Add 256Mx8 Single Rank.
1.3	2018/7	Add VLU Series(VLP-UDIMM) & LLE Series(UDIMM w/ECC)

Description

The Silicon Power Computer & Communications industrial DDR3L LLU/VLU series products are 240-Pin Double Data Rate 3 (DDR3) Synchronous DRAM Unbuffered Dual In-Line Memory Module (UDIMM), organized as a one rank 512Mx64, high-speed memory array or two ranks 1024Mx64 high-speed memory array, The module uses eight 256Mx8 (2GB), 512Mx8 (4GB), sixteen 512Mx8 (8GB) DDR3 SDRAMs in BGA packages

The Silicon Power Computer & Communications LLE series products are 240-Pin Double Data Rate 3 (DDR3) Synchronous DRAM Unbuffered Dual In-Line Memory Module (UDIMM), organized as a one rank 512Mx72, high-speed memory array or two ranks 1024Mx72 high-speed memory array, The module uses nine 512Mx8 (4GB), eighteen 512Mx8 (8GB) DDR3 SDRAMs in BGA packages

This DIMM are manufactured using raw cards developed for broad industry use as reference designs. The use of these common design files minimizes electrical variation between suppliers.

DDR3 SDRAM DIMM provide a high-performance, flexible 8-byte interface in a 5.25” long space-saving footprint.

The DIMM is intended for use in applications operating of 800MHz clock speeds and achieves high-speed data transfer rates of 1600Mbps. Prior to any access operation, the device CAS latency and burst/length/operation type must be programmed into the DIMM by address inputs A0-A13(128Mx8 or 128Mx16), A0-A14(256Mx8 or 256Mx16), A0-A15 (512Mx8) and I/O inputs BA0~BA2 using the mode register set cycle.

The DIMM uses serial presence-detect implemented via a serial EEPROM using a standard IIC protocol.

Features

• DDR3(L) functionality and operations supported as defined in the component data sheet
•LLU Series:
240pin, unbuffered dual in-line memory module (UDIMM)
2GB (256 Meg x 64), 4GB (512Meg x 64), 8GB (1Giga x 64)
•VLU Series:
240pin, very low profile unbuffered dual in-line memory module (VLP-UDIMM)
4GB (512Meg x 64), 8GB (1Giga x 64)
•LLE Serier
240pin, unbuffered dual in-line memory module (UDIMM w/ECC)
4GB (512Meg x 72), 8GB (1Giga x 72)
• Fast data transfer rates:
DDR3L-1600(PC3L-12800)
• Single or Dual rank
• DDR3L Low Power V_{DD} = V_{DDQ} =1.35V (+0.1~-0.067V)
• V_{DDSPD} = 3.0V to 3.6V
• Reset pin for improved system stability
• Nominal and dynamic on-die termination (ODT) for data, strobe, and mask signals
• Fixed burst chop (BC) of 4 and burst length (BL) of 8 via the mode register set (MRS)
• Fly-by topology
• Terminated control, command, and address bus
• Adjustable data-output drive strength
• Serial presence-detect (SPD) EEPROM
• Gold edge contacts
• Pb-free

DDR3L Industrial UDIMM LLU Series Module Specification

Part Number	Module Density & Configuration	Bandwidth	Data Rate	Timing (tCL-tRCD-tRP)	Operator Voltage
SP002GILLU160VS0	2GB (256Mx64) 256Mx8 1Rank	PC3L-12800	DDR3L-1600	11-11-11	1.35V
SP002GILLU160WH0	2GB (256Mx64) 256Mx16 1Rank	PC3L-12800	DDR3L-1600	11-11-11	1.35V
SP004GILLU160NH0	4GB (512Mx64) 512Mx8 1Rank	PC3L-12800	DDR3L-1600	11-11-11	1.35V
SP008GILLU160NH0	8GB (1Gx64) 512Mx8 2Ranks	PC3L-12800	DDR3L-1600	11-11-11	1.35V

DDR3L Industrial VLP-UDIMM VLU Series Module Specification

Part Number	Module Density & Configuration	Bandwidth	Data Rate	Timing (tCL-tRCD-tRP)	Operator Voltage
SP004GIVLU160NH0	4GB (512Mx64) 512Mx8 1Rank	PC3L-12800	DDR3L-1600	11-11-11	1.35V
SP008GIVLU160NH0	8GB (1Gx64) 512Mx8 2Ranks	PC3L-12800	DDR3L-1600	11-11-11	1.35V

DDR3L Industrial ECC-UDIMM LLE Series Module Specification

Part Number	Module Density & Configuration	Bandwidth	Data Rate	Timing (tCL-tRCD-tRP)	Operator Voltage
SP004GILLE160NH0	4GB (512Mx72) 512Mx8 1Rank	PC3L-12800	DDR3L-1600	11-11-11	1.35V
SP008GILLE160NH0	8GB (1Gx72) 512Mx8 2Ranks	PC3L-12800	DDR3L-1600	11-11-11	1.35V

Pin Assignments

240-Pin UDIMM Front							
Pin	Symbol	Pin	Symbol	Pin	Symbol	Pin	Symbol
1	V_{REFDQ}	31	DQ25	61	A2	91	DQ41
2	V_{SS}	32	V_{SS}	62	V_{DD}	92	V_{SS}
3	DQ0	33	DQS3#	63	CK1	93	DQS5#
4	DQ1	34	DQS3	64	CK1#	94	DQS5
5	V_{SS}	35	V_{SS}	65	V_{DD}	95	V_{SS}
6	DQS0#	36	DQ26	66	V_{DD}	96	DQ42
7	DQS0	37	DQ27	67	V_{REFCA}	97	DQ43
8	V_{SS}	38	V_{SS}	68	NC	98	V_{SS}
9	DQ2	39	CB0	69	V_{DD}	99	DQ48
10	DQ3	40	CB1	70	A10	100	DQ49
11	V_{SS}	41	V_{SS}	71	BA0	101	V_{SS}
12	DQ8	42	DQS8#	72	V_{DD}	102	DQS6#
13	DQ9	43	DQS8	73	WE#	103	DQS6
14	V_{SS}	44	Vss	74	CAS#	104	V_{SS}
15	DQS1#	45	CB2	75	V_{DD}	105	DQ50
16	DQS1	46	CB3	76	S1#	106	DQ51
17	VSS	47	V_{SS}	77	ODT1	107	V_{SS}
18	DQ10	48	NC	78	V_{DD}	108	DQ56
19	DQ11	49	NC	79	NC	109	DQ57
20	V_{SS}	50	CKE0	80	VSS	110	VSS
21	DQ16	51	V_{DD}	81	DQ32	111	DQS7#
22	DQ17	52	BA2	82	DQ33	112	DQS7
23	V_{SS}	53	NC	83	VSS	113	V_{SS}
24	DQS2#	54	V_{DD}	84	DQS4#	114	DQ58
25	DQS2	55	A11	85	DQS4	115	DQ59
26	V_{SS}	56	A7	86	V_{SS}	116	V_{SS}
27	DQ18	57	V_{DD}	87	DQ34	117	SA0
28	DQ19	58	A5	88	DQ35	118	SCL
29	V_{SS}	59	A4	89	V_{SS}	119	SA2
30	DQ24	60	V_{DD}	90	DQ40	120	V_{TT}

240-Pin UDIMM Back							
Pin	Symbol	Pin	Symbol	Pin	Symbol	Pin	Symbol
121	V_{SS}	151	V_{SS}	181	A1	211	V_{SS}
122	DQ4	152	DM3	182	V_{DD}	212	DM5
123	DQ5	153	NC	183	V_{DD}	213	NC
124	V_{SS}	154	V_{SS}	184	CK0	214	V_{SS}
125	DM0	155	DQ30	185	CK0#	215	DQ46
126	NC	156	DQ31	186	V_{DD}	216	DQ47
127	V_{SS}	157	V_{SS}	187	EVENT#	217	V_{SS}
128	DQ6	158	CB4	188	A0	218	DQ52
129	DQ7	159	CB5	189	V_{DD}	219	DQ53
130	V_{SS}	160	Vss	190	BA1	220	V_{SS}
131	DQ12	161	DM8	191	V_{DD}	221	DM6
132	DQ13	162	NC	192	RAS#	222	NC
133	V_{SS}	163	Vss	193	S0#	223	V_{SS}
134	DM1	164	CB6	194	V_{DD}	224	DQ54
135	NC	165	CB7	195	ODT0	225	DQ55
136	V_{SS}	166	V_{SS}	196	A13	226	V_{SS}
137	DQ14	167	NC	197	V_{DD}	227	DQ60
138	DQ15	168	RESET#	198	NC	228	DQ61
139	V_{SS}	169	CKE1	199	V_{SS}	229	V_{SS}
140	DQ20	170	V_{DD}	200	DQ36	230	DM7
141	DQ21	171	NC	201	DQ37	231	NC
142	V_{SS}	172	NC/A14	202	V_{SS}	232	V_{SS}
143	DM2	173	V_{DD}	203	DM4	233	DQ62
144	NC	174	A12	204	NC	234	DQ63
145	V_{SS}	175	A9	205	V_{SS}	235	V_{SS}
146	DQ22	176	V_{DD}	206	DQ38	236	V_{DDSPD}
147	DQ23	177	A8	207	DQ39	237	SA1
148	V_{SS}	178	A6	208	V_{SS}	238	SDA
149	DQ28	179	V_{DD}	209	DQ44	239	V_{SS}
150	DQ29	180	A3	210	DQ45	240	V_{TT}

Pin Description

Symbol	Type	Description
A0–A14	Input	**Address inputs:** Provide the row address for ACTIVE commands and the column address and auto precharge bit for READ/WRITE commands to select one location out of the memory array in the respective bank. A10 is sampled during a PRECHARGE command to determine whether the PRECHARGE applies to one bank (A10 LOW) or all banks (A10 HIGH). If only one bank is to be precharged, the bank is selected by BA. A12 is sampled during READ and WRITE commands to determine if burst chop (on-the-fly) will be performed. The address inputs also provide the opcode during mode register command set. A0–A13 (128Mx8) A0–A14 (256Mx8).
BA0–BA2	Input	**Bank address inputs:** BA0, BA1 define to which device bank an ACTIVE, READ, WRITE, orPRECHARGE command is being applied. BA0, BA1 define which mode register, including MR, EMR, EMR(2), and EMR(3), is loaded during the LOAD MODE command.
CK0, CK0#, CK1, CK1#	Input	**Clock:** CK and CK# are differential clock inputs. All address and control input signals are sampled on the crossing of the positive edge of CK and negative edge of CK#. Output data (DQs and DQS/DQS#) is referenced to the crossings of CK and CK#.
CKE0, CKE1	Input	**Clock enable:** CKE (registered HIGH) activates and CKE (registered LOW) deactivates clocking circuitry on the DDR3 SDRAM.
DM0–DM8	Input	**Data input mask:** DM is an input mask signal for write data. Input data is masked when DM issampled HIGH, along with that input data, during a write access. DM is sampled on both edges of DQS. Although DM pins are input-only, the DM loading is designed to match that of DQ and DQS7pins.
ODT0 ODT1	Input	**On-die termination:** ODT (registered HIGH) enables termination resistance internal to the DDR3 SDRAM. When enabled, ODT is only applied to the following pins: DQ, DQS, DQS# and DM. The ODT input will be ignored if disabled via the LOAD MODE command.
RAS#, CAS#, WE#	Input	**Command inputs:** RAS#, CAS#, and WE# (along with S#) define the command being entered.
RESET#	Input (LVCMOS)	**Reset:** RESET# is an active LOW CMOS input referenced to V_{SS}. The RESET# input receiver is a CMOS input defined as a rail-to-rail signal with DC HIGH ≥ 0.8 ×V_{DD} and DC LOW ≤ 0.2 ×V_{DD}.
S0#, S1#	Input	**Chip select:** S# enables (registered LOW) and disables (registered HIGH) the command decoder.
SA[2:0]	Input	**Presence-detect address inputs:** These pins are used to configure the SPD EEPROM address range.
SCL	Input	**Serial clock for presence-detect:** SCL is used to synchronize the presence-detect data transfer to and from the module.
EVENT#	Output (open-drain)	**Temperature event:** The EVENT# pin is asserted by the temperature sensor when critical temperature thresholds have been exceeded.
CB[7:0]	I/O	**Check bits:** Data used for ECC.
DQ0–DQ63	I/O	**Data input/output:** Bidirectional data bus.
DQS0–DQS7 DQS0#–DQS7#	I/O	**Data strobe:** Output with read data, input with write data for source synchronous operation. Edge-aligned with read data, center-aligned with write data.
SDA	I/O	**Serial presence-detect data:** SDA is a bidirectional pin used to transfer addresses and data into and out of the SPD EEPROM on the module.
V_{DD}	Supply	**Power supply:** 1.5V ±0.075V. The component V_{DD} and V_{DDQ} are connected to the module V_{DD}.
V_{DDSPD}	Supply	**Temperature sensor/SPD EEPROM power supply:** +3.0V to +3.6V.
V_{REFCA}	Supply	**Reference voltage:** Control, command, and address (V_{DD}/2).
V_{REFDQ}	Supply	**Reference voltage:** DQ, DM (V_{DD}/2).
V_{SS}	Supply	Ground.
V_{TT}	Supply	**Termination voltage:** Used for control, command, and address (V_{DD}/2).
NC	–	**No connect:** These pins are not connected on the module.
NU	–	**Not used:** These pins are not used in specific module configuration/operations.

Environmental Requirements

Symbol	Parameter	Rating	Units	Note
T_{OPR}	Module Operating Temperature Range (ambient)	0 to 55	°C	3
H_{OPR}	Operating Humidity (relative)	10 to 90	%	1
T_{STG}	Storage Temperature (Plastic)	-55 to 100	°C	1
H_{STG}	Storage Humidity (without condensation)	5 to 95	%	1
P_{BAR}	Barometric Pressure (operating & storage)	105 to 69	K Pascal	1, 2

Note:
1. Stresses greater than those listed may cause permanent damage to the device. This is a stress rating only and device functional operation at or above the conditions indicated is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability.
2. Up to 9850 ft.
3. The component maximum case temperature shall not exceed the value specified in the component spec.

Absolute Maximum DC Ratings

Symbol	Parameter	Rating	Units	Note
V_{DD}	Voltage on V_{DD} pins relative to V_{SS}	-0.4 V ~ 1.975 V	V	1, 3
V_{DDQ}	Voltage on V_{DDQ} pins relative to V_{SS}	-0.4 V ~ 1.975 V	V	1, 3
V_{IN}, V_{OUT}	Voltage on I/O pins relative to V_{SS}	-0.4 V ~ 1.975 V	V	1
T_{STG}	Storage Temperature	-55 to +100	°C	1, 2

Note:
1. Stresses greater than those listed under “Absolute Maximum Ratings” may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability.
2. Storage Temperature is the case surface temperature on the center/top side of the DRAM.
3. V_{DD} and V_{DDQ} must be within 300 mV of each other at all times; and V_{REF} must be not greater

Operating temperature Conditions

Symbol	Parameter	Rating	Units	Note
T_{OPER}	Normal Operating Temperature Range	0 to 85	°C	1, 2
	Extended Temperature Range (Optional)	85 to 95	°C	1, 3

Note:

1. Operating Temperature T_{OPER} is the case surface temperature on the center / top side of the DRAM.
2. The Normal Temperature Range specifies the temperatures where all DRAM specifications will be supported. During operation, the DRAM case temperature must be maintained between 0 to 85 °C under all operating conditions
3. Some applications require operation of the DRAM in the Extended Temperature Range between 85 °C and 95 °C case temperature. Full specifications are supported in this range, but the following additional conditions apply:
   a) Refresh commands must be doubled in frequency, therefore reducing the Refresh interval tREFI to 3.9 µs. It is also possible to specify a component with 1X refresh (tREFI to 7.8µs) in the Extended Temperature Range. Please refer to supplier data sheet and/or the DIMM SPD for option availability.
   b) If Self-Refresh operation is required in the Extended Temperature Range, then it is mandatory to either use the Manual Self-Refresh mode with Extended Temperature Range capability (MR2 A6 = 0b and MR2 A7 = 1b) or enable the optional Auto Self-Refresh mode(MR2 A6 = 1b and MR2 A7 = 0b). Please refer to the supplier data sheet and/or the DIMM SPD for Auto Self-Refresh option availability, Extended Temperature Range support and tREFI requirements in the Extended Temperature Range.

DC Electrical Characteristics and Operating Conditions

Symbol	Parameter	Min	Typ	Max	Units	Notes
V_{DD}	Supply Voltage	1.283	1.35	1.45	V	1,2
V_{DDQ}	Output Supply Voltage	1.283	1.35	1.45	V	1,2

Note:

1. Under all conditions V_{DDQ} must be less than or equal to V_{DD}.
2. V_{DDQ} tracks with V_{DD}. AC parameters are measured with V_{DD} and V_{DDQ} tied together.

Single-Ended AC and DC Input Levels for Command and Address

Symbol	Parameter	DDR3-1066		DDR3-1333/DDR3-1600		Units	Note
		Min.	Max.	Min.	Max.		
VIH.CA(DC)	DC Input Logic High	Vref + 0.100	VDD	Vref + 0.100	VDD	V	1
VIL.CA(DC)	DC Input Logic Low	VSS	Vref - 0.100	VSS	Vref - 0.100	V	1
VIH.CA(AC)	AC Input Logic High	Vref + 0.175	Note 2	Vref + 0.175	Note 2	V	1, 2
VIL.CA(AC)	AC Input Logic Low	Note 2	Vref - 0.175	Note 2	Vref - 0.175	V	1, 2
VIH.CA(AC150)	AC Input Logic High	-	-	Vref + 0.15	Note 2	V	1, 2
VIL.CA(AC150)	AC Input Logic Low	-	-	Note 2	Vref - 0.15	V	1, 2
VRefCA(DC)	Reference Voltage for ADD, CMD Inputs	0.49 x VDD	0.51 x VDD	0.49 x VDD	0.51 x VDD	V	3, 4

Note:

1. For input only pins except . Vref = VrefCA(DC).
2. See “Overshoot and Undershoot Specifications” in the device datasheet.
3. The ac peak noise on VRef may not allow VRef to deviate from VRefDQ(DC) by more than +/-1% VDD (for reference: approx. +/- 15 mV).
4. For reference: approx. VDD/2 +/- 15 mV.

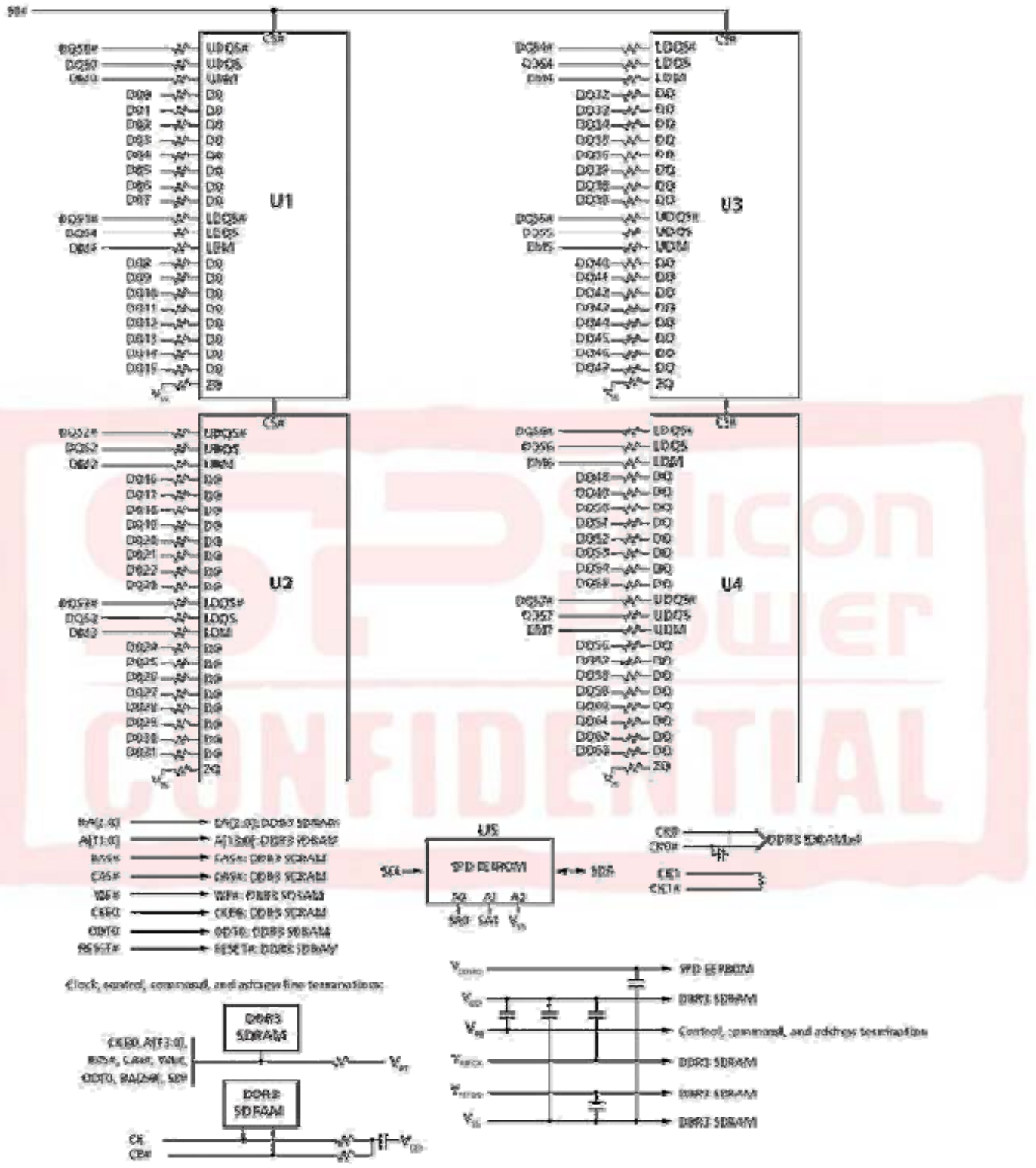
Single-Ended AC and DC Input Levels for DQ and DM

Symbol	Parameter	DDR3-1066		DDR3-1333/DDR3-1600		Units	Note
		Min.	Max.	Min.	Max.		
VIH.DQ(DC)	DC Input Logic High	Vref + 0.100	VDD	Vref + 0.100	VDD	V	1
VIL.DQ(DC)	DC Input Logic Low	VSS	Vref - 0.100	VSS	Vref - 0.100	V	1
VIH.DQ(AC)	AC Input Logic High	Vref + 0.175	Note 2	Vref + 0.15	Note 2	V	1, 2, 5
VIL.DQ(AC)	AC Input Logic Low	Note 2	Vref - 0.175	Note 2	Vref - 0.15	V	1, 2, 5
VRefDQ(DC)	Reference Voltage for DQ, DM Inputs	0.49 x VDD	0.51 x VDD	0.49 x VDD	0.51 x VDD	V	3, 4

Note: 1. For input only pins except. Vref = VrefDQ(DC).

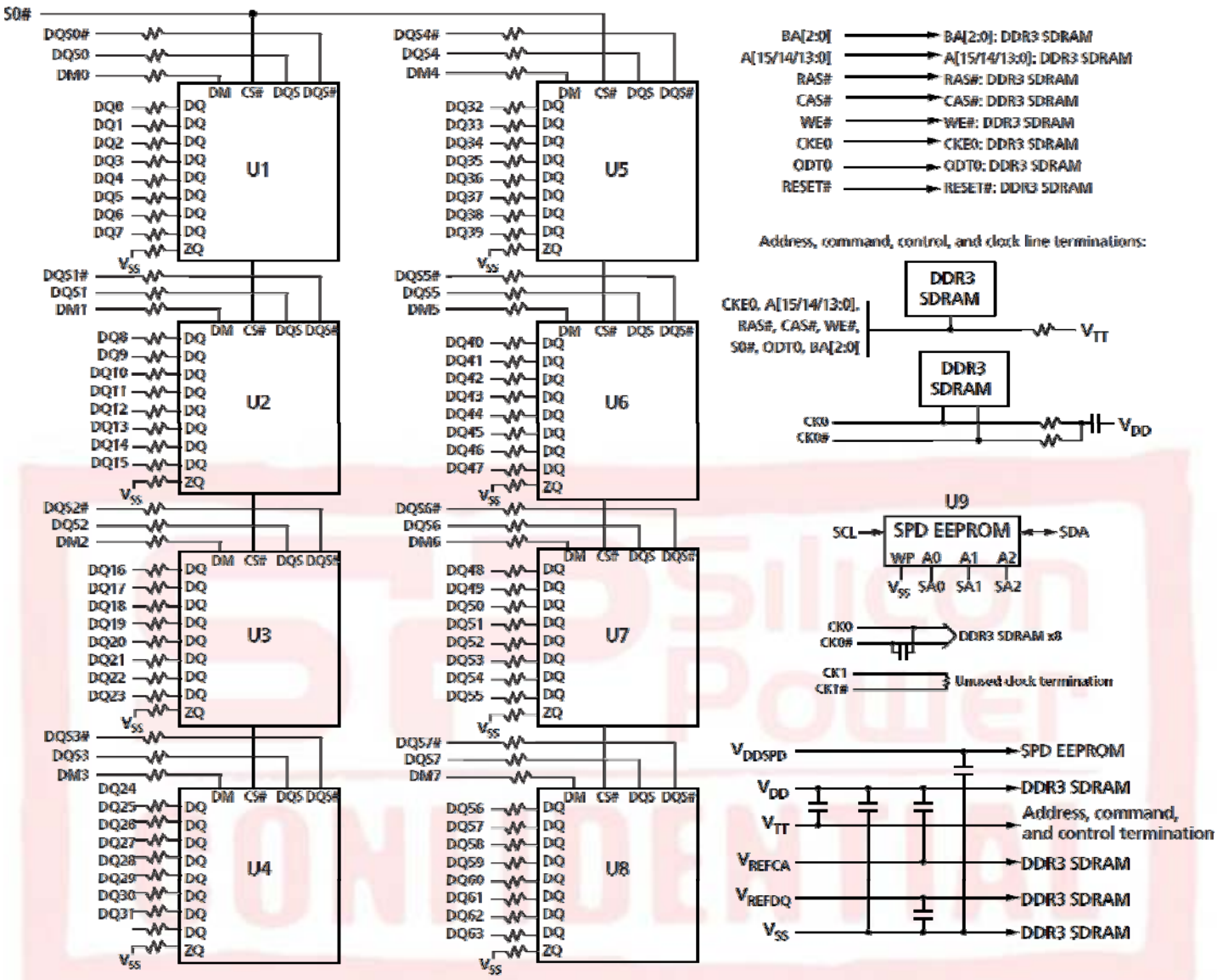
2. See “Overshoot and Undershoot Specifications” in the device datasheet.
3. The ac peak noise on VRef may not allow VRef to deviate from VRefDQ(DC) by more than +/-1% VDD (for reference: approx. +/- 15 mV).
4. For reference: approx. VDD/2 +/- 15 mV.
5. Single-ended swing requirement for DQS, DQS# is 350 mV (peak to peak). Differential swing requirement for DQS - DQS# is 700 mV(peak to peak).

Block Diagram (64bits x16 1Rank)



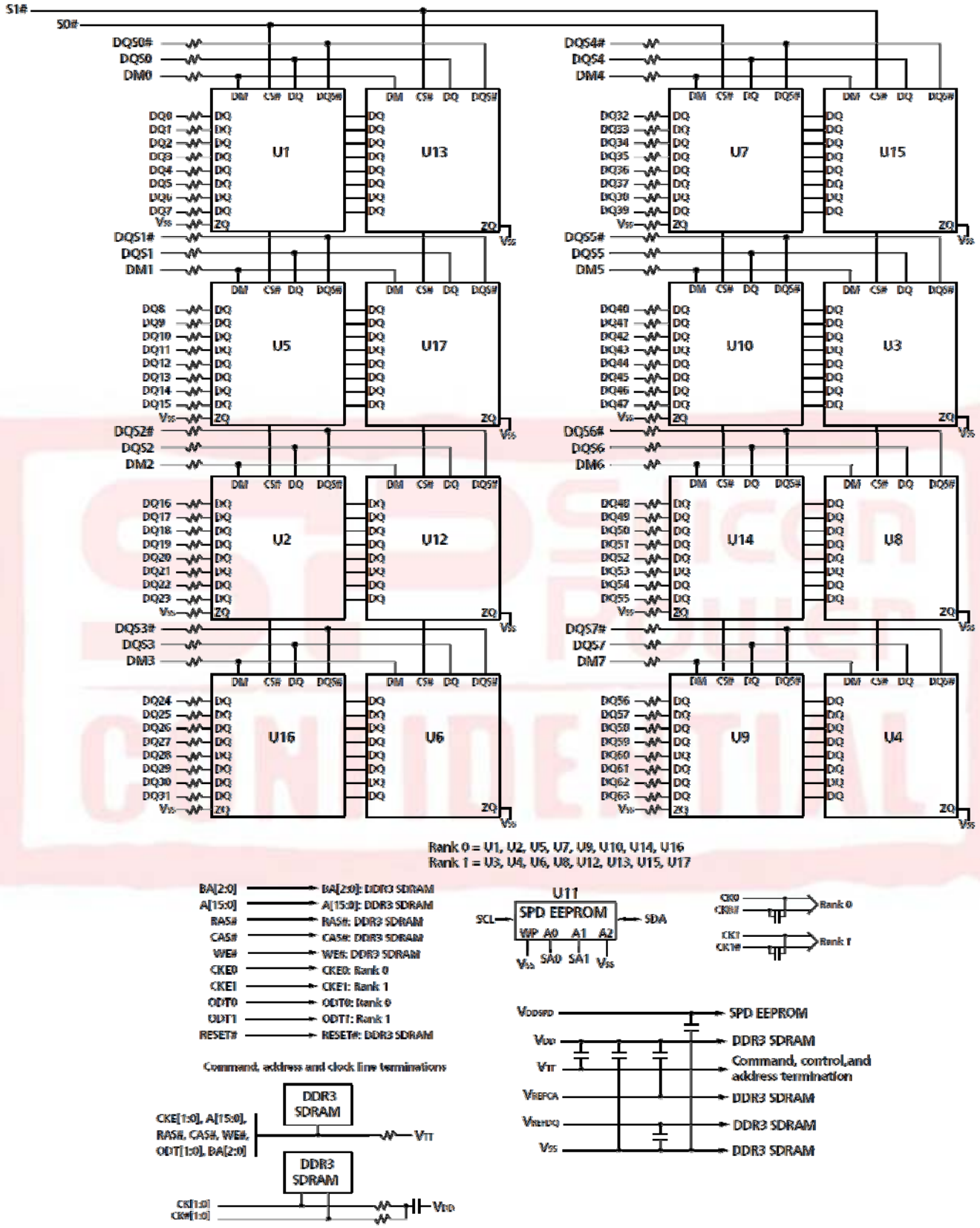
Note: The ZQ ball on each DDR3 component is connected to an external 240Ω resistor that is tied to ground. It is used for the calibration of the component's ODT and output driver.

Block Diagram (64bits x8 1Rank)



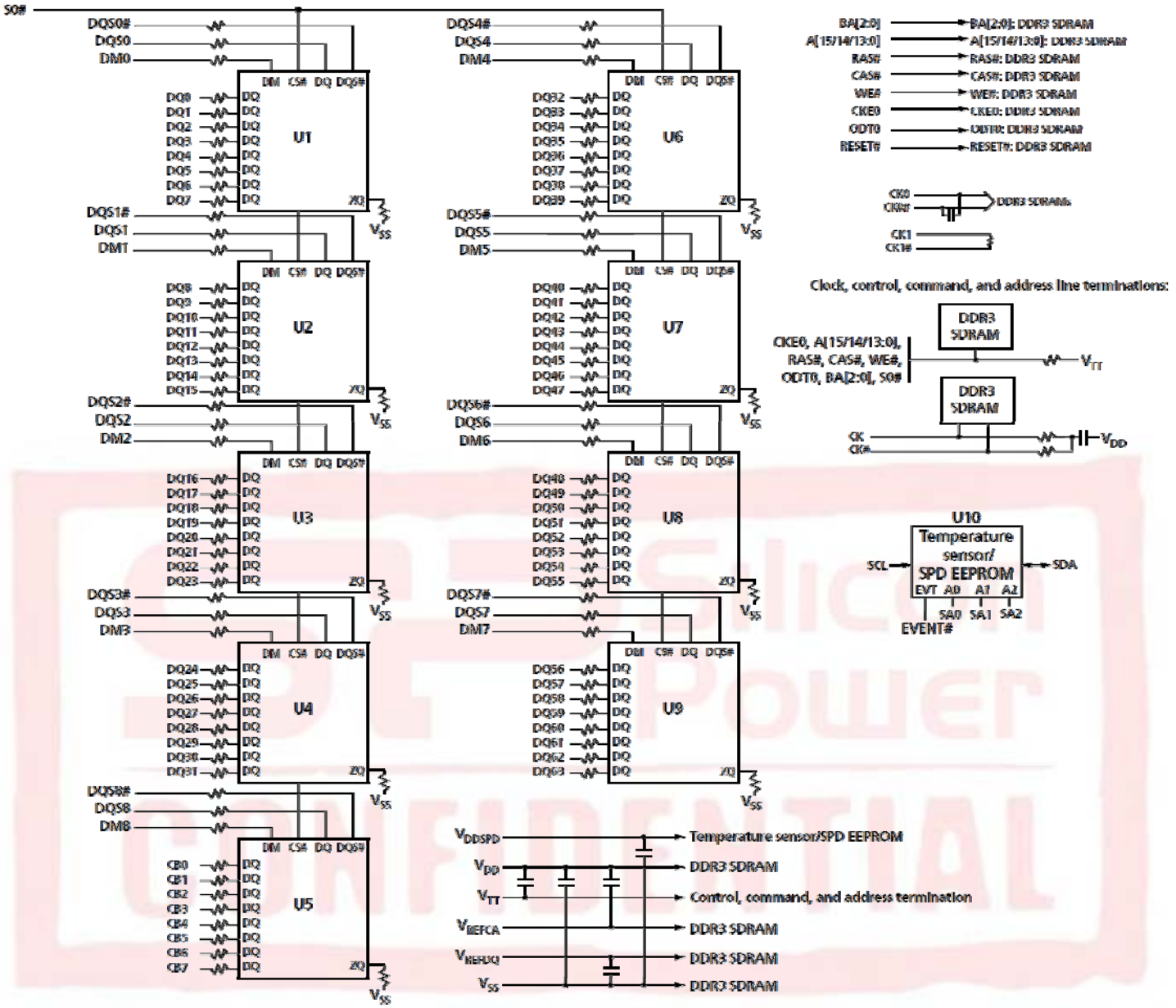
Note: The ZQ ball on each DDR3 component is connected to an external 240Ω resistor that is tied to ground. It is used for the calibration of the component's ODT and output driver.

Block Diagram (64bits x8 2Ranks)



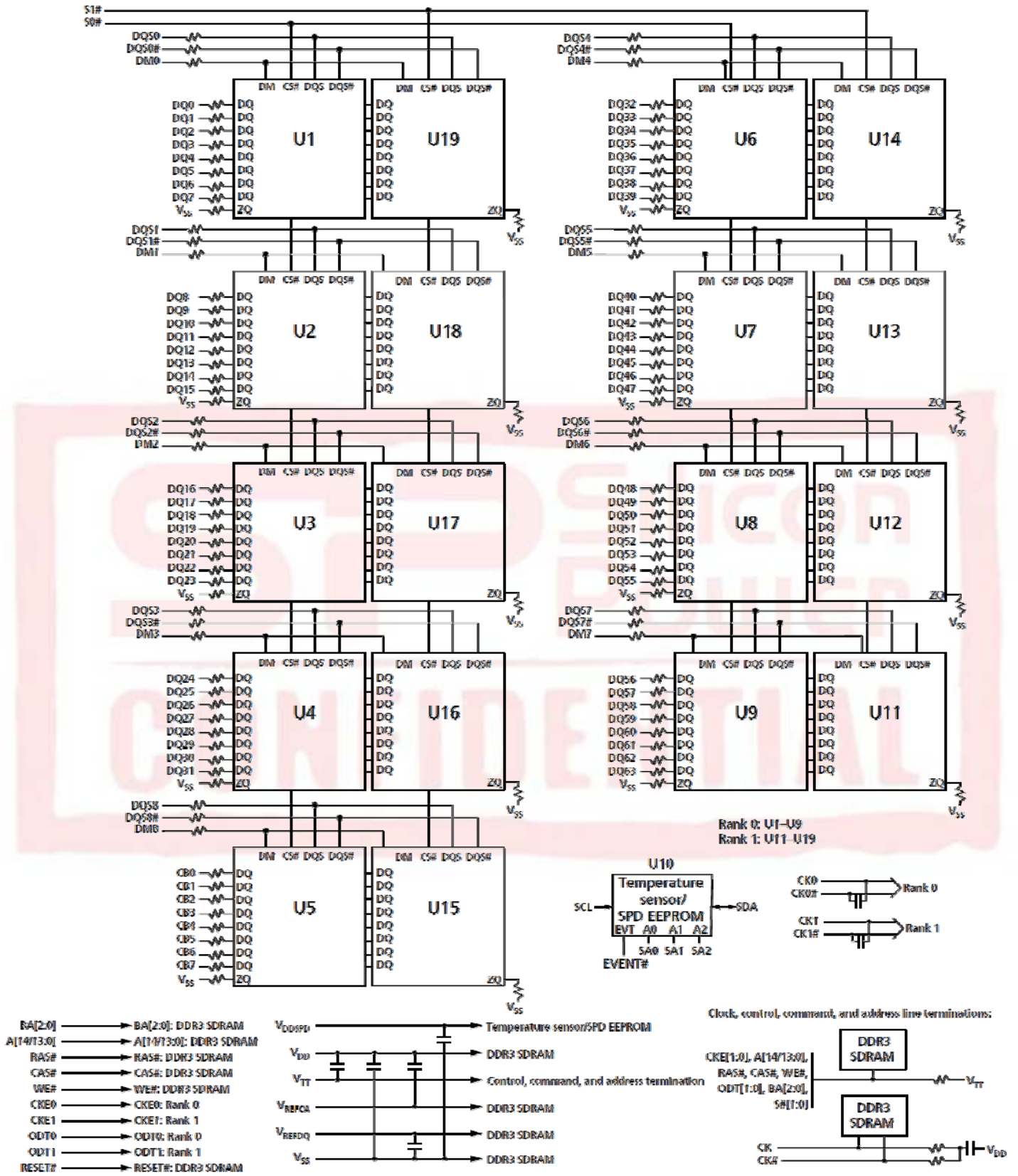
Note: The ZQ ball on each DDR3 component is connected to an external 240Ω resistor that is tied to ground. It is used for the calibration of the component's ODT and output driver.

Block Diagram (72bits x8 1Rank)



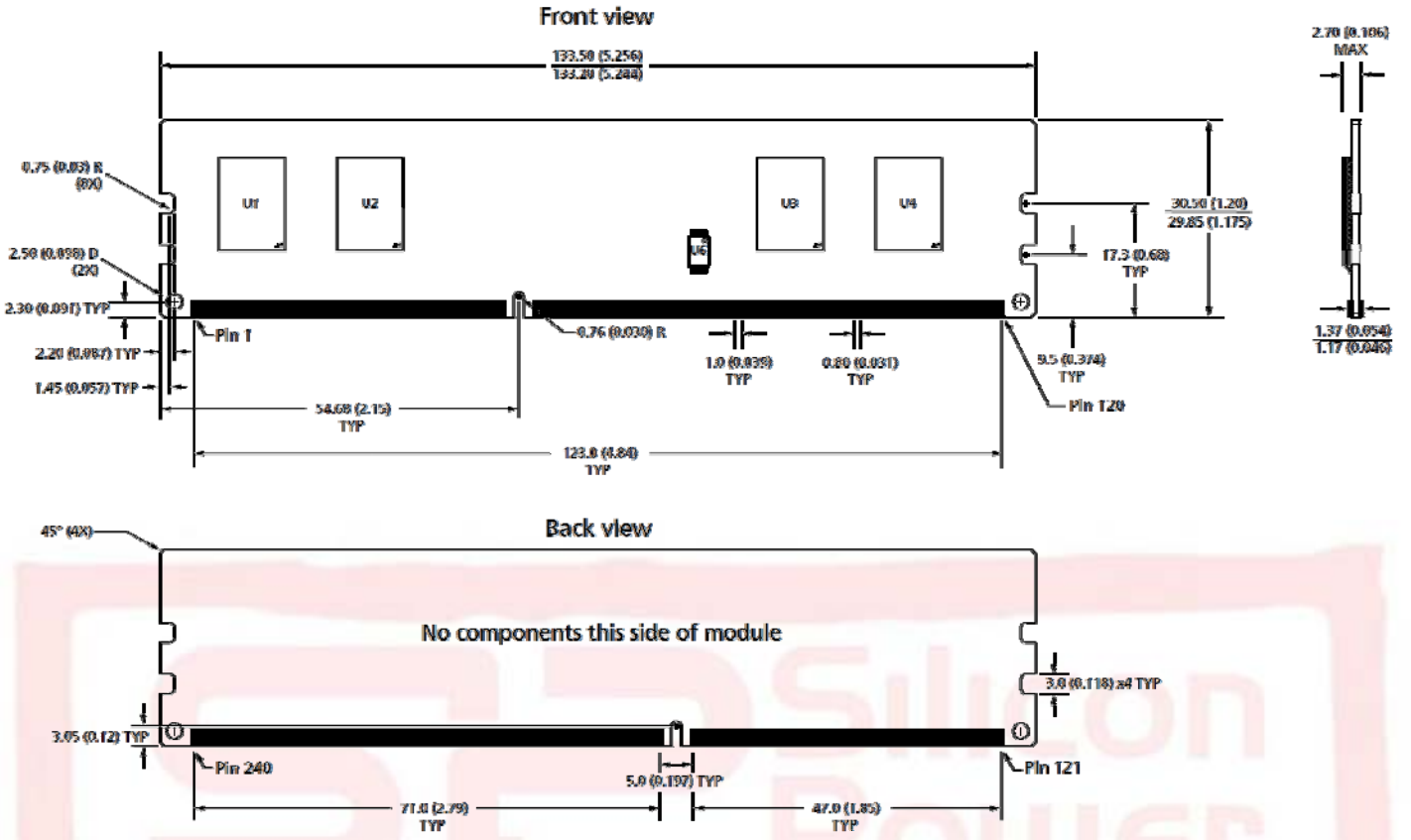
Note: The ZQ ball on each DDR3 component is connected to an external 240Ω resistor that is tied to ground. It is used for the calibration of the component's ODT and output driver.

Block Diagram (72bits x8 2Ranks)



Note: The ZQ ball on each DDR3 component is connected to an external 240Ω resistor that is tied to ground. It is used for the calibration of the component's ODT and output driver.

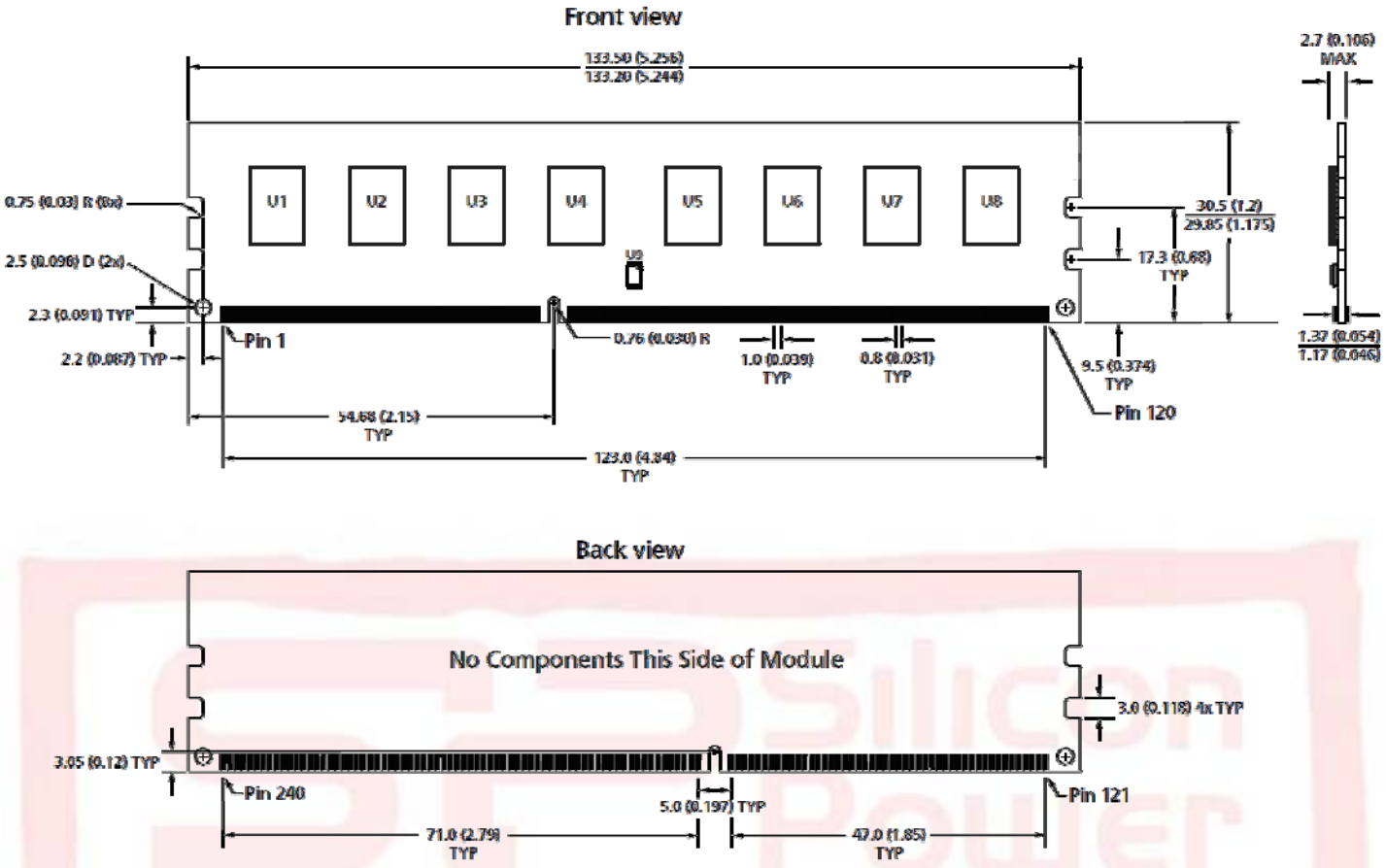
LLU Series Simplified Mechanical Drawing (64bits x16 1Rank)



Note: 1. All dimensions are in millimeters (inches); MAX/MIN or typical (TYP) where noted.

Note: 2. The dimensional diagram is for reference only.

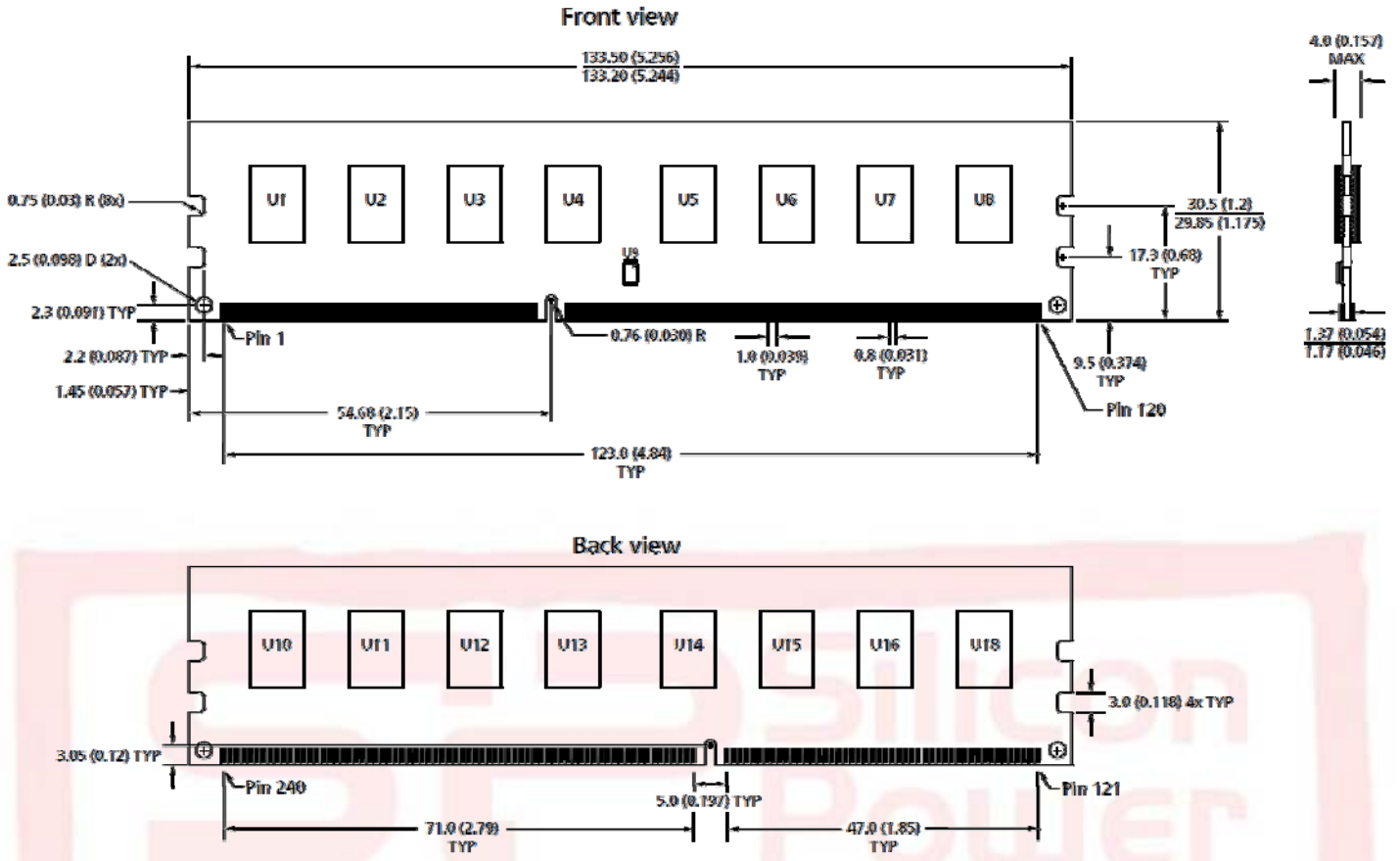
LLU Series Simplified Mechanical Drawing (64bits x8 1Rank)



Note: 1. All dimensions are in millimeters (inches); MAX/MIN or typical (TYP) where noted.

Note: 2. The dimensional diagram is for reference only.

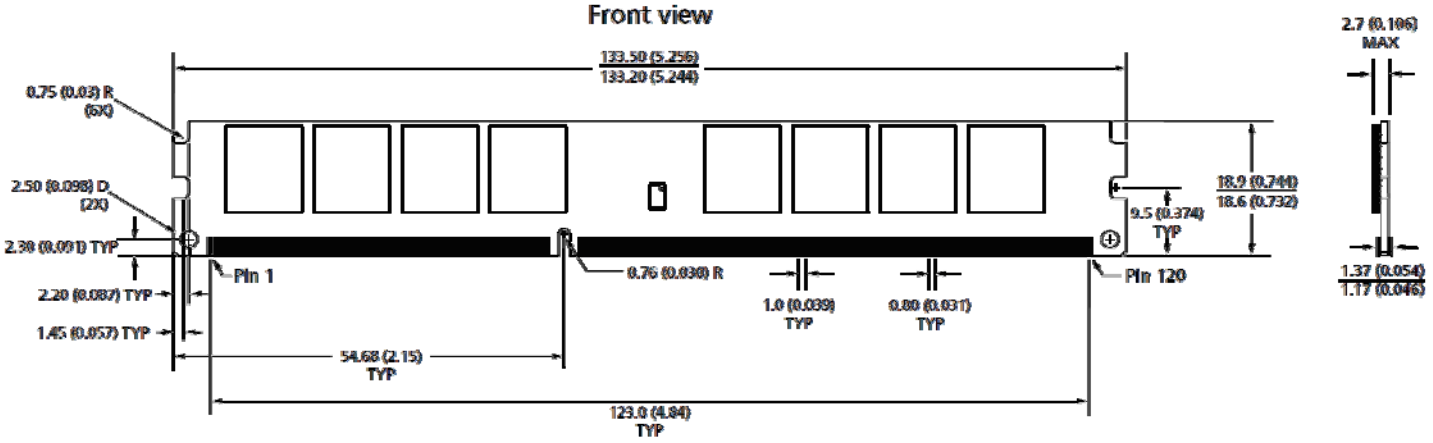
LLU Series Simplified Mechanical Drawing (64bits x8 2Ranks)

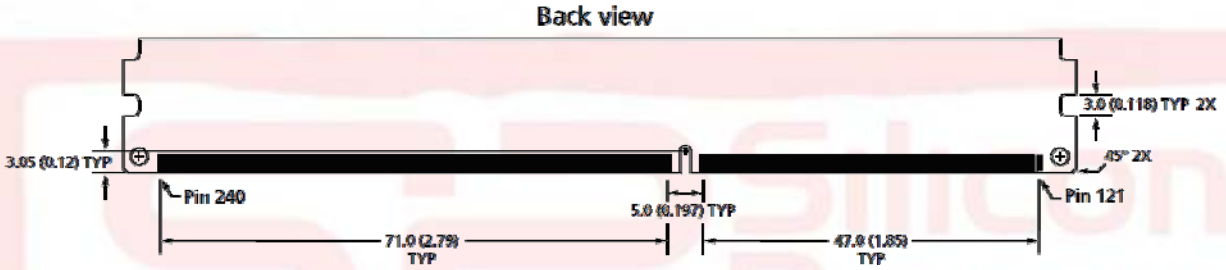


Note: 1. All dimensions are in millimeters (inches); MAX/MIN or typical (TYP) where noted.

Note: 2. The dimensional diagram is for reference only.

VLU Series Simplified Mechanical Drawing (64bits x8 1Rank)

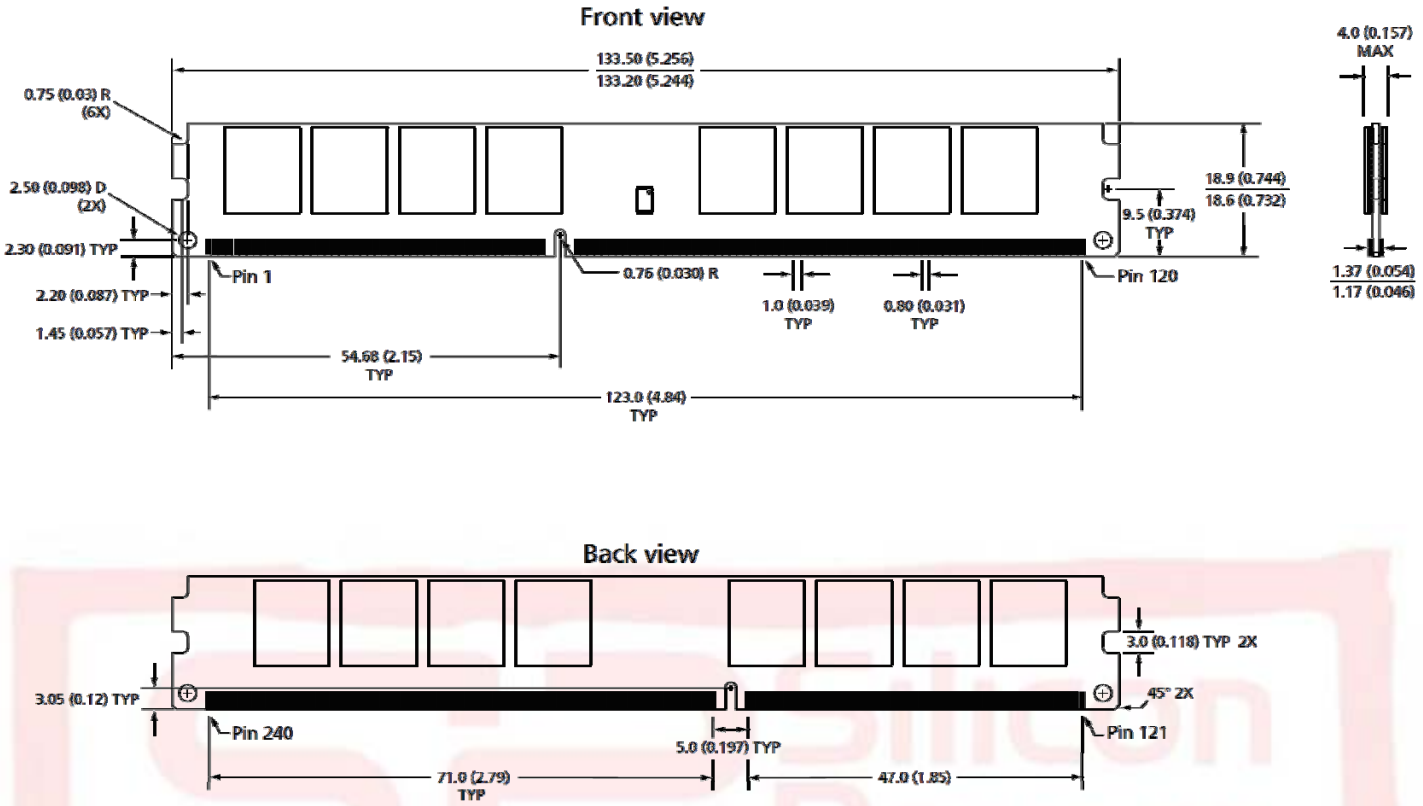




Note: 1. All dimensions are in millimeters (inches); MAX/MIN or typical (TYP) where noted.

Note: 2. The dimensional diagram is for reference only.

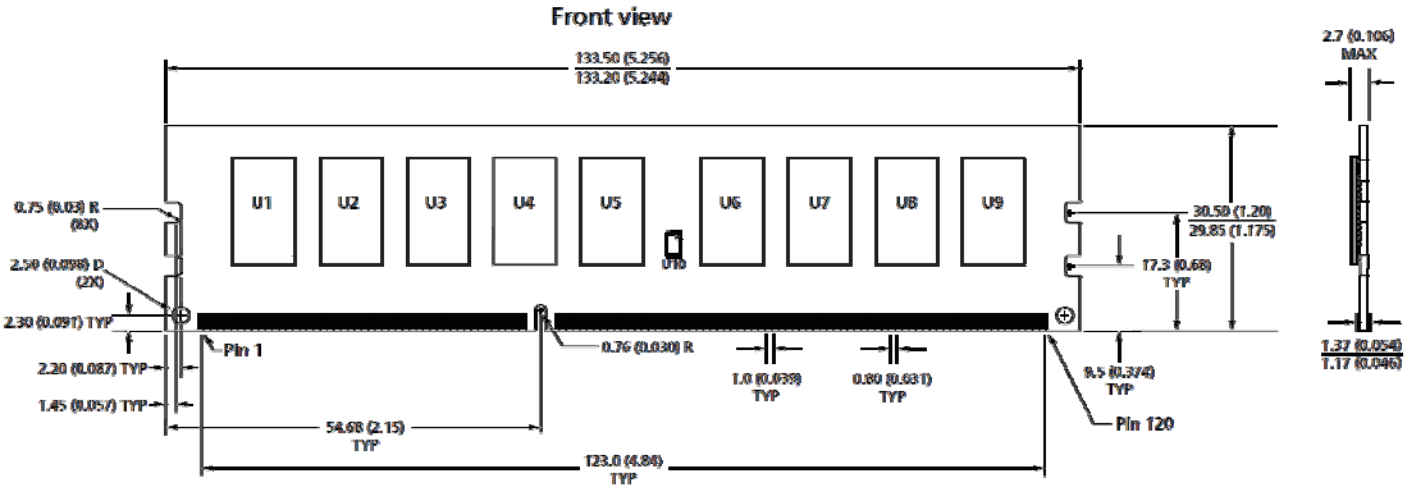
VLU Series Simplified Mechanical Drawing (64bits x8 2Ranks)

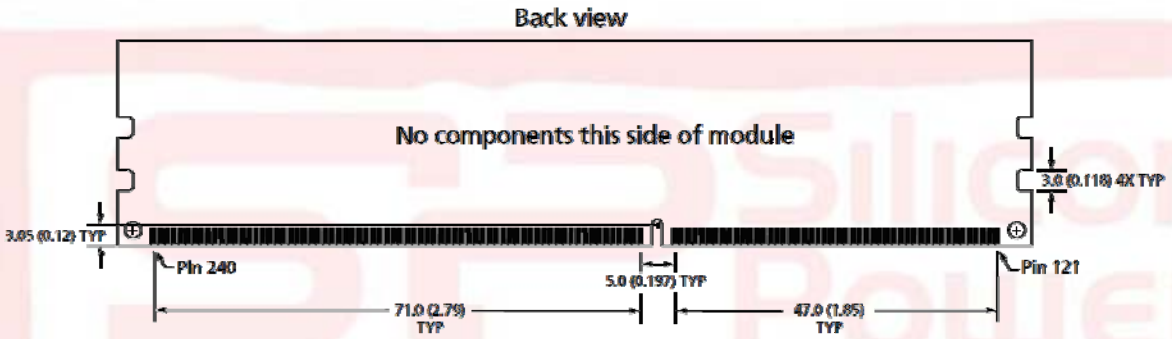


Note: 1. All dimensions are in millimeters (inches); MAX/MIN or typical (TYP) where noted.

Note: 2. The dimensional diagram is for reference only.

LLE Series Simplified Mechanical Drawing (72bits x8 1Rank)

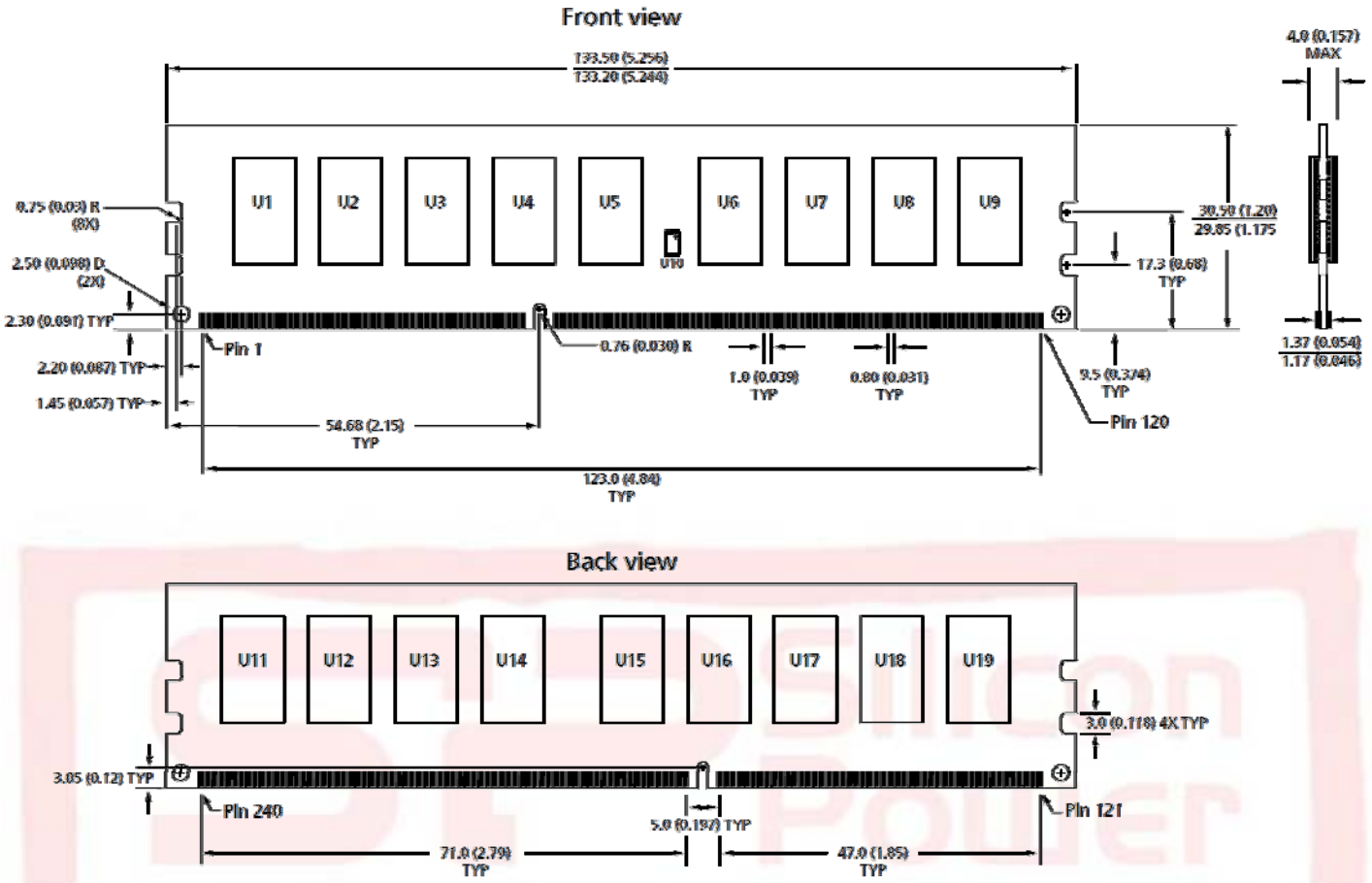




Note: 1. All dimensions are in millimeters (inches); MAX/MIN or typical (TYP) where noted.

Note: 2. The dimensional diagram is for reference only.

LLE Series Simplified Mechanical Drawing (72bits x8 2Rank)



Note: 1. All dimensions are in millimeters (inches); MAX/MIN or typical (TYP) where noted.

Note: 2. The dimensional diagram is for reference only.