Industrial
DDR4 SODIMM
Datasheet

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Revision History

Revision No.	Date	Remarks
1.0	2017/12	First release
1.1	2018/3	Add 512Mx16 Solution
1.2	2018/7	Add Wide Temp series
1.3	2019/6	Add 256Mx16, DDR4-2666 products.
1.3a	2019/9	Modify part number

Description

The Silicon Power Computer & Communications industrial SFU & SFE series products are 260-Pin low power Double Data Rate 4 (DDR4) Synchronous DRAM Small Outline Dual In-Line Memory Module (SODIMM).

The industrial SFU and SFV series organized as a one rank 256Mx64, 512Mx64, 1024Mx64, high-speed memory array or two ranks 2048Mx64, high-speed memory array, The module uses four 256Mx16(2GB), 512Mx16(4GB), eight 1Gx8(8GB), sixteen 1Gx8(16GB) DDR4 SDRAMs in BGA packages.

The industrial SFE series organized as a one rank 1024Mx72, high-speed memory array or two ranks 2048Mx72, high-speed memory array, The module uses nine 512Mx8(4GB), 1Gx8(8GB), eighteen 1Gx8 (16GB) DDR4 SDRAMs in BGA packages.

This DIMM is manufactured using raw cards developed for broad industry use as reference designs. The use of these common design files minimizes electrical variation between suppliers.

DDR4 SDRAM SODIMM provide a high-performance, flexible 8-byte interface in a space-saving footprint.

The DIMM is intended for use in applications operating of 1200MHz or 1333MHz clock speeds and achieves high-speed data transfer rates of 2400Mbps or 2666Mbps. Prior to any access operation, the device CAS latency and burst/length/operation type must be programmed into the DIMM by address inputs A0-A15(1Gx8) and I/O inputs BA0, BA1, BG0, BG1 using the mode register set cycle.

The DIMM uses serial presence-detect implemented via a serial EEPROM using a standard IIC protocol.

Features

- DDR4 functionality and operations supported as defined in the component data sheet
- 260pin, Small Outline Dual In-line Memory Module (SODIMM)
- Fast data transfer rates:
  DDR4-2400(PC4-19200)
  DDR4-2666(PC4-21300)
- Single or Dual rank
- SFU/SFV: 2GB(256Mega x 64), 4GB(512Mega x 64), 8GB (1Giga x 64), 16GB (2Giga x 64)
- SFE/SFF: 4GB(512Mega x 72), 8GB (1Giga x 72), 16GB (2Giga x 72)
- $V_{DD} = V_{DDQ} = 1.2V \pm 0.06V$
- V_{DDSPD} = 1.7V to 3.6V
- V_{PP} = 2.5V(DRAM Activating Power Supply:)
- 16 internal banks; 4 groups of 4 banks each
- Nominal and dynamic on-die termination (ODT) for data, strobe, and mask signals
- Low-power auto self refresh (LPASR)
- Data bus inversion (DBI) for data bus
- Fixed burst chop (BC) of 4 and burst length (BL) of 8 via the mode register set (MRS)
- Fly-by topology
- Terminated control, command, and address bus
- This product is in compliance with the RoHS directive
- Integrated serial presence-detect (SPD) EEPROM
- Gold edge contacts

Module Specification

DDR4 Industrial SODIMM SFU Module Specification

Part Number	Module Density & Configuration	Bandwidth	Data Rate	Timing	Operating Voltage
				tCL-tRCD-tRP	
SP002GISFU266WN0	2GB (256Mx64) 256Mx16 1Rank	21.3GB/s	DDR4-2666	19-19-19	1.2V
SP004GISFU240CS0	4GB (512Mx64) 512Mx16 1Rank	19.2GB/s	DDR4-2400	17-17-17	1.2V
SP004GISFU240NH0	4GB (512Mx64) 512Mx16 1Rank	19.2GB/s	DDR4-2400	17-17-17	1.2V
SP008GISFU240BS0	8GB (1Gx64) 1Gx8 1Rank	19.2GB/s	DDR4-2400	17-17-17	1.2V
SP008GISFU266BH0	8GB (1Gx64) 1Gx8 1Rank	21.3GB/s	DDR4-2666	19-19-19	1.2V
SP016GISFU240BS0	16GB (2Gx64) 1Gx8 2Ranks	19.2GB/s	DDR4-2400	17-17-17	1.2V
SP016GISFU266BH0	16GB (2Gx64) 1Gx8 2Ranks	21.3GB/s	DDR4-2666	19-19-19	1.2V

DDR4 Industrial SODIMM with ECC SFE Module Specification

Part Number	Module Density & Configuration	Bandwidth	Data Rate	Timing	Operator Voltage
				tCL-tRCD-tRP	
SP004GISFE240NH0	4GB (1Gx72) 512Mx8 1Rank	19.2GB/s	DDR4-2400	17-17-17	1.2V
SP004GISFE240NS0	4GB (1Gx72) 512Mx8 1Rank	19.2GB/s	DDR4-2400	17-17-17	1.2V
SP008GISFE240BS0	8GB (1Gx72) 1Gx8 1Rank	19.2GB/s	DDR4-2400	17-17-17	1.2V
SP008GISFE266BH0	8GB (1Gx72) 1Gx8 1Rank	21.3GB/s	DDR4-2666	19-19-19	1.2V
SP016GISFE240BS0	16GB (2Gx72) 1Gx8 2Ranks	19.2GB/s	DDR4-2400	17-17-17	1.2V
SP016GISFE266BH0	16GB (2Gx72) 1Gx8 2Ranks	21.3GB/s	DDR4-2666	19-19-19	1.2V

Note:

1. This document supports all industrial SFU & SFE Series DDR4 260Pin SODIMM products.
2. Some items were being EOL in this list, Please contact with our sales Dep.
3. All part numbers end with a double-digit code is for customize use only.

   `Example: SP008GISFU240BS0XX`

DDR4 Industrial wide temp SODIMM SFV Series Module Specification

Part Number	Module Density & Configuration	Bandwidth	Data Rate	Timing tCL-tRCD-tRP	Operating Voltage	Operating Temperature
SP004GISFV240CS0	4GB (512Mx64) 512Mx16 1Rank	19.2GB/s	DDR4-2400	17-17-17	1.2V	-40~85°C
SP004GISFV240NH0	4GB (512Mx64) 512Mx81Rank	19.2GB/s	DDR4-2400	17-17-17	1.2V	-40~85°C
SP008GISFV240BS0	8GB (1Gx64) 1Gx8 1Rank	19.2GB/s	DDR4-2400	17-17-17	1.2V	-40~85°C
SP008GISFV266BH0	8GB (1Gx64) 1Gx8 1Rank	21.3GB/s	DDR4-2666	19-19-19	1.2V	-40~85°C
SP016GISFV240BS0	16GB (2Gx64) 1Gx8 2Ranks	19.2GB/s	DDR4-2400	17-17-17	1.2V	-40~85°C
SP016GISFV266BH0	16GB (2Gx64) 1Gx8 2Ranks	21.3GB/s	DDR4-2666	19-19-19	1.2V	-40~85°C

DDR4 Industrial wide temp SODIMM with ECC SFF Module Specification

Part Number	Module Density & Configuration	Bandwidth	Data Rate	Timing tCL-tRCD-tRP	Operator Voltage	Operating Temperature
SP004GISFF240NH0	4GB (1Gx72) 512Mx8 1Rank	19.2GB/s	DDR4-2400	17-17-17	1.2V	-40~85°C
SP004GISFF240NS0	8GB (1Gx72) 1Gx8 1Rank	19.2GB/s	DDR4-2400	17-17-17	1.2V	-40~85°C
SP008GISFF240BS0	8GB (1Gx72) 1Gx8 1Rank	19.2GB/s	DDR4-2400	17-17-17	1.2V	-40~85°C
SP008GISFF266BH0	8GB (1Gx72) 1Gx8 1Rank	21.3GB/s	DDR4-2666	19-19-19	1.2V	-40~85°C
SP016GISFF240BS0	16GB (2Gx72) 1Gx8 2Ranks	19.2GB/s	DDR4-2400	17-17-17	1.2V	-40~85°C
SP016GISFF266BH0	16GB (2Gx72) 1Gx8 2Ranks	21.3GB/s	DDR4-2666	19-19-19	1.2V	-40~85°C

Note:

1. This document supports all industrial SFV & SFE Series DDR4 260Pin SODIMM products.
2. Some items were being EOL in this list, Please contact with our sales Dep.
3. All part numbers end with a double-digit code is for customize use only.

`Example: SP008GISFV240BS0XX`

Pin Assignments

260-Pin DDR4 SODIMM Front								260-Pin DDR4 SODIMM Back							
Pin	**Symbol**	**Pin**	**Symbol**	**Pin**	**Symbol**	**Pin**	**Symbol**	**Pin**	**Symbol**	**Pin**	**Symbol**	**Pin**	**Symbol**	**Pin**	**Symbol**
1	VSS	67	DQ29	133	A1	199	DM5_n/DBI5_n	2	VSS	68	VSS	134	EVENT_n, NF	200	DQS5_t
3	DQ5	69	VSS	135	VDD	201	VSS	4	DQ4	70	DQ24	136	VDD	202	VSS
5	VSS	71	DQ25	137	CK0_t	203	DQ46	6	VSS	72	VSS	138	CK1_t/NF	204	DQ47
7	DQ1	73	VSS	139	CK0_c	205	VSS	8	DQ0	74	DQS3_c	140	CK1_c/NF	206	VSS
9	VSS	75	DM3_n/DBI3_n	141	VDD	207	DQ42	10	VSS	76	DQS3_t	142	VDD	208	DQ43
11	DQS0_c	77	VSS	143	PARITY	209	VSS	12	DM0_n/DBI0_n	78	VSS	144	A0	210	VSS
13	DQS0_t	79	DQ30	145	BA1	211	DQ52	14	VSS	80	DQ31	146	A10/AP	212	DQ53
15	VSS	81	VSS	147	VDD	213	VSS	16	DQ6	82	VSS	148	VDD	214	VSS
17	DQ7	83	DQ26	149	CS0_n	215	DQ49	18	VSS	84	DQ27	150	BA0	216	DQ48
19	VSS	85	VSS	151	WE_n/ A14	217	VSS	20	DQ2	86	VSS	152	RAS_n/A16	218	VSS
21	DQ3	87	CB5/NC	153	VDD	219	DQS6_c	22	VSS	88	CB4/NC	154	VDD	220	DM6_n/DBI6_n
23	VSS	89	VSS	155	ODT0	221	DQS6_t	24	DQ12	90	VSS	156	CAS_n/A15	222	VSS
25	DQ13	91	CB1/NC	157	CS1_n/ NC	223	VSS	26	VSS	92	CB0/NC	158	A13	224	DQ54
27	VSS	93	VSS	159	VDD	225	DQ55	28	DQ8	94	VSS	160	VDD	226	VSS
29	DQ9	95	DQS8_c	161	ODT1/ NC	227	VSS	30	VSS	96	DM8_n/DBI_n/NC	162	C0/CS2_n/NC	228	DQ50
31	VSS	97	DQS8_t	163	VDD	229	DQ51	32	DQS1_c	98	VSS	164	VREFCA	230	VSS
33	DM1_n/DBI_n	99	VSS	165	C1, CS3_n, NC	231	VSS	34	DQS1_t	100	CB6/NC	166	SA2	232	DQ60
35	VSS	101	CB2/NC	167	VSS	233	DQ61	36	VSS	102	VSS	168	VSS	234	VSS
37	DQ15	103	VSS	169	DQ37	235	VSS	38	DQ14	104	CB7/NC	170	DQ36	236	DQ57
39	VSS	105	CB3/NC	171	VSS	237	DQ56	40	VSS	106	VSS	172	VSS	238	VSS
41	DQ10	107	VSS	173	DQ33	239	VSS	42	DQ11	108	RESET_n	174	DQ32	240	DQS7_c
43	VSS	109	CKE0	175	VSS	241	DM7_n/DBI7_n	44	VSS	110	CKE1/ NC	176	VSS	242	DQS7_t
45	DQ21	111	VDD	177	DQS4_c	243	VSS	46	DQ20	112	VDD	178	DM4_n/DBI4_n	244	VSS
47	VSS	113	BG1	179	DQS4_t	245	DQ62	48	VSS	114	ACT_n	180	VSS	246	DQ63
49	DQ17	115	BG0	181	VSS	247	VSS	50	DQ16	116	ALERT_n	182	DQ39	248	VSS
51	VSS	117	VDD	183	DQ38	249	DQ58	52	VSS	118	VDD	184	VSS	250	DQ59
53	DQS2_c	119	A12	185	VSS	251	VSS	54	DM2_n/DBI2_n	120	A11	186	DQ35	252	VSS
55	DQS2_t	121	A9	187	DQ34	253	SCL	56	VSS	122	A7	188	VSS	254	SDA
57	VSS	123	VDD	189	VSS	255	VDDSPD	58	DQ22	124	VDD	190	DQ45	256	SA0
59	DQ23	125	A8	191	DQ44	257	VPP	60	VSS	126	A5	192	VSS	258	VTT
61	VSS	127	A6	193	VSS	259	VPP	62	DQ18	128	A4	194	DQ41	260	SA1
63	DQ19	129	VDD	195	DQ40	–	–	64	VSS	130	VDD	196	VSS	–	–
65	VSS	131	A3	197	VSS	–	–	66	DQ28	132	A2	198	DQS5_c	–	–

Pin Description

Symbol	Type	Description
Ax	Input	**Address inputs:** Provide the row address for ACTIVATE commands and the column address for READ/WRITE commands in order to select one location out of the memory array in the respective bank. (A10/AP, A12/BC_n, WE_n/A14, CAS_n/A15, and RAS_n/A16 have additional functions; see individual entries in this table.) The address inputs also provide the op-code during the MODE REGISTER SET command. A17 is only defined for x4 SDRAM. A0–A14 (512Mx8).
A10/AP	Input	**Auto precharge:** A10 is sampled during READ and WRITE commands to determine whether an auto precharge should be performed on the accessed bank after a READ or WRITE operation. (HIGH = auto precharge; LOW = no auto precharge.) A10 is sampled during a PRECHARGE command to determine whether the precharge applies to one bank (A10 LOW) or all banks (A10 HIGH). If only one bank is to be precharged, the bank is selected by the bank group and bank addresses.
A12/BC_n	Input	**Burst chop:** A12/BC_n is sampled during READ and WRITE commands to determine if burst chop (on-the-fly) will be performed. (HIGH = no burst chop; LOW = burst- chopped.) See Command Truth Table in the DDR4 component data sheet.
ACT_n	Input	**Command input:** ACT_n defines the ACTIVATE command being entered along with CS_n. The input into RAS_n/A16, CAS_n/A15, and WE_n/A14 are considered as row address A16, A15, and A14. See Command Truth Table.
BAx	Input	**Bank address inputs:** Define the bank (with a bank group) to which an ACTIVATE, READ, WRITE, or PRECHARGE command is being applied. Also determine which mode register is to be accessed during a MODE REGISTER SET command.
BGx	Input	**Bank group address inputs:** Define the bank group to which a REFRESH, ACTIVATE, READ, WRITE, or PRECHARGE command is being applied. Also determine which mode register is to be accessed during a MODE REGISTER SET command. BG[1:0] are used in the x4 and x8 configurations. x16-based SDRAM only has BG0.
C0, C1, C2 (RDIMM/LRDIMM only)	Input	**Chip ID:** These inputs are used only when devices are stacked; that is, 2H, 4H, and 8H stacks for x4 and x8 configurations using through-silicon vias (TSVs). These pins are not used in the x16 configuration. Some DDR4 modules support a traditional DDP package, which uses CS1_n, CKE1, and ODT1 to control the second die. All other stack configurations, such as a 4H or 8H, are assumed to be single-load (master/slave) type configurations where C0, C1, and C2 are used as chip ID selects in conjunction with a single CS_n, CKE, and ODT. Chip ID is considered part of the command code.
CKx_t CKx_c	Input	**Clock:** Differential clock inputs. All address, command, and control input signals are sampled on the crossing of the positive edge of CK_t and the negative edge of CK_c.
CKEx	Input	**Clock enable:** CKE HIGH activates and CKE LOW deactivates the internal clock signals, device input buffers, and output drivers. Taking CKE LOW provides PRECHARGE POWER-DOWN and SELF REFRESH operations (all banks idle), or active power-down (row active in any bank). CKE is asynchronous for self refresh exit. After VREFCA has become stable during the power-on and initialization sequence, it must be maintained during all operations (including SELF REFRESH). CKE must be maintained HIGH throughout read and write accesses. Input buffers (excluding CK_t, CK_c, ODT, RESET_n, and CKE) are disabled during power-down. Input buffers (excluding CKE and RESET#) are disabled during self refresh.
CSx_n	Input	**Chip select:** All commands are masked when CS_n is registered HIGH. CS_n provides external rank selection on systems with multiple ranks. CS_n is considered part of the command code. (CS2_n and CS3_n are not used on UDIMMs.)
ODTx	Input	**On-die termination:** ODT (registered HIGH) enables termination resistance internal to the DDR4 SDRAM. When enabled, ODT (RTT) is applied only to each DQ, DQS_t, DQS_c, DM_n/DBI_n/TDQS_t, and TDQS_c signal for x4 and x8 configurations (when the TDQS function is enabled via the mode register). For the x16 configuration, RTT is applied to each DQ, DQSU_t, DQSU_c, DQSL_t, DQSL_c, UDM_n, and LDM_n signal. The ODT pin will be ignored if the mode registers are programmed to disable RTT.

Pin Description (Continued)

Symbol	Type	Description
PARITY	Input	**Parity for command and address:** This function can be enabled or disabled via the mode register. When enabled in MR5, the DRAM calculates parity with ACT_n, RAS_n/A16, CAS_n/A15, WE_n/A14, BG[1:0], BA[1:0], A[16:0]. Input parity should be maintained at the rising edge of the clock and at the same time as command and address with CS_n LOW.
RAS_n/A16 CAS_n/A15 WE_n/A14	Input	**Command inputs:** RAS_n/A16, CAS_n/A15, and WE_n/A14 (along with CS_n) define the command and/or address being entered and have multiple functions. For example, for activation with ACT_n LOW, these are addresses like A16, A15, and A14, but for a non-activation command with ACT_n HIGH, these are command pins for READ, WRITE, and other commands defined in Command Truth Table.
RESET_n	CMOS Input	**Active LOW asynchronous reset:** Reset is active when RESET_n is LOW and inactive when RESET_n is HIGH. RESET_n must be HIGH during normal operation.
SAx	Input	**Serial address inputs:** Used to configure the temperature sensor/SPD EEPROM address range on the I2C bus.
SCL	Input	**Serial clock for temperature sensor/SPD EEPROM:** Used to synchronize communication to and from the temperature sensor/SPD EEPROM on the I2C bus.
DQx, CBx	I/O	**Data input/output and check bit input/output:** Bidirectional data bus. DQ represents DQ[3:0], DQ[7:0], and DQ[15:0] for the x4, x8, and x16 configurations, respectively. If cyclic redundancy checksum (CRC) is enabled via the mode register, the CRC code is added at the end of the data burst. Any one or all of DQ0, DQ1, DQ2, or DQ3 may be used for monitoring of internal VREF level during test via mode register setting MR[4] A[4] = HIGH; training times change when enabled.
DM_n/DBI_n/TDQS_t (DMU_n, DBIU_n), (DML_n/DBIl_n)	I/O	**Input data mask and data bus inversion:** DM_n is an input mask signal for write data. Input data is masked when DM_n is sampled LOW coincident with that input data during a write access. DM_n is sampled on both edges of DQS. DM is multiplexed with the DBI function by the mode register A10, A11, and A12 settings in MR5. For a x8 device, the function of DM or TDQS is enabled by the mode register A11 setting in MR1. DBI_n is an input/output identifying whether to store/output the true or inverted data. If DBI_n is LOW, the data will be stored/output after inversion inside the DDR4 device and not inverted if DBI_n is HIGH. TDQS is only supported in x8 SDRAM configurations. (TDQS is not valid for UDIMMs.)
SDA	I/O	**Serial Data:** Bidirectional signal used to transfer data in or out of the EEPROM or EEPROM/TS combo device.
DQS_t DQS_c DQSU_t DQSU_c DQSL_t DQSL_c	I/O	**Data strobe:** Output with read data, input with write data. Edge-aligned with read data, centered-aligned with write data. For x16 configurations, DQSL corresponds to the data on DQ[7:0], and DQSU corresponds to the data on DQ[15:8]. For the x4 and x8 configurations, DQS corresponds to the data on DQ[3:0] and DQ[7:0], respectively. DDR4 SDRAM supports a differential data strobe only and does not support a singleended data strobe.
ALERT_n	Output	**Alert output:** Possesses functions such as CRC error flag and command and address parity error flag as output signal. If a CRC error occurs, ALERT_n goes LOW for the period time interval and returns HIGH. If an error occurs during a command address parity check, ALERT_n goes LOW until the on-going DRAM internal recovery transaction is complete. During connectivity test mode, this pin functions as an input. Use of this signal is system-dependent. If not connected as signal, ALERT_n pin must be connected to VDD on DIMMs.
EVENT_n	Output	**Temperature event:** The EVENT_n pin is asserted by the temperature sensor when critical temperature thresholds have been exceeded. This pin has no function (NF) on modules without temperature sensors.

Pin Description (Continued)

Symbol	Type	Description
TDQS_t TDQS_c (x8 DRAM-based RDIMM only)	Output	**Termination data strobe:** When enabled via the mode register, the DRAM device enables the same RTT termination resistance on TDQS_t and TDQS_c that is applied to DQS_t and DQS_c. When the TDQS function is disabled via the mode register, the DM/ TDQS_t pin provides the data mask (DM) function, and the TDQS_c pin is not used. The TDQS function must be disabled in the mode register for both the x4 and x16 configurations. The DM function is supported only in x8 and x16 configurations. DM, DBI, and TDQS are a shared pin and are enabled/disabled by mode register settings. For more information about TDQS, see the DDR4 DRAM component data sheet. (TDQS_t and TDQS_c are not valid for UDIMMs.)
VDD	Supply	**Module power supply:** 1.21V (TYP).
VPP	Supply	**DRAM activating power supply:** 2.5V -0.125V / +0.250V.
VREFCA	Supply	Reference voltage for control, command, and address pins.
VSS	Supply	Ground.
VTT	Supply	Power supply for termination of address, command, and control VDD/2.
VDDSPD	Supply	Power supply used to power the I2C bus for SPD.
RFU	-	Reserved for future use.
NC	-	**No connect:** No internal electrical connection is present.
NF	-	**No function:** May have internal connection present, but has no function.

Environmental Requirements

Symbol	Parameter	Rating	Units	Note
T_{C}	Module operating case temperature	0 to 55	°C	1, 4
T_{OPR}	Module Operating Temperature Range (ambient)	0 to 55	°C	3, 4
$T_{C(\text{Wide Temp})}$	Wide temperature series Module operating case temperature	-40 to 85	°C	1, 4
$T_{OPR(\text{Wide Temp})}$	Wide temperature series Module Operating Temperature Range (ambient)	-40 to 85	°C	3, 4
H_{OPR}	Operating Humidity (relative)	10 to 90	%	4, 5
T_{STG}	Storage Temperature (Plastic)	-55 to 100	°C	2, 4, 5
H_{STG}	Storage Humidity (without condensation)	5 to 95	%	4, 5
P_{BAR}	Barometric Pressure (operating & storage)	105 to 69	K Pascal	4, 5, 6

Note:

1. Maximum operating case temperature; TC is measured in the center of the package.
2. Storage temperature is defined as the temperature of the top/center of the DRAM and does not reflect the storage temperatures of shipping trays.
3. The normal temperature range specifies the temperatures at which all DRAM specifications will be supported. During operation, the DRAM case temperature must be maintained between 0°C to 85°C under all operating conditions for the commercial offering; The wide temperature series offering allows the case temperature to go below 0°C to -40°C.
4. The component maximum case temperature shall not exceed the value specified in the component spec.
5. Stresses greater than those listed may cause permanent damage to the device. This is a stress rating only and device functional operation at or above the conditions indicated is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability.
6. Up to 9850 ft.

Absolute Maximum DC Ratings

Symbol	Parameter	Rating	Units	Note
VDD	Voltage on VDD pins relative to VSS	-0.3 V ~ 1.5 V	V	1
VDDQ	Voltage on VDDQ pins relative to VSS	-0.3 V ~ 1.5 V	V	1
VPP	Voltage on VPP pin relative to VSS	-0.3 V ~ 3.0 V	V	2
VIN, VOUT	Voltage on any pin relative to VSS	-0.3 V ~ 1.5 V	V	

Notes:

1. VDDQ tracks with VDD; VDDQ and VDD are tied together.
2. VPP must be greater than or equal to VDD at all times.
3. VDD and VDDQ must be within 300 mV of each other at all times;and VREFCA must be not greater than 0.6 x VDDQ, When VDD and VDDQ are less than 500 mV; VREFCA may be equal to or less than 300 mV.

Operating temperature Conditions

Symbol	Parameter	Rating	Units	Note
T_{OPER}	Normal Operating Temperature Range	0 to 85	°C	1, 2
	Extended Temperature Range (Optional)	85 to 95	°C	1, 3

Note:

1. Operating Temperature TOPER is the case surface temperature on the center / top side of the DRAM. For measurement conditions, please refer to the JEDEC document JESD51-2.
2. The Normal Temperature Range specifies the temperatures where all DRAM specifications will be supported. During operation, the DRAM case temperature must be maintained between 0 – 85^{0}C under all operating conditions.
3. Some applications require operation of the DRAM in the Extended Temperature Range between 85^{0}C and 95^{0}C case temperature. Full specifications are guaranteed in this range, but the following additional conditions apply:
   a. Refresh commands must be doubled in frequency, therefore reducing the Refresh interval tREFI to 3.9 µs. It is also possible to specify a component with 2X refresh (tREFI to 3.9µs) in the Extended Temperature Range. Please refer to the DIMM SPD for option availability.
   b. If Self-Refresh operation is required in the Extended Temperature Range, then it is mandatory to either use the Manual Self-Refresh mode with Extended Temperature Range capability (MR2 A6 = 0b and MR2 A7 = 1b) or enable the optional Auto Self-Refresh mode (MR2 A6 = 1b and MR2 A7 = 0b). DDR4 SDRAMs support Auto Self-Refresh and in Extended Temperature Range and please refer to component datasheet and/or the DIMM SPD for tREFI requirements in the Extended Temperature Range.

DC Electrical Characteristics and Operating Conditions

Symbol	Parameter	Min	Typ	Max	Units	Notes
VDD	Supply Voltage	1.14	1.2	1.26	V	1,2,3
V_{DDQ}	Output Supply Voltage	1.14	1.2	1.26	V	1,2,3
VPP	Supply Voltage for DRAM Activating	2.375	2.5	2.75	V	3

Note:

1. Under all conditions VDDQ must be less than or equal to VDD.
2. VDDQ tracks with VDD. AC parameters are measured with VDD and VDDQ tied together.
3. DC bandwidth is limited to 20MHz.

Single-Ended AC and DC Input Levels for Command and Address

Symbol	Parameter	DDR4-2133		Units	Note
		Min.	Max.		
VIH.CA(DC75)	DC Input Logic High	VREFCA+ 0.075	VDD	V	
VIL.CA(DC75)	DC Input Logic Low	VSS	VREFCA-0.075	V	
VIH.CA(AC100)	AC Input Logic High	VREF + 0.1	Note 2	V	1
VIL.CA(AC100)	AC Input Logic Low	Note 2	VREF - 0.1	V	1
VRefCA(DC)	Reference Voltage for ADD, CMD Inputs	0.49 x VDD	0.51 x VDD	V	2,3

Note:

1. See “Overshoot and Undershoot Specifications” on section.
2. The AC peak noise on VREFCA may not allow VREFCA to deviate from VREFCA(DC) by more than ± 1% VDD (for reference : approx. ± 12mV) .
3. For reference : approx. VDD/2 ± 12mV.

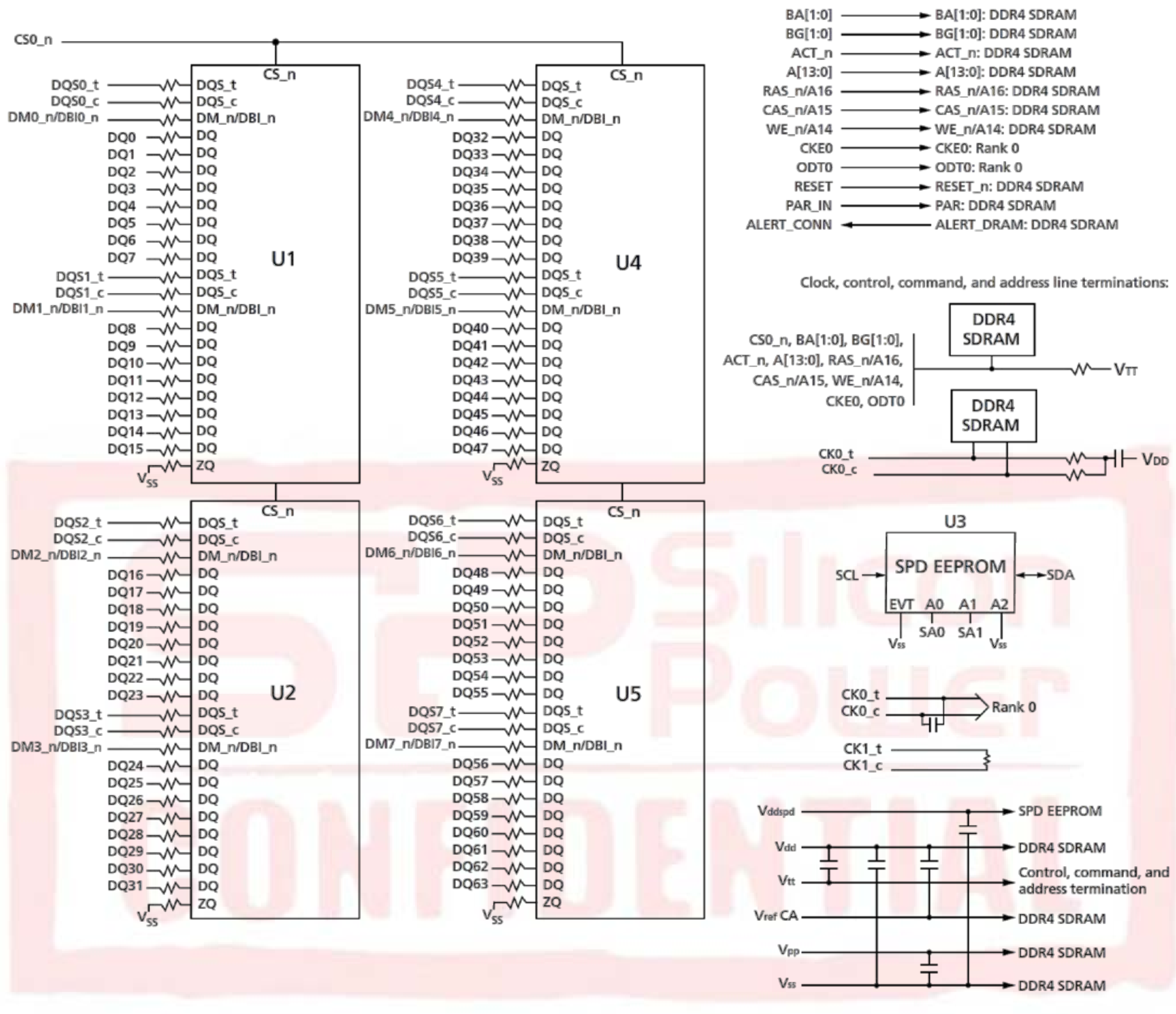
Single-Ended AC & DC Output Levels

Symbol	Parameter	DDR4-2133	Units	Note
VOH(DC)	DC output high measurement level (for IV curve linearity)	1.1 x VDDQ	V	
VOM(DC)	DC output mid measurement level (for IV curve linearity)	0.8 x VDDQ	V	
VOL(DC)	DC output low measurement level (for IV curve linearity)	0.5 x VDDQ	V	
VOH(AC)	AC output high measurement level (for output SR)	(0.7 + 0.15) x VDDQ	V	1
VOL(AC)	AC output low measurement level (for output SR)	(0.7 - 0.15) x VDDQ	V	1

Note:

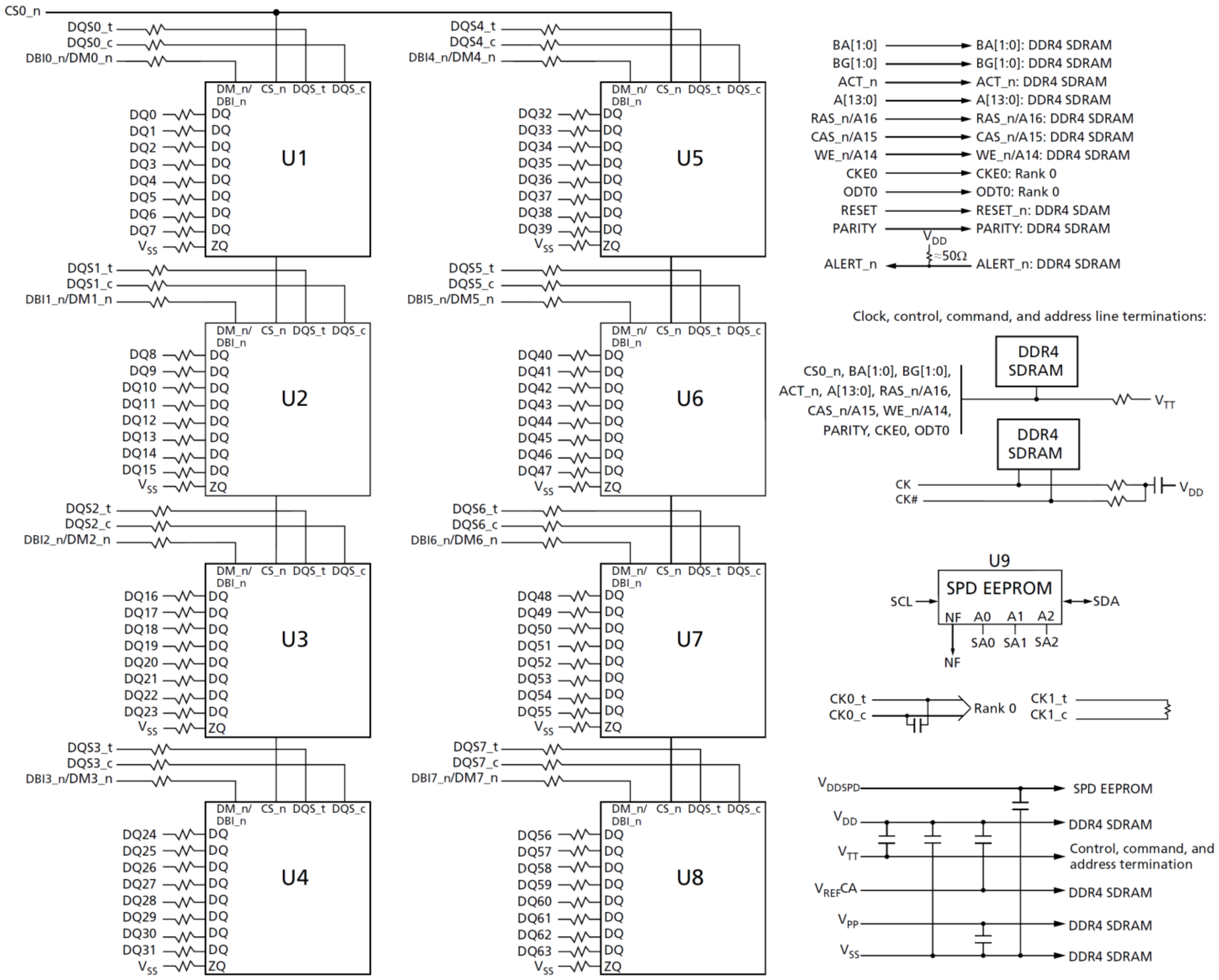
1. The swing of ± 0.15 × VDDQ is based on approximately 50% of the static single-ended output peak-to-peak swing with a driver impedance of RZQ/7Ω and an effective test load of 50Ω to VTT = VDDQ.

Block Diagram(x16 1Rank without ECC)



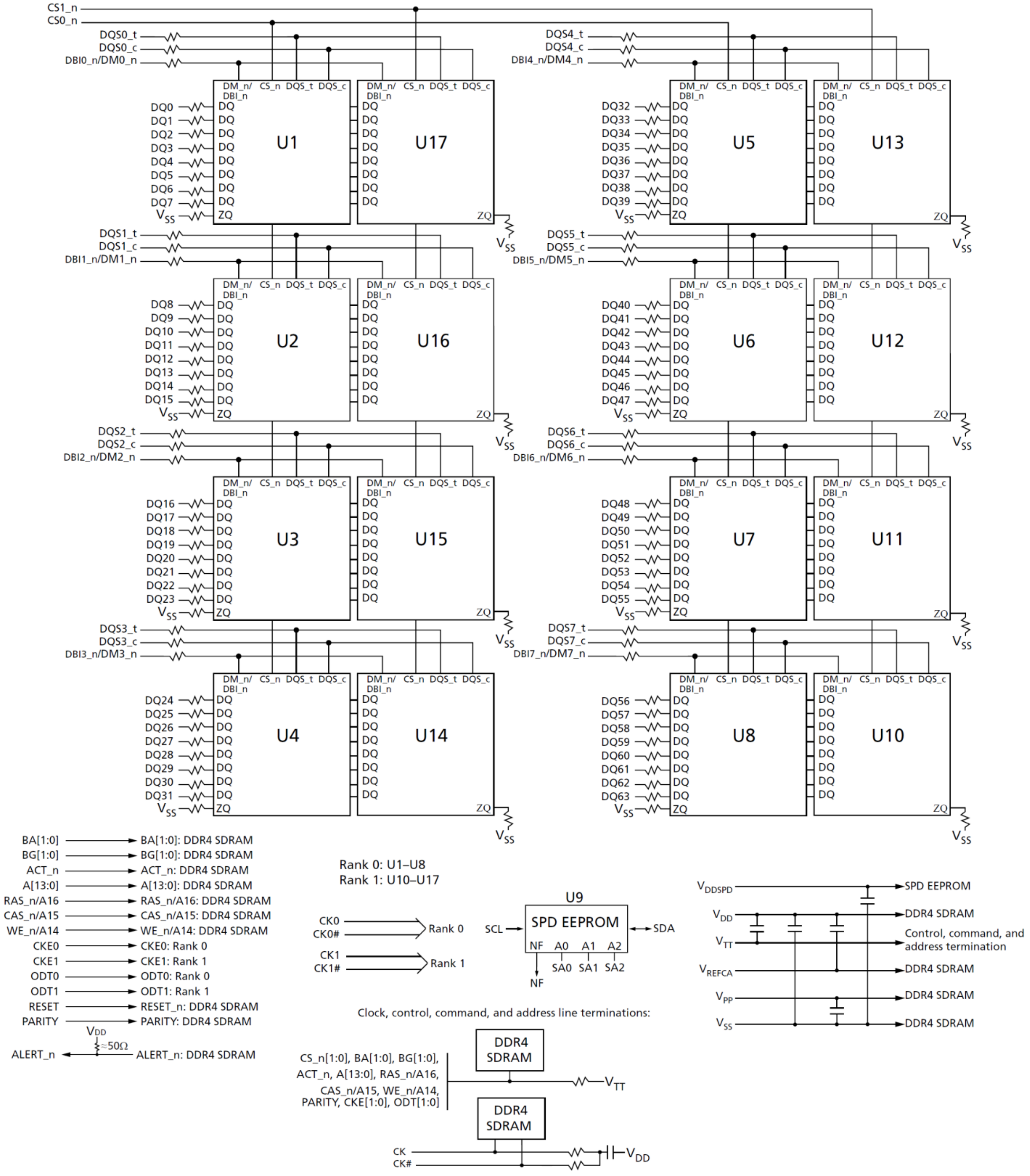
Note: 1. The ZQ ball on each DDR4 component is connected to an external 240Ω ±1% resistor that is tied to ground. It is used for the calibration of the component’s ODT and output driver.

Block Diagram(x8 1Rank without ECC)



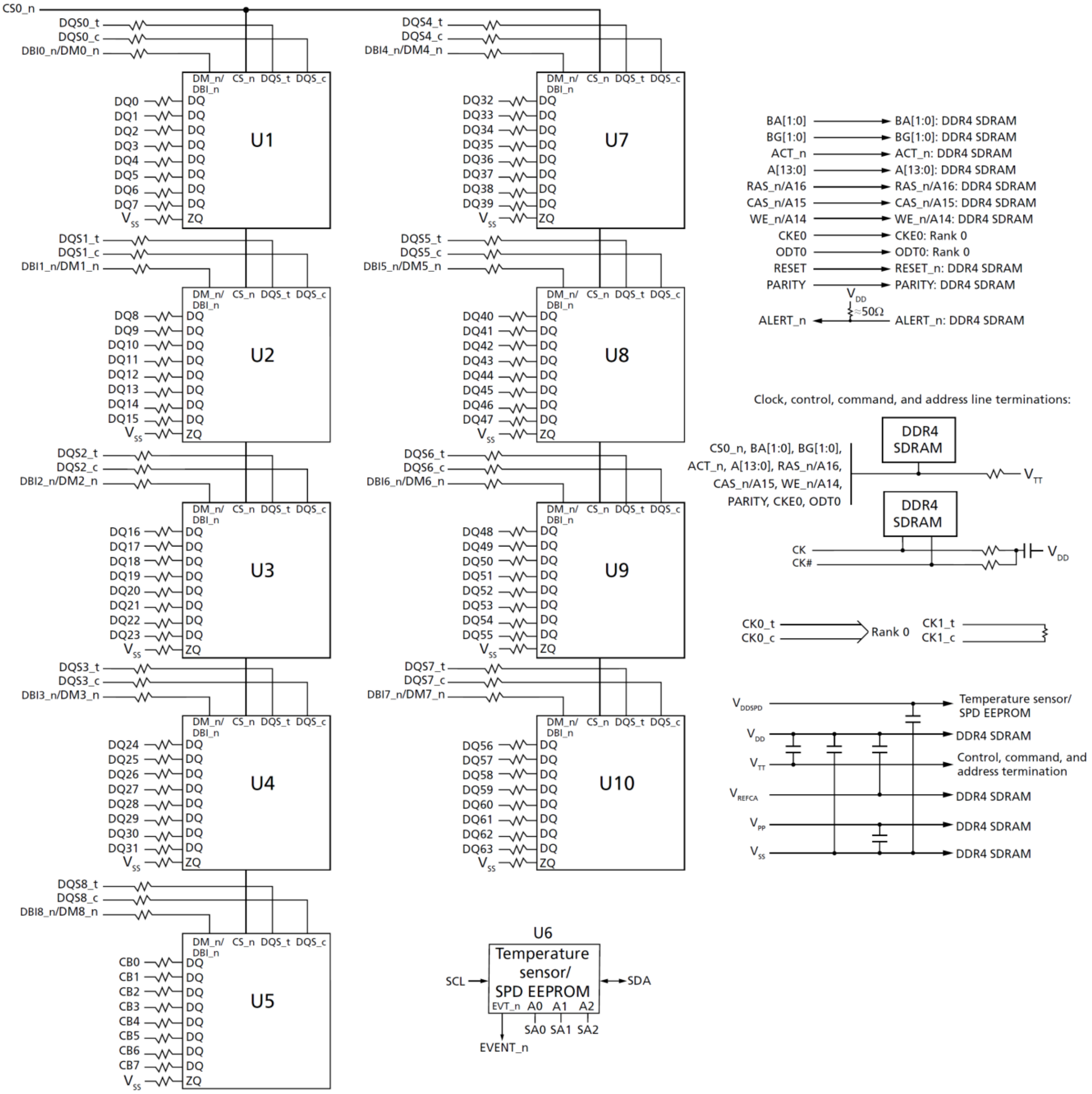
Note: 1. The ZQ ball on each DDR4 component is connected to an external 240Ω ±1% resistor that is tied to ground. It is used for the calibration of the component’s ODT and output driver.

Block Diagram(x8 2Ranks without ECC)



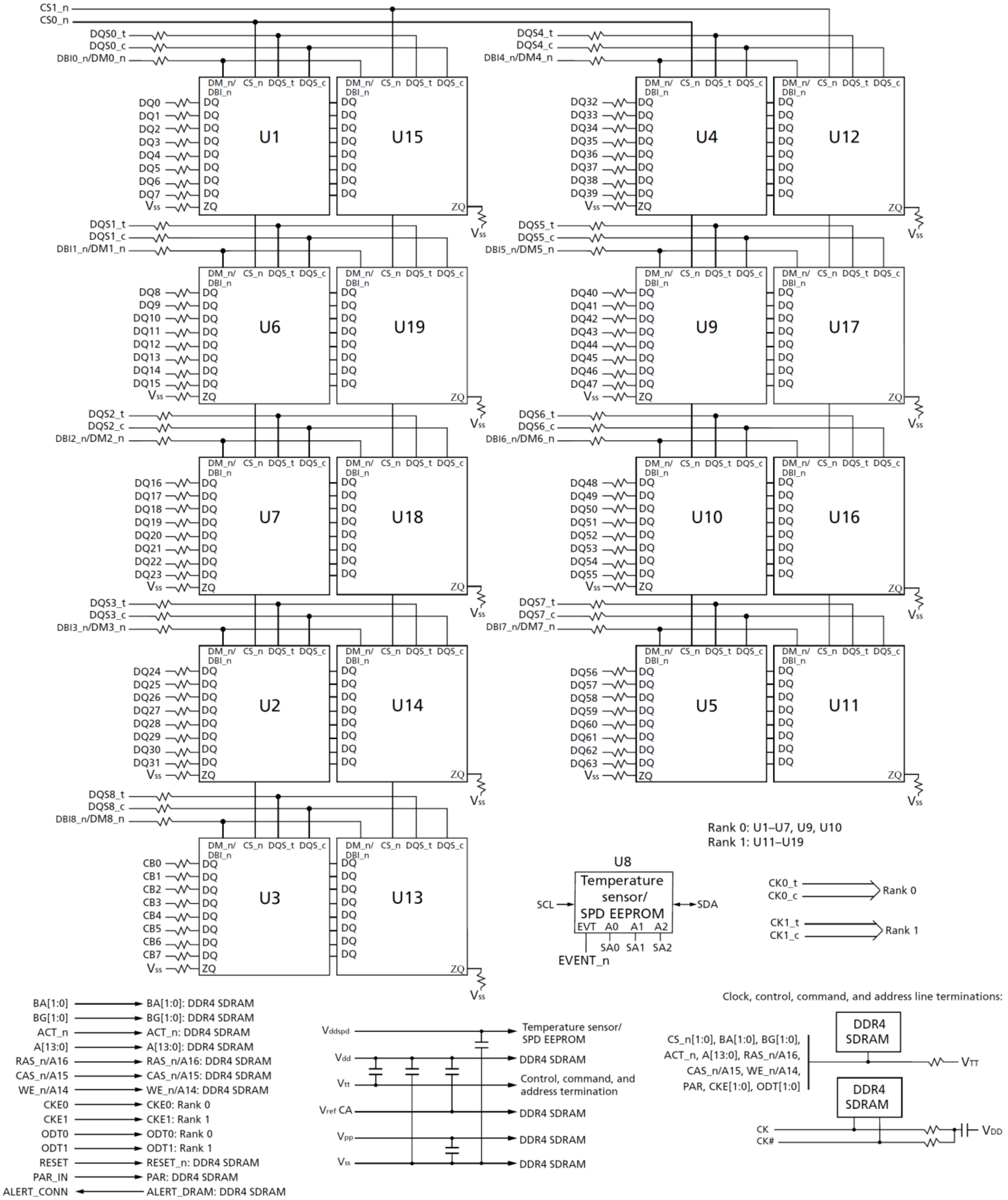
Note: 1. The ZQ ball on each DDR4 component is connected to an external 240Ω ±1% resistor that is tied to ground. It is used for the calibration of the component’s ODT and output driver.

Block Diagram(x8 1Rank with ECC)



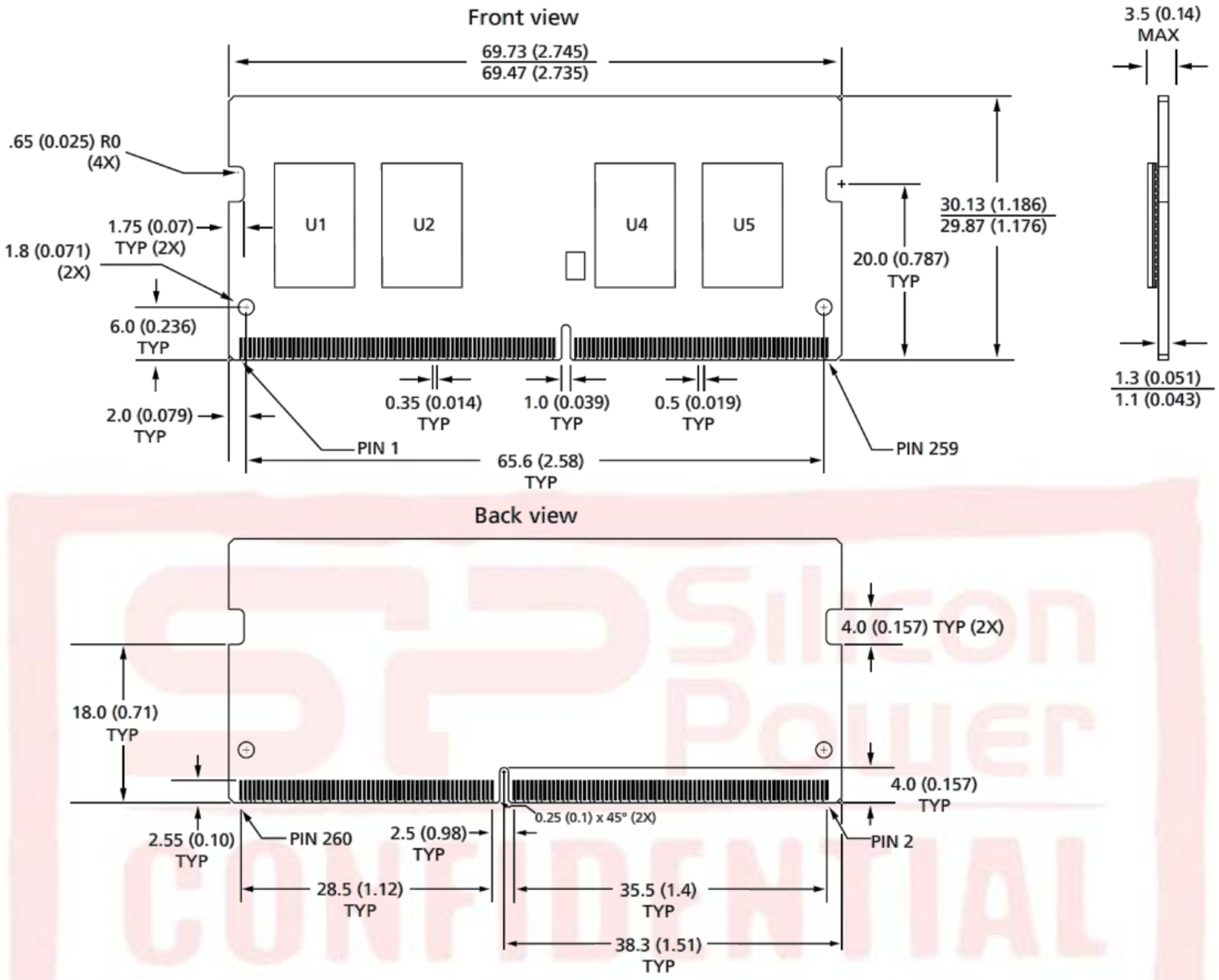
Note: 1. The ZQ ball on each DDR4 component is connected to an external 240Ω ±1% resistor that is tied to ground. It is used for the calibration of the component’s ODT and output driver.

Block Diagram(x8 2Ranks with ECC)



Note: 1. The ZQ ball on each DDR4 component is connected to an external 240Ω ±1% resistor that is tied to ground. It is used for the calibration of the component’s ODT and output driver.

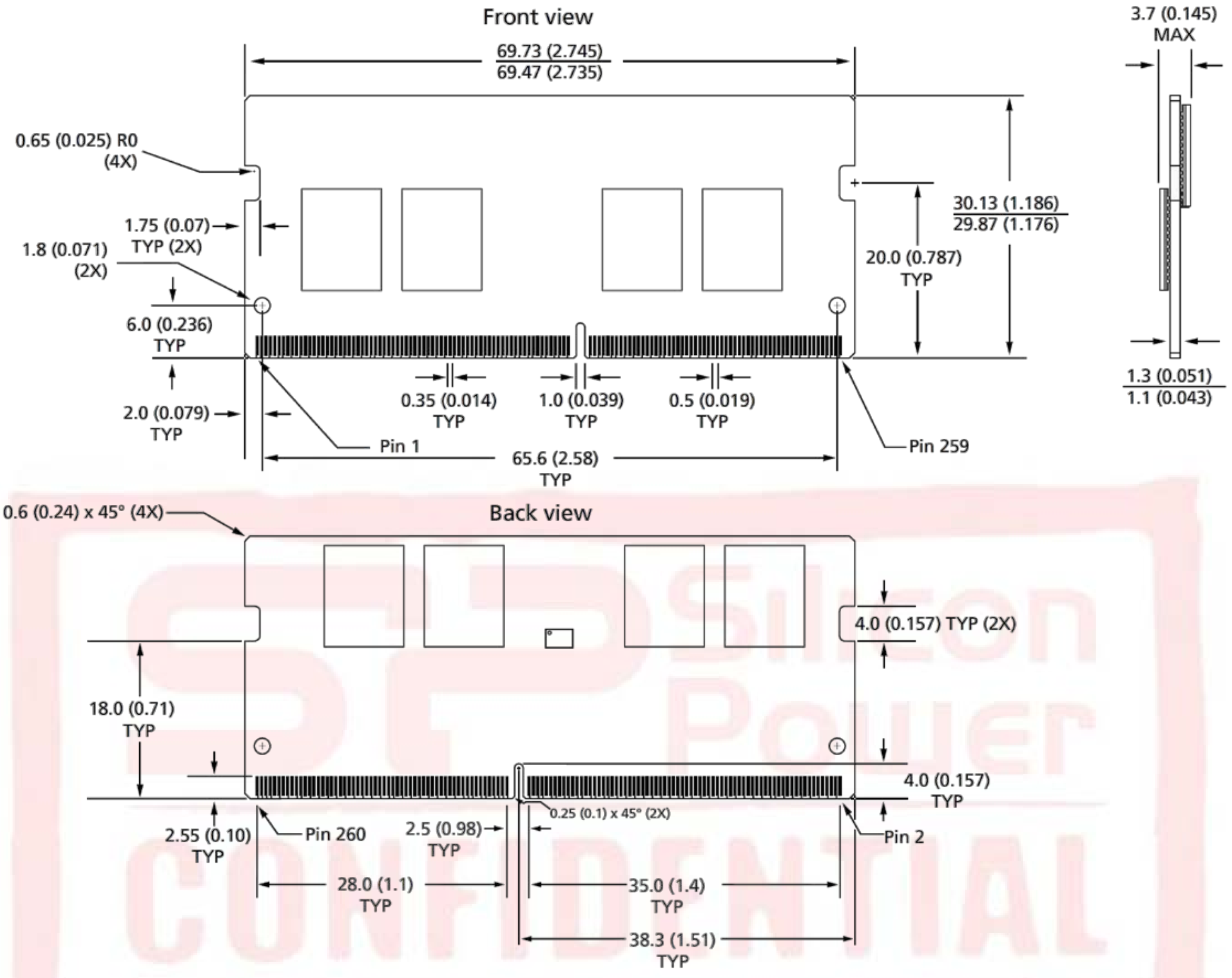
Simplified Mechanical Drawing (64bits SODIMM x16 1Rank)



Notes: 1. All dimensions are in millimeters (inches); MAX/MIN or typical (TYP) where noted.

Notes: 2. The dimensional diagram is for reference only.

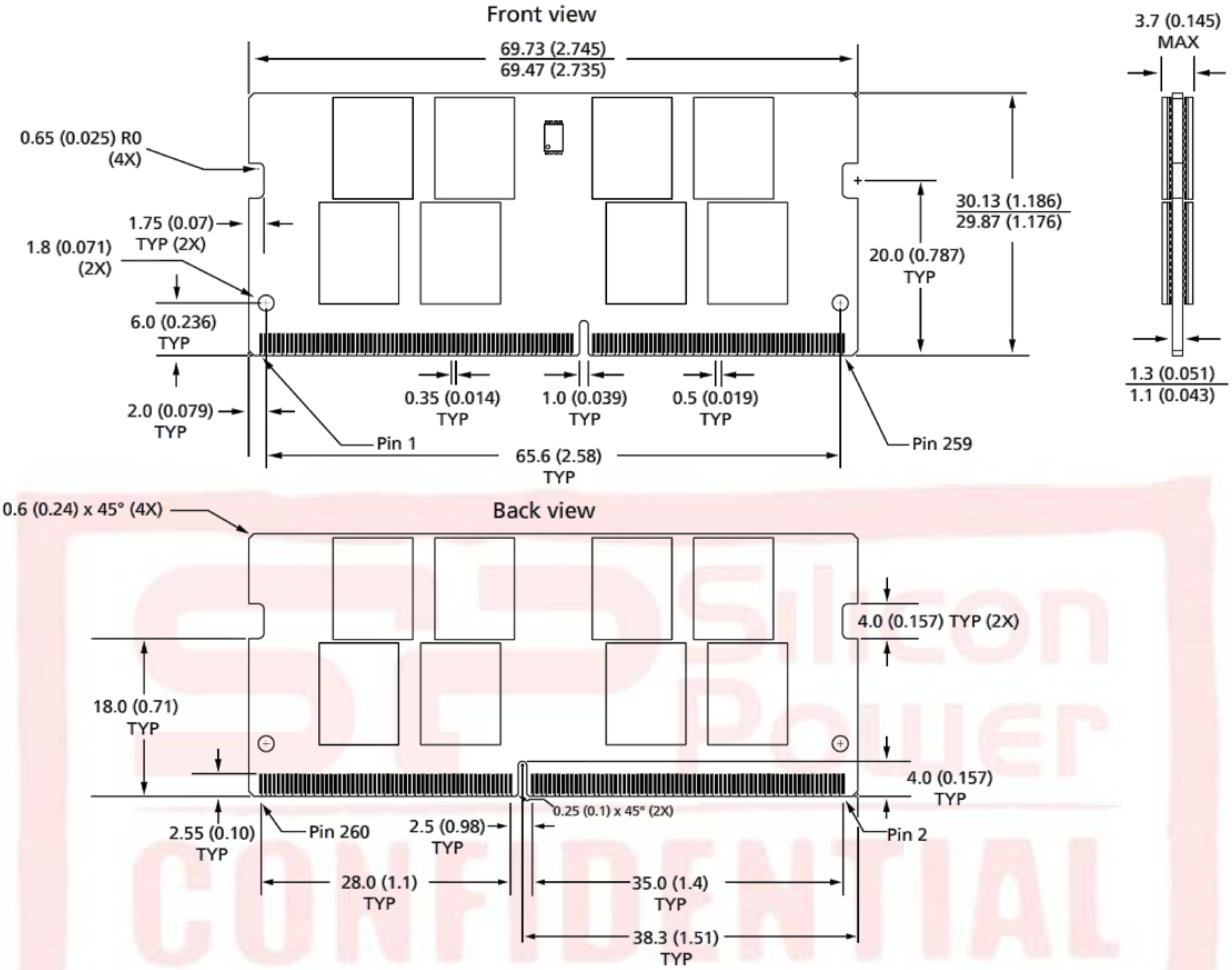
Simplified Mechanical Drawing (64bits SODIMM x8 1Rank)



Notes: 1. All dimensions are in millimeters (inches); MAX/MIN or typical (TYP) where noted.

Notes: 2. The dimensional diagram is for reference only.

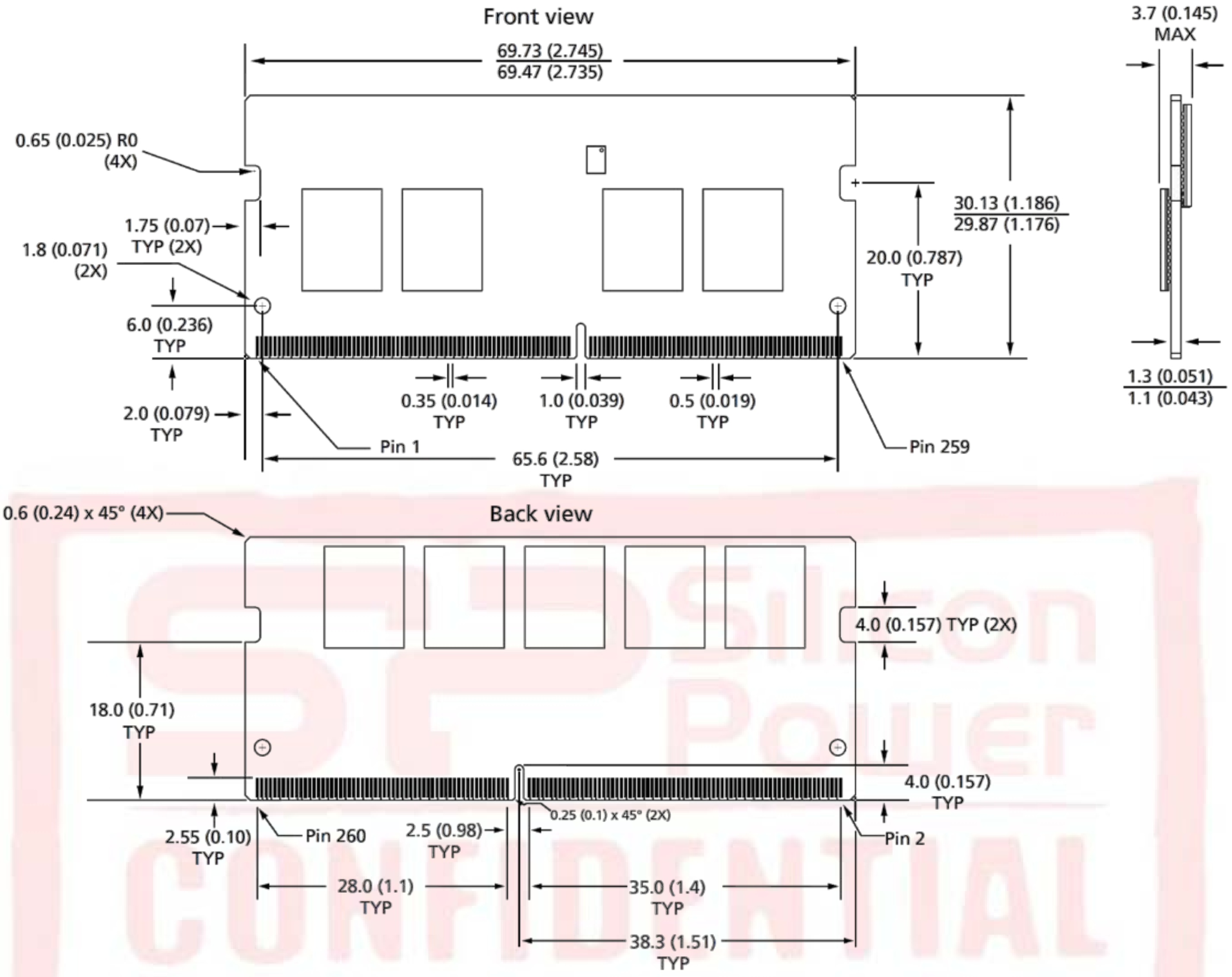
Simplified Mechanical Drawing (64bits SODIMM x8 2Ranks)



Notes: 1. All dimensions are in millimeters (inches); MAX/MIN or typical (TYP) where noted.

Notes: 2. The dimensional diagram is for reference only.

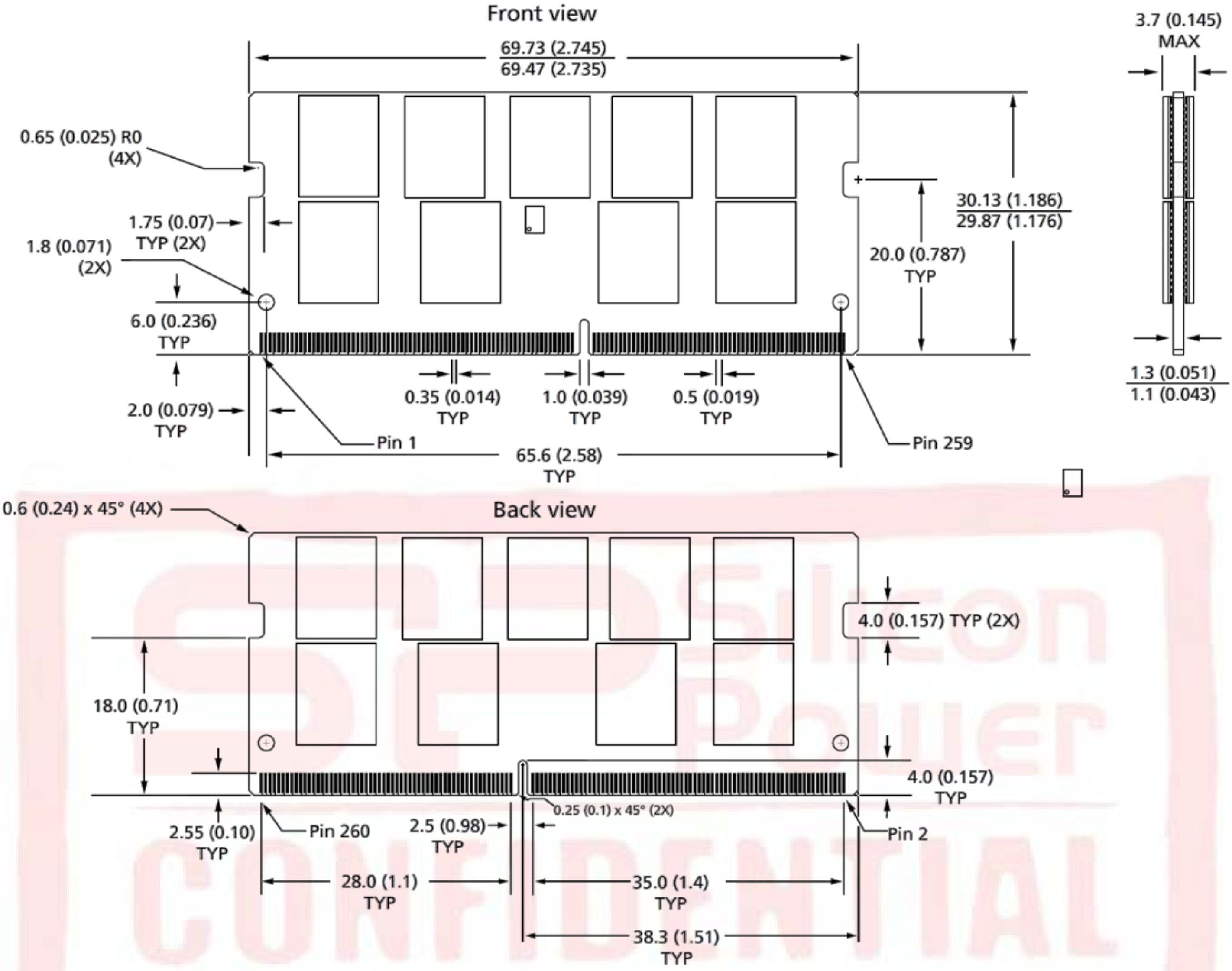
Simplified Mechanical Drawing (72bits SODIMM x8 1Rank)



Notes: 1. All dimensions are in millimeters (inches); MAX/MIN or typical (TYP) where noted.

Notes: 2. The dimensional diagram is for reference only.

Simplified Mechanical Drawing (72bits SODIMM x8 2Rank)



Notes: 1. All dimensions are in millimeters (inches); MAX/MIN or typical (TYP) where noted.

Notes: 2. The dimensional diagram is for reference only.