2N6497

High Voltage NPN Silicon Power Transistors

These devices are designed for high voltage inverters, switching regulators and line−operated amplifier applications. Especially well suited for switching power supply applications.

Features

- High Collector−Emitter Sustaining Voltage − $V_{CEO(sus)}$ = 250 Vdc (Min)
- Excellent DC Current Gain − h_{FE} = 10−75 @ I_C = 2.5 Adc
- Low Collector−Emitter Saturation Voltage @ I_C = 2.5 Adc − $V_{CE(sat)}$ = 1.0 Vdc (Max)
- Pb−Free Packages are Available*

MAXIMUM RATINGS (Note 1)

Rating	Symbol	Value	Unit
Collector−Emitter Voltage	V_{CEO}	250	Vdc
Collector−Base Voltage	V_{CB}	350	Vdc
Emitter−Base Voltage	V_{EB}	6.0	Vdc
Collector Current − Continuous − Peak	I_C	5.0 10	Adc
Base Current	I_B	2.0	Adc
Total Power Dissipation @ T_C = 25°C Derate above 25°C	P_D	80 0.64	W W/°C
Operating and Storage Junction Temperature Range	T_J, T_{stg}	−65 to +150	°C

THERMAL CHARACTERISTICS

Characteristics	Symbol	Max	Unit
Thermal Resistance, Junction−to−Case	$R_{\theta JC}$	1.56	°C/W

Stresses exceeding Maximum Ratings may damage the device. Maximum Ratings are stress ratings only. Functional operation above the Recommended Operating Conditions is not implied. Extended exposure to stresses above the Recommended Operating Conditions may affect device reliability.

1. Indicates JEDEC Registered Data.

*For additional information on our Pb−Free strategy and soldering details, please download the ON Semiconductor Soldering and Mounting Techniques Reference Manual, SOLDERRM/D.

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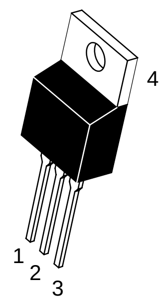
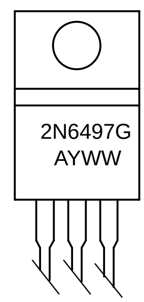
5 AMPERE POWER TRANSISTORS NPN SILICON 250 VOLTS − 80 WATTS

MARKING DIAGRAM



TO−220AB CASE 221A STYLE 1



2N6497 = Device Code
G = Pb−Free Package
A = Assembly Location
Y = Year
WW = Work Week

ORDERING INFORMATION

Device	Package	Shipping
2N6497	TO−220AB	50 Units / Rail
2N6497G	TO−220AB (Pb−Free)	50 Units / Rail

ELECTRICAL CHARACTERISTICS (T_C = 25°C unless otherwise noted) (Note 2)

Characteristic	Symbol	Min	Typ	Max	Unit
OFF CHARACTERISTICS					
Collector−Emitter Sustaining Voltage (Note 3) (I_C = 25 mAdc, I_B = 0)	$V_{CEO(sus)}$	250	−	−	Vdc
Collector Cutoff Current (V_{CE} = 350 Vdc, $V_{BE(off)}$ = 1.5 Vdc) (V_{CE} = 175 Vdc, $V_{BE(off)}$ = 1.5 Vdc, T_C = 100°C)	I_{CEX}	 − −	 − −	 1.0 10	mAdc
Emitter Cutoff Current (V_{BE} = 6.0 Vdc, I_C = 0)	I_{EBO}	−	−	1.0	mAdc
ON CHARACTERISTICS (Note 3)					
DC Current Gain (I_C = 2.5 Adc, V_{CE} = 10 Vdc) (I_C = 5.0 Adc, V_{CE} = 10 Vdc)	h_{FE}	 10 3.0	 − −	 75 −	−
Collector−Emitter Saturation Voltage (I_C = 2.5 Adc, I_B = 500 mAdc) (I_C = 5.0 Adc, I_B = 2.0 Adc)	$V_{CE(sat)}$	 − −	 − −	 1.0 5.0	Vdc
Base−Emitter Saturation Voltage (I_C = 2.5 Adc, I_B = 500 mAdc) (I_C = 5.0 Adc, I_B = 2.0 Adc)	$V_{BE(sat)}$	 − −	 − −	 1.5 2.5	Vdc
DYNAMIC CHARACTERISTICS					
Current−Gain − Bandwidth Product (I_C = 250 mAdc, V_{CE} = 10 Vdc, f = 1.0 MHz)	f_T	 5.0	 −	 −	MHz
Output Capacitance (V_{CB} = 10 Vdc, I_E = 0, f = 100 kHz)	C_{ob}	−	−	150	pF
SWITCHING CHARACTERISTICS					
Rise Time (V_{CC} = 125 Vdc, I_C = 2.5 Adc, I_{B1} = 0.5 Adc)	t_r	−	0.4	1.0	μs
Storage Time (V_{CC} = 125 Vdc, I_C = 2.5 Adc, V_{BE} = 5.0 Vdc, I_{B1} = I_{B2} = 0.5 Adc)	t_s	 −	 1.4	 2.5	μs
Fall Time (V_{CC} = 125 Vdc, I_C = 2.5 Adc, I_{B1} = I_{B2} = 0.5 Adc)	t_f	−	0.45	1.0	μs

2. Indicates JEDEC Registered Data.
3. Pulse Test: Pulse Width ≤ 300 μs, Duty Cycle ≤ 2.0%.

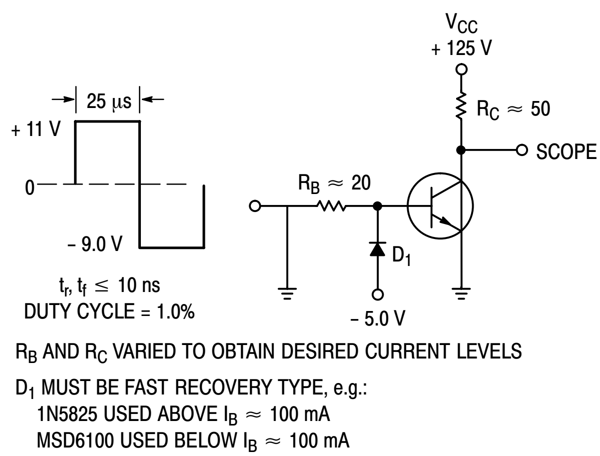


Figure 1. Switching Time Test Circuit

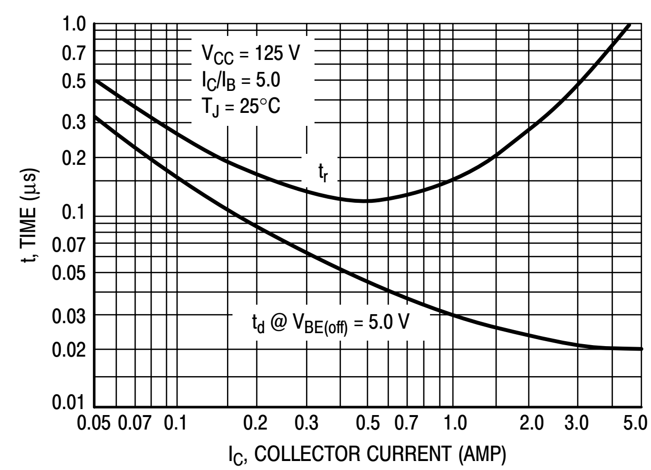


Figure 2. Turn−On Time

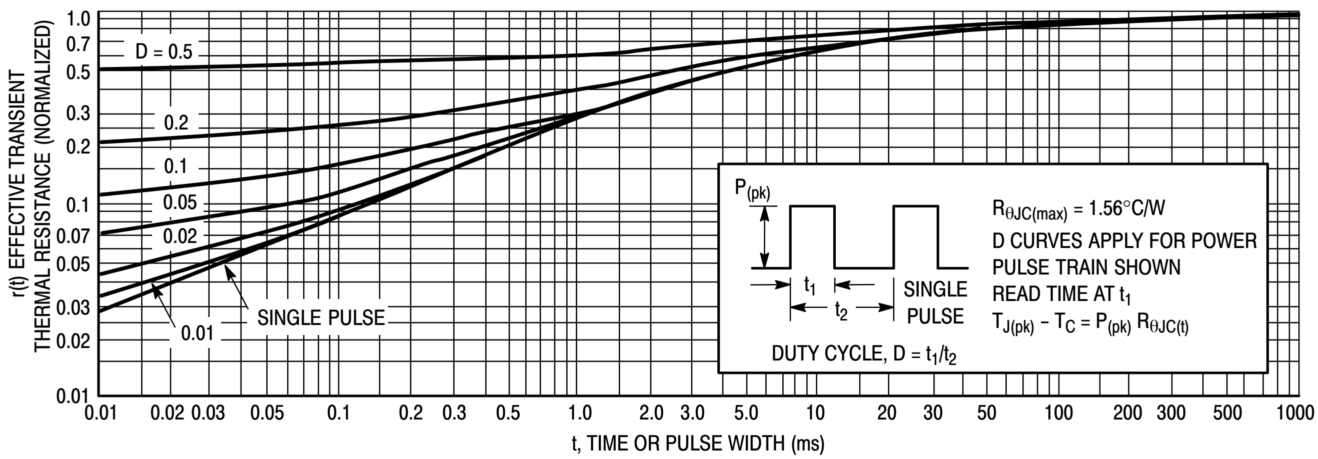


Figure 3. Thermal Response

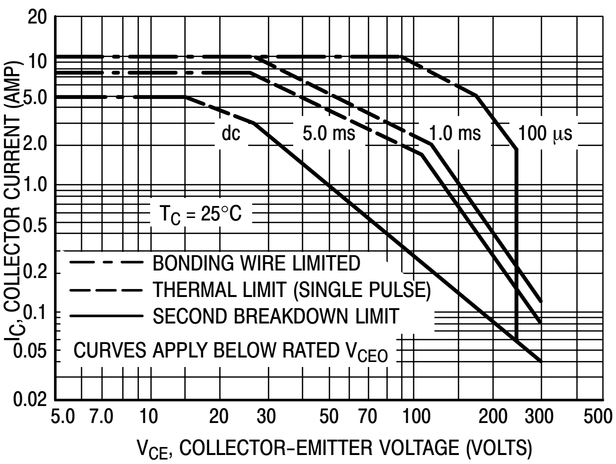


Figure 4. Active−Region Safe Operating Area

There are two limitations on the power handling ability of a transistor: average junction temperature and second breakdown. Safe operating area curves indicate $I_C - V_{CE}$ limits of the transistor that must be observed for reliable operation; i.e., the transistor must not be subjected to greater dissipation than the curves indicate.

The data of Figure 4 is based on $T_C = 25°C$; $T_{J(pk)}$ is variable depending on power level. Second breakdown pulse limits are valid for duty cycles to 10% provided $T_{J(pk)} \leq 150°C$. $T_{J(pk)}$ may be calculated from the data in Figure 3. At high case temperatures, thermal limitations will reduce the power that can be handled to values less than the limitations imposed by second breakdown. Second breakdown limitations do not derate the same as thermal limitations. Allowable current at the voltage shown on Figure 4 may be found at any case temperature by using the appropriate curve on Figure 6.

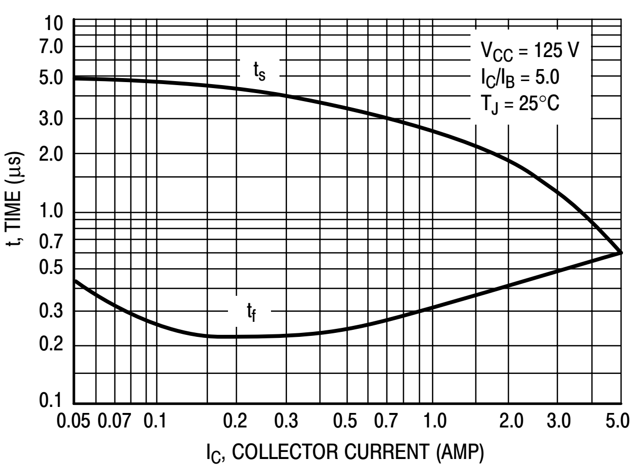


Figure 5. Turn−Off Time

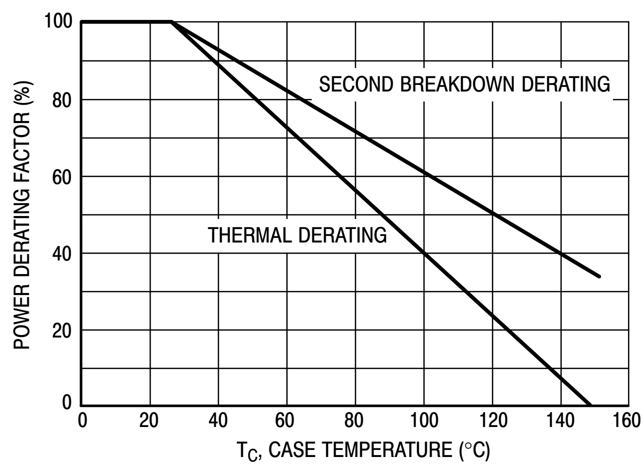


Figure 6. Power Derating

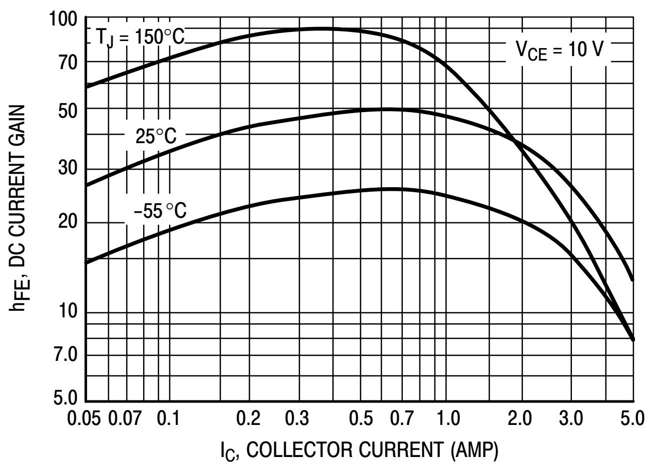


Figure 7. DC Current Gain

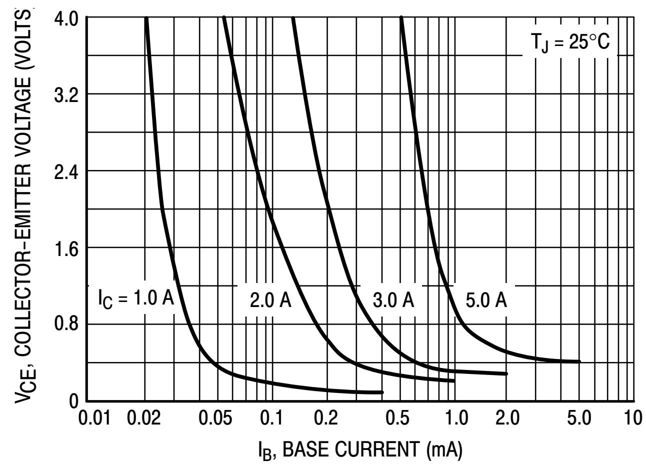


Figure 8. Collector Saturation Region

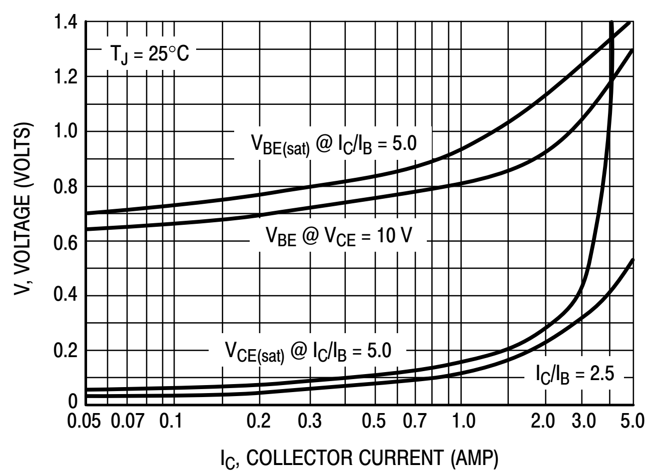


Figure 9. “On” Voltages

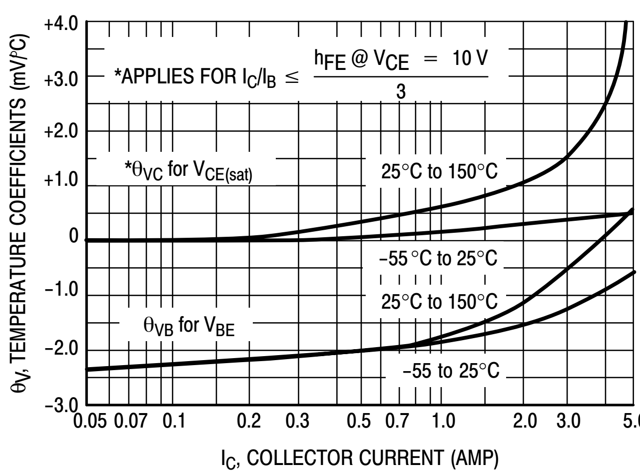


Figure 10. Temperature Coefficients

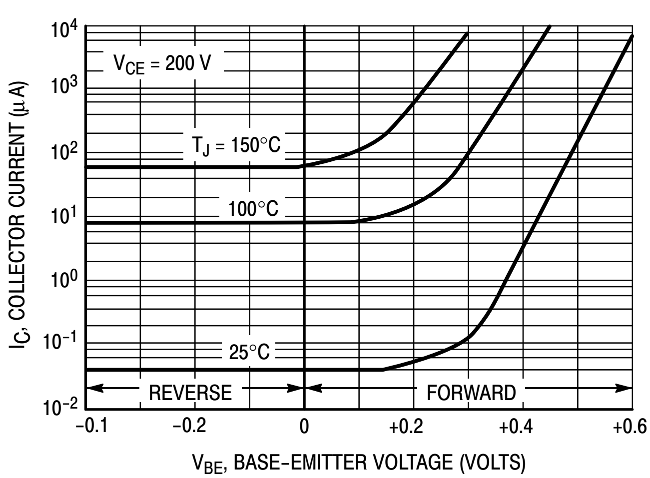


Figure 11. Collector Cutoff Region

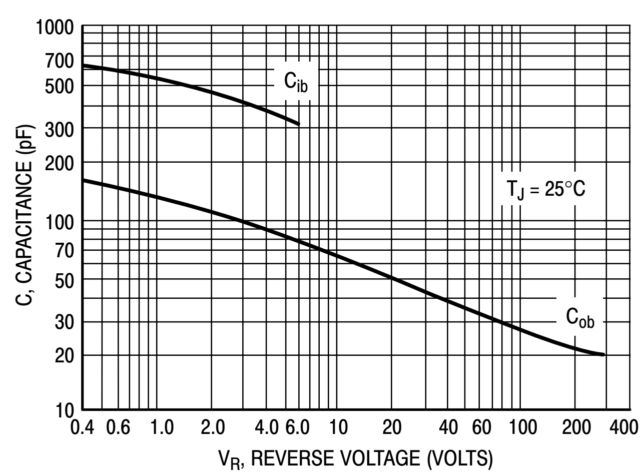


Figure 12. Capacitance

ADDITIONAL INFORMATION

TECHNICAL PUBLICATIONS:
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