PDTA143ZM

50 V, 100 mA PNP resistor-equipped transistor; R1 = 4.7 kΩ, R2 = 47 kΩ

23 January 2024 Product data sheet

1. General description

PNP Resistor-Equipped Transistor (RET) in an ultra small SOT883 (SC-101) Surface-Mounted Device (SMD) plastic package.

NPN complement: PDTC143ZM

2. Features and benefits

- 100 mA output current capability
- Built-in bias resistors
- Simplifies circuit design
- Reduces component count
- Reduces pick and place costs
- AEC-Q101 qualified

3. Applications

- Digital application in automotive and industrial segments
- Cost-saving alternative for BC847/857 series in digital applications
- Controlling IC inputs
- Switching loads

4. Quick reference data

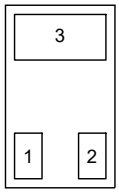
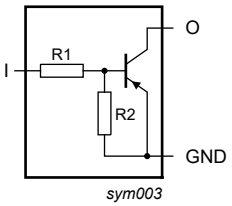
Table 1. Quick reference data

Symbol	Parameter	Conditions		Min	Typ	Max	Unit
V_{CEO}	collector-emitter voltage	open base		-	-	-50	V
I_O	output current			-	-	-100	mA
R1	bias resistor 1 (input)	T_{amb} = 25 °C	[1]	3.3	4.7	6.1	kΩ
R2/R1	bias resistor ratio		[1]	8	10	12	

[1] See section "Test information" for resistor calculation and test conditions

5. Pinning information

Table 2. Pinning information

Pin	Symbol	Description	Simplified outline	Graphic symbol
1	I	input (base)	 Transparent top view **DFN1006-3 (SOT883)**	
2	GND	ground (emitter)		
3	O	output (collector)		

6. Ordering information

Table 3. Ordering information

Type number	Package		
	Name	Description	Version
PDTA143ZM	DFN1006-3	plastic, leadless ultra small package; 3 terminals; 0.35 mm pitch; 1 mm x 0.6 mm x 0.48 mm body	SOT883

7. Marking

Table 4. Marking codes

Type number	Marking code
PDTA143ZM	DP

8. Limiting values

Table 5. Limiting values

In accordance with the Absolute Maximum Rating System (IEC 60134).

Symbol	Parameter	Conditions		Min	Max	Unit
V_{CBO}	collector-base voltage	open emitter		-	-50	V
V_{CEO}	collector-emitter voltage	open base		-	-50	V
V_{EBO}	emitter-base voltage	open collector		-	-5	V
V_I	input voltage			-30	5	V
I_O	output current			-	-100	mA
P_{tot}	total power dissipation	$T_{amb} \leq 25$ °C	[1] [2]	-	250	mW
T_j	junction temperature			-	150	°C
T_{amb}	ambient temperature			-65	150	°C
T_{stg}	storage temperature			-65	150	°C

[1] Reflow soldering is the only recommended soldering method.
[2] Device mounted on an FR4 Printed-Circuit Board (PCB) with 70 µm copper strip line, standard footprint.

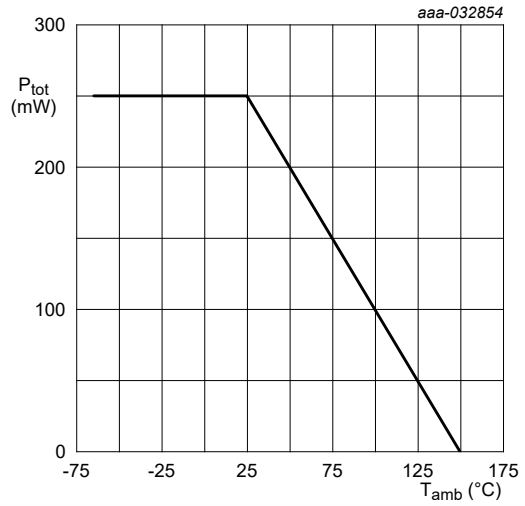


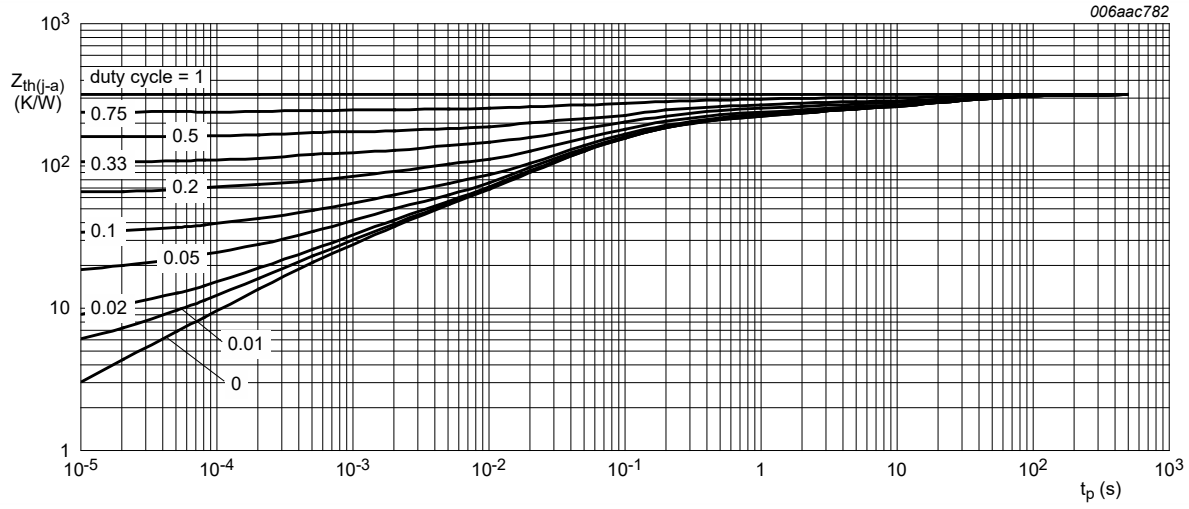
Fig. 1. Power derating curve

9. Thermal characteristics

Table 6. Thermal characteristics

Symbol	Parameter	Conditions		Min	Typ	Max	Unit
$R_{th(j-a)}$	thermal resistance from junction to ambient		[1] [2]	-	-	500	K/W

[1] Reflow soldering is the only recommended soldering method.
[2] Device mounted on an FR4 PCB with 70 µm copper strip line, standard footprint.



FR4 PCB, 70 µm copper strip line

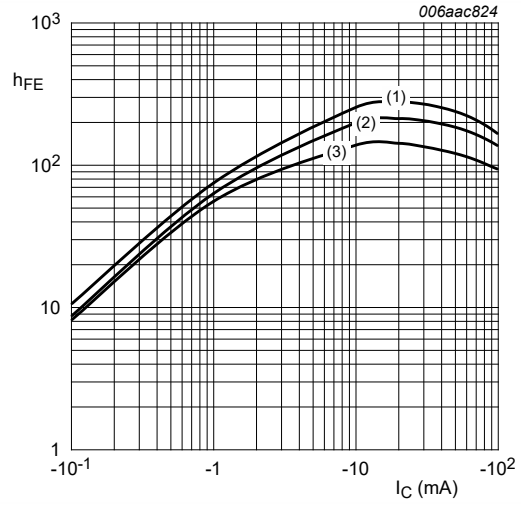
Fig. 2. Transient thermal impedance from junction to ambient as a function of pulse duration; typical values

10. Characteristics

Table 7. Characteristics

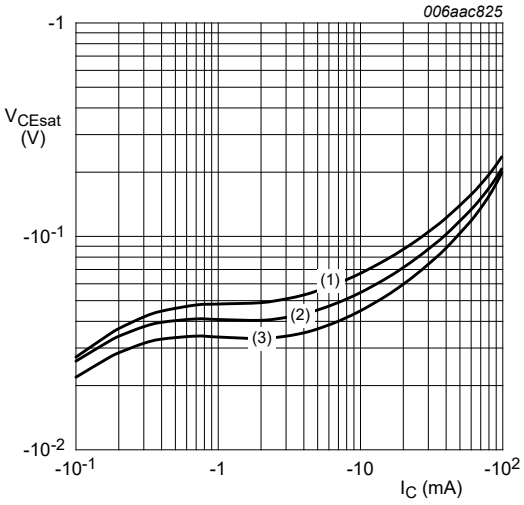
Symbol	Parameter	Conditions		Min	Typ	Max	Unit
$V_{(BR)CBO}$	collector-base breakdown voltage	I_C = -100 µA; I_E = 0 A; T_{amb} = 25 °C		-50	-	-	V
$V_{(BR)CEO}$	collector-emitter breakdown voltage	I_C = -2 mA; I_B = 0 A; T_{amb} = 25 °C		-50	-	-	V
$V_{(BR)EBO}$	emitter-base breakdown voltage	I_C = 0 A; I_E = -100 µA; T_{amb} = 25 °C		-5	-	-	V
I_{CBO}	collector-base cut-off current	V_{CB} = -50 V; I_E = 0 A; T_{amb} = 25 °C		-	-	-100	nA
I_{CEO}	collector-emitter cut-off current	V_{CE} = -30 V; I_B = 0 A; T_{amb} = 25 °C		-	-	-1	µA
		V_{CE} = -30 V; I_B = 0 A; T_j = 150 °C		-	-	-5	µA
I_{EBO}	emitter-base cut-off current	V_{EB} = -5 V; I_C = 0 A; T_{amb} = 25 °C		-	-	-170	µA
h_{FE}	DC current gain	V_{CE} = -5 V; I_C = -10 mA; T_{amb} = 25 °C		100	-	-	
V_{CEsat}	collector-emitter saturation voltage	I_C = -5 mA; I_B = -0.25 mA; T_{amb} = 25 °C		-	-	-100	mV
$V_{I(off)}$	off-state input voltage	V_{CE} = -5 V; I_C = -100 µA; T_{amb} = 25 °C		-	-0.6	-0.5	V
$V_{I(on)}$	on-state input voltage	V_{CE} = -0.3 V; I_C = -5 mA; T_{amb} = 25 °C		-1.3	-0.9	-	V
R1	bias resistor 1 (input)	T_{amb} = 25 °C	[1]	3.3	4.7	6.1	kΩ
R2/R1	bias resistor ratio		[1]	8	10	12	
C_c	collector capacitance	V_{CB} = -10 V; I_E = 0 A; i_e = 0 A; f = 1 MHz; T_{amb} = 25 °C		-	-	3	pF
f_T	transition frequency	V_{CE} = -5 V; I_C = -10 mA; f = 100 MHz; T_{amb} = 25 °C	[2]	-	180	-	MHz

[1] See section "Test information" for resistor calculation and test conditions
[2] Characteristics of built-in transistor



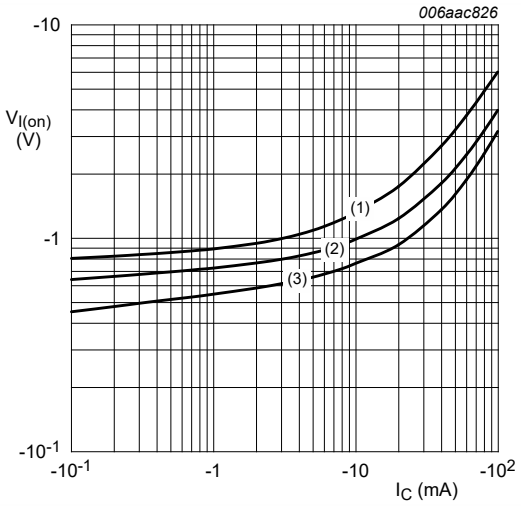
V_{CE} = -5 V
(1) T_{amb} = 100 °C
(2) T_{amb} = 25 °C
(3) T_{amb} = -40 °C

Fig. 3. DC current gain as a function of collector current; typical values



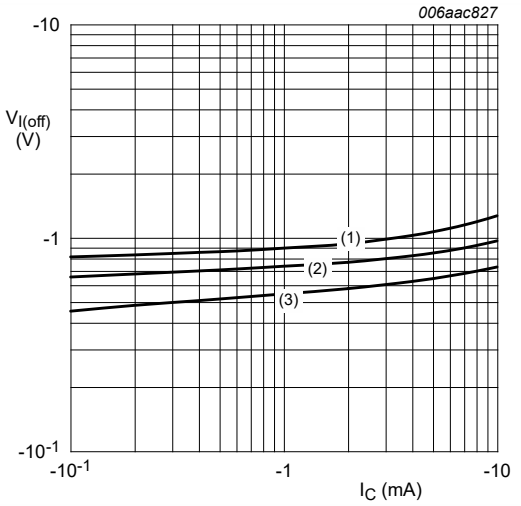
I_C/I_B = 20
(1) T_{amb} = 100 °C
(2) T_{amb} = 25 °C
(3) T_{amb} = -40 °C

Fig. 4. Collector-emitter saturation voltage as a function of collector current; typical values



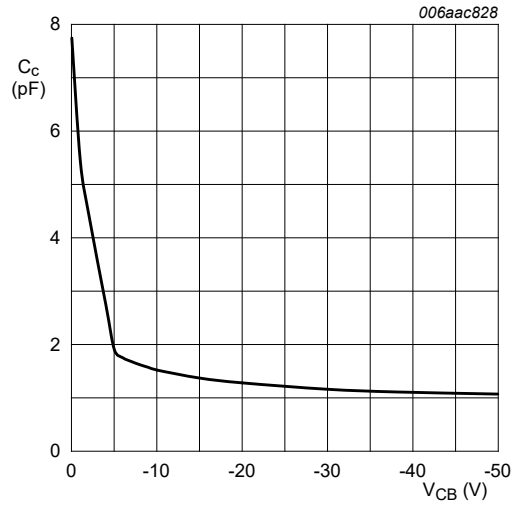
V_{CE} = -0.3 V
(1) T_{amb} = -40 °C
(2) T_{amb} = 25 °C
(3) T_{amb} = 100 °C

Fig. 5. On-state input voltage as a function of collector current; typical values



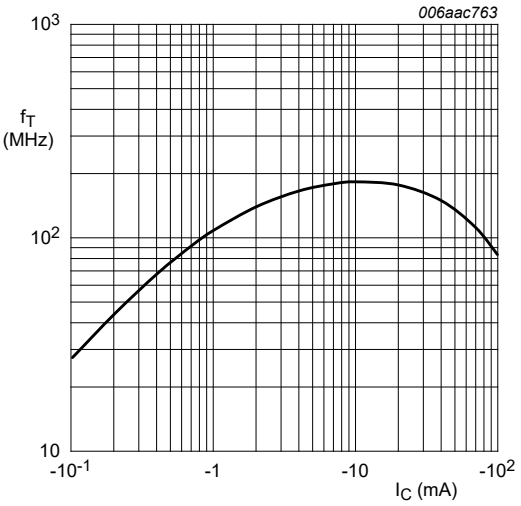
V_{CE} = -5 V
(1) T_{amb} = -40 °C
(2) T_{amb} = 25 °C
(3) T_{amb} = 100 °C

Fig. 6. Off-state input voltage as a function of collector current; typical values



f = 1 MHz; T_{amb} = 25 °C

Fig. 7. Collector capacitance as a function of collector-base voltage; typical values



V_{CE} = -5 V; T_{amb} = 25 °C

Fig. 8. Transition frequency as a function of collector current; typical values of built-in transistor

11. Test information

Quality information

This product has been qualified in accordance with the Automotive Electronics Council (AEC) standard *Q101 - Stress test qualification for discrete semiconductors*, and is suitable for use in automotive applications.

Resistor calculation

- Calculation of bias resistor 1 (R1)

$$R_1 = \frac{V(I_2) - V(I_1)}{I_2 - I_1}$$

- Calculation of bias resistor ratio (R2/R1)

$$\frac{R2}{R1} = \frac{V(I_4) - V(I_3)}{R1 \cdot (I_4 - I_3)} - 1$$

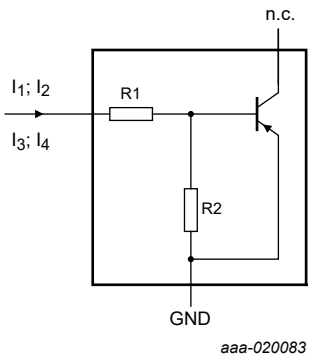


Fig. 9. PNP transistor: Resistor test circuit

Resistor test conditions

Table 8. Resistor test conditions

Type number	R1 (kΩ)	R2 (kΩ)	Test conditions			
			I_1	I_2	I_3	I_4
PDTA143ZM	4.7	47	-90 µA	-140 µA	55 µA	105 µA

12. Package outline

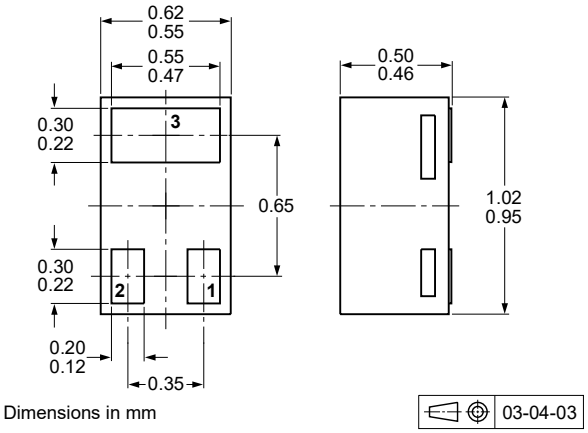


Fig. 10. Package outline DFN1006-3 (SOT883)

13. Soldering

Footprint information for reflow soldering of DFN1006-3 (SOT883) package **SOT883**

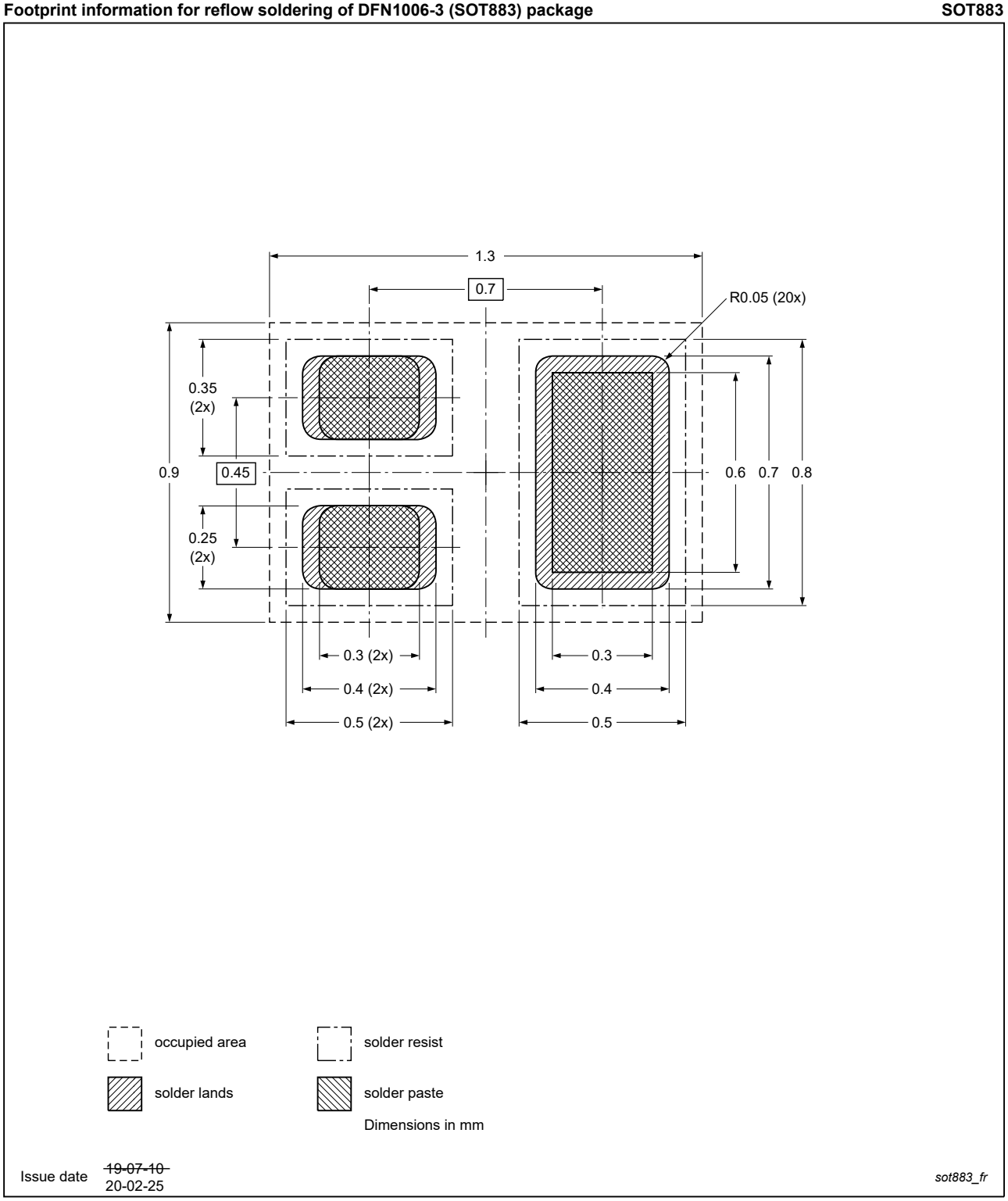


Fig. 11. Reflow soldering footprint for DFN1006-3 (SOT883)

14. Revision history

Table 9. Revision history

Data sheet ID	Release date	Data sheet status	Change notice	Supersedes
PDTA143ZM v.8	20240123	Product data sheet	-	PDTA143Z_SER v.7
Modification:	• Family data sheet reduced to single type data sheet. • Packing information removed.			
PDTA143Z_SER v.7	20111205	Product data sheet	-	PDTA143Z_SERIES v.6
PDTA143Z_SERIES v.6	20040805	Product data sheet	-	PDTA143Z_SERIES v.5
PDTA143Z_SERIES v.5	20030908	Product specification	-	PDTA143Z_SERIES v.4
PDTA143Z_SERIES v.4	20030410	Product specification	-	-

15. Legal information

Data sheet status

Document status [1][2]	Product status [3]	Definition
Objective [short] data sheet	Development	This document contains data from the objective specification for product development.
Preliminary [short] data sheet	Qualification	This document contains data from the preliminary specification.
Product [short] data sheet	Production	This document contains the product specification.

[1] Please consult the most recently issued document before initiating or completing a design.
[2] The term 'short data sheet' is explained in section "Definitions".
[3] The product status of device(s) described in this document may have changed since this document was published and may differ in case of multiple devices. The latest product status information is available on the internet at https://www.nexperia.com.

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