# PDTC114EU

NPN resistor-equipped transistors; R1 = 10 kΩ, R2 = 10 kΩ
9 October 2024

Product data sheet

### 1. General description

NPN Resistor-Equipped Transistor (RET) in a very small SOT323 (SC-70) Surface-Mounted Device (SMD) plastic package.

### 2. Features and benefits

- 100 mA output current capability
- Built-in bias resistors
- · Simplifies circuit design
- Reduces component count
- Reduces pick and place costs

### 3. Applications

- · Digital application in automotive and industrial segments
- Control of IC inputs
- · Cost-saving alternative for BC847/857 series in digital applications
- · Switching loads

### 4. Quick reference data

Table 1. Quick reference data

Symbol	Parameter	Conditions	Min	Тур	Max	Unit
V <sub>CEO</sub>	collector-emitter voltage	open base	-	-	50	V
Io	output current		-	-	100	mA
R1	bias resistor 1 (input)		7	10	13	kΩ
R2/R1	bias resistor ratio		8.0	1	1.2	

## 5. Pinning information

**Table 2. Pinning information** 

Pin	Symbol	Description	Simplified outline	Graphic symbol
1	I	input (base)	<u></u> 3	
2	GND	ground (emitter)		R <sub>1</sub>
3	0	output (collector)	SC-70 (SOT323)	GND————————————————————————————————————



### NPN resistor-equipped transistors; R1 = 10 k $\Omega$ , R2 = 10 k $\Omega$

# 6. Ordering information

#### **Table 3. Ordering information**

Type number Package				
	Name	Description	Version	
PDTC114EU	SC-70	plastic, surface-mounted package; 3 leads; 1.3 mm pitch; 2 mm x 1.25 mm x 0.95 mm body	SOT323	

### 7. Marking

#### Table 4. Marking codes

Type number	Marking code[1]
PDTC114EU	809

<sup>[1] % =</sup> placeholder for manufacturing site code

### 8. Limiting values

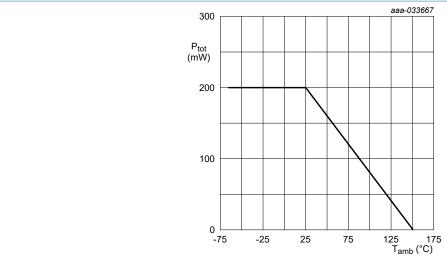
#### Table 5. Limiting values

In accordance with the Absolute Maximum Rating System (IEC 60134).

Symbol	Parameter	Conditions		Min	Max	Unit
$V_{CBO}$	collector-base voltage	open emitter		-	50	V
V <sub>CEO</sub>	collector-emitter voltage	open base		-	50	V
$V_{EBO}$	emitter-base voltage	open collector		-	10	V
VI	input voltage			-10	40	V
I <sub>O</sub>	output current			-	100	mA
P <sub>tot</sub>	total power dissipation	T <sub>amb</sub> ≤ 25 °C	[1]	-	200	mW
Tj	junction temperature			-	150	°C
T <sub>amb</sub>	ambient temperature			-65	150	°C
T <sub>stg</sub>	storage temperature			-65	150	°C

<sup>[1]</sup> Device mounted on an FR4 Printed-Circuit Board (PCB), single-sided copper, tin-plated and standard footprint.

### NPN resistor-equipped transistors; R1 = 10 k $\Omega$ , R2 = 10 k $\Omega$



FR4 PCB, single-sided, 35 µm copper, tin-plated and standard footprint

Fig. 1. Power derating curve

### 9. Thermal characteristics

**Table 6. Thermal characteristics** 

Symbol	Parameter	Conditions		Min	Тур	Max	Unit
ui(j-a)	thermal resistance from junction to ambient	in free air	[1]	-	-	625	K/W

[1] Device mounted on an FR4 PCB, single-sided copper, tin-plated and standard footprint.

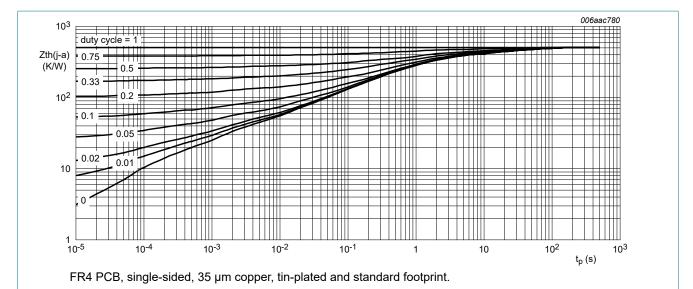


Fig. 2. Transient thermal impedance from junction to ambient as a function of pulse duration; typical values

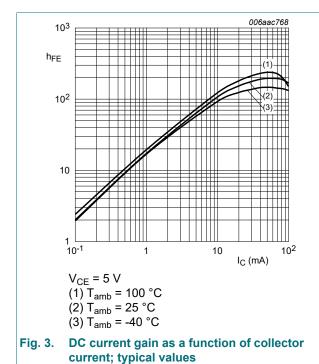
### NPN resistor-equipped transistors; R1 = 10 k $\Omega$ , R2 = 10 k $\Omega$

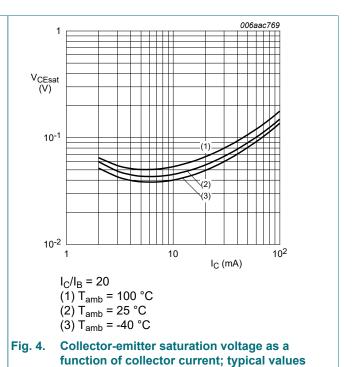
### 10. Characteristics

**Table 7. Characteristics** 

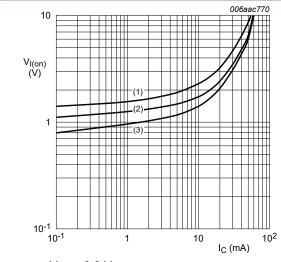
Symbol	Parameter	Conditions		Min	Тур	Max	Unit
$V_{(BR)CBO}$	collector-base breakdown voltage	$I_C = 100 \ \mu A; I_E = 0 \ A; T_{amb} = 25 \ ^{\circ}C$		50	-	-	V
$V_{(BR)CEO}$	collector-emitter breakdown voltage	<sub>C</sub> = 2 mA; I <sub>B</sub> = 0 A; T <sub>amb</sub> = 25 °C		50	-	-	V
I <sub>CBO</sub>	collector-base cut-off current	/ <sub>CB</sub> = 50 V; I <sub>E</sub> = 0 A; T <sub>amb</sub> = 25 °C		-	-	100	nA
I <sub>CEO</sub>	collector-emitter cut-off	V <sub>CE</sub> = 30 V; I <sub>B</sub> = 0 A; T <sub>amb</sub> = 25 °C		-	-	100	nA
	current	V <sub>CE</sub> = 30 V; I <sub>B</sub> = 0 A; T <sub>j</sub> = 150 °C		-	-	5	μΑ
I <sub>EBO</sub>	emitter-base cut-off current	$V_{EB} = 5 \text{ V}; I_{C} = 0 \text{ A}; T_{amb} = 25 \text{ °C}$		-	-	400	μΑ
h <sub>FE</sub>	DC current gain	V <sub>CE</sub> = 5 V; I <sub>C</sub> = 5 mA; T <sub>amb</sub> = 25 °C		30	-	-	
V <sub>CEsat</sub>	collector-emitter saturation voltage	$I_C = 10 \text{ mA}; I_B = 0.5 \text{ mA}; T_{amb} = 25 \text{ °C}$		-	-	150	mV
V <sub>I(off)</sub>	off-state input voltage	V <sub>CE</sub> = 5 V; I <sub>C</sub> = 100 μA; T <sub>amb</sub> = 25 °C		-	1.1	0.8	V
V <sub>I(on)</sub>	on-state input voltage	$V_{CE} = 0.3 \text{ V}; I_{C} = 10 \text{ mA}; T_{amb} = 25 ^{\circ}\text{C}$		2.5	1.8	-	V
R1	bias resistor 1 (input)			7	10	13	kΩ
R2/R1	bias resistor ratio			0.8	1	1.2	
C <sub>c</sub>	collector capacitance	$V_{CB}$ = 10 V; $I_{E}$ = 0 A; $i_{e}$ = 0 A; f = 1 MHz; $T_{amb}$ = 25 °C		-	-	2.5	pF
f <sub>T</sub>	transition frequency	$V_{CE} = 5 \text{ V}; I_{C} = 10 \text{ mA}; f = 100 \text{ MHz};$ $T_{amb} = 25 \text{ °C}$	[1]	-	230	-	MHz

#### [1] Characteristics of built-in transistor.





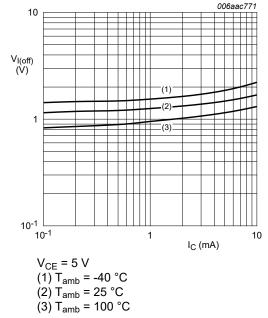
#### NPN resistor-equipped transistors; R1 = 10 k $\Omega$ , R2 = 10 k $\Omega$



 $V_{CE} = 0.3 V$ 

(1) T<sub>amb</sub> = -40 °C (2) T<sub>amb</sub> = 25 °C (3) T<sub>amb</sub> = 100 °C





Off-state input voltage as a function of collector current; typical values

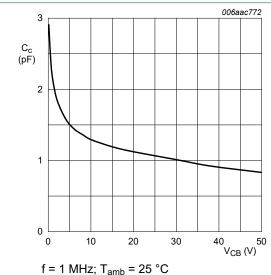
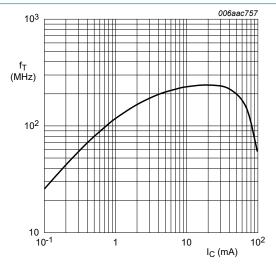


Fig. 7. Collector capacitance as a function of collector- Fig. 8. base voltage; typical values



 $V_{CE}$  = 5 V;  $T_{amb}$  = 25 °C

Transition frequency as a function of collector current; typical values of built-in transistor

NPN resistor-equipped transistors; R1 = 10 k $\Omega$ , R2 = 10 k $\Omega$ 

### 11. Test information

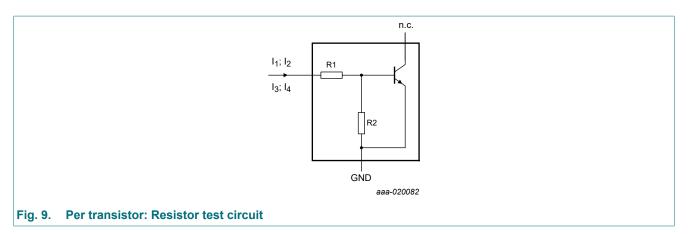
#### **Resistor calculation**

Calculation of bias resistor 1 (R1)

$$R_{I} = \frac{V(I_{2}) - V(I_{1})}{I_{2} - I_{1}}$$

· Calculation of bias resistor ratio (R2/R1)

$$\frac{R2}{R1} = \frac{V(I4) - V(I3)}{R1 \cdot (I4 - I3)} - 1$$

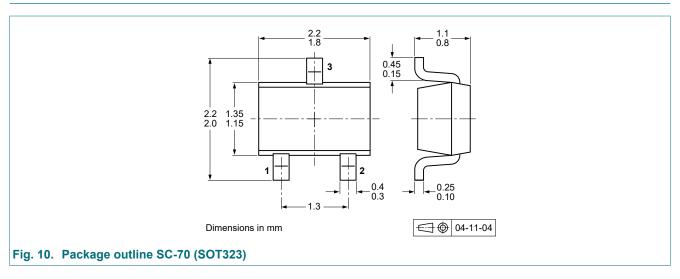


### **Resistor test conditions**

**Table 8. Resistor test conditions** 

Type number	R1 (kΩ)	R2 (kΩ)	Test conditions			
			I <sub>1</sub>	l <sub>2</sub>	l <sub>3</sub>	14
PDTC114EU	10	10	350 μΑ	450 μA	-350 μΑ	-450 μA

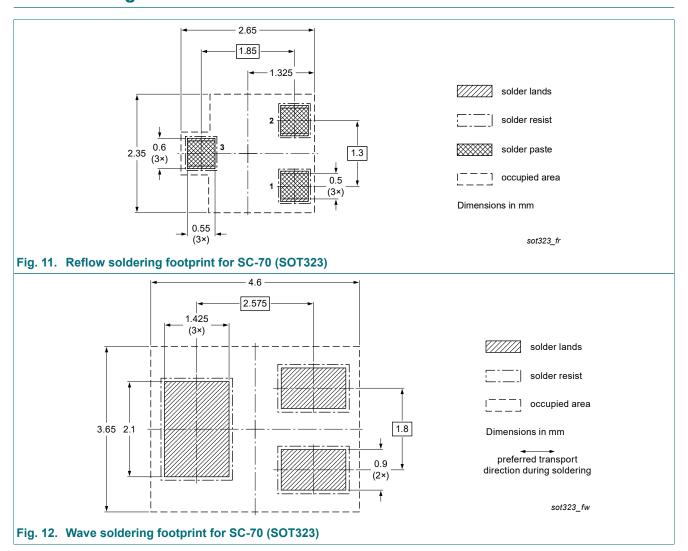
# 12. Package outline



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### NPN resistor-equipped transistors; R1 = 10 k $\Omega$ , R2 = 10 k $\Omega$

# 13. Soldering



### NPN resistor-equipped transistors; R1 = 10 k $\Omega$ , R2 = 10 k $\Omega$

# 14. Revision history

### Table 9. Revision history

Table 3. Revision history							
Data sheet ID	Release date	Data sheet status	Change notice	Supersedes			
PDTC114EU v.15	20241009	Product data sheet	-	PDTC114EU v.14			
Modification:		nanged to non-automotive qual Q) product alternative(s).	ification. Please	refer to nexperia.com for			
PDTC114EU v.14	20230602	Product data sheet	-	PDTC114EU v.13			
PDTC114EU v.13	20220812	Product data sheet	-	PDTC114E_SER v.12			
PDTC114E_SER v.12	20111221	Product data sheet	-	PDTC114E_SER v.11			
PDTC114E_SER v.11	20111121	Product data sheet	-	PDTC114E_SERIES v.10			
PDTC114E_SERIES v.10	20040805	Product specification	-	PDTC114E_SERIES v.9			
PDTC114E_SERIES v.9	20030410	Product specification	-	-			

#### NPN resistor-equipped transistors; R1 = 10 k $\Omega$ , R2 = 10 k $\Omega$

### 15. Legal information

#### **Data sheet status**

Document status [1][2]	Product status [3]	Definition
Objective [short] data sheet	Development	This document contains data from the objective specification for product development.
Preliminary [short] data sheet	Qualification	This document contains data from the preliminary specification.
Product [short] data sheet	Production	This document contains the product specification.

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