

PDTC114YU-Q

50 V, 100 mA NPN resistor-equipped transistor; R1 = 10 k Ω , R2 = 47 k Ω

25 April 2023

Product data sheet

1. General description

NPN Resistor-Equipped Transistor (RET) in a very small SOT323 (SC-70) Surface-Mounted Device (SMD) plastic package.

PNP complement: PDTA114YU

2. Features and benefits

- 100 mA output current capability
- · Built-in bias resistors
- · Simplifies circuit design
- Reduces component count
- Reduces pick and place costs
- Qualified according to AEC-Q101 and recommended for use in automotive applications

3. Applications

- · Digital application in automotive and industrial segments
- Cost-saving alternative for BC847-Q series in digital applications
- · Controlling IC inputs
- Switching loads

4. Quick reference data

Table 1. Quick reference data

Symbol	Parameter	Conditions		Min	Тур	Max	Unit
V _{CEO}	collector-emitter voltage	open base		-	-	50	V
Io	output current			-	-	100	mA
R1	bias resistor 1 (input)		[1]	7	10	13	kΩ
R2/R1	bias resistor ratio		[1]	3.7	4.7	5.7	

[1] See "Section 11: Test information" for resistor calculation and test conditions.



5. Pinning information

Table 2. Pinning information

Pin	Symbol	Description	Simplified outline	Graphic symbol
1	1	input (base)	3	
2	GND	ground (emitter)		R ₁
3	0	output (collector)	3C-70 (SOT323)	GND R2

6. Ordering information

Table 3. Ordering information

Type number	Package						
	Name	Description	Version				
PDTC114YU-Q	SC-70	plastic, surface-mounted package; 3 leads; 1.3 mm pitch; 2 mm x 1.25 mm x 0.95 mm body	SOT323				

7. Marking

Table 4. Marking codes

Type number	Marking code[1]
PDTC114YU-Q	%30

^{[1] % =} placeholder for manufacturing site code

8. Limiting values

Table 5. Limiting values

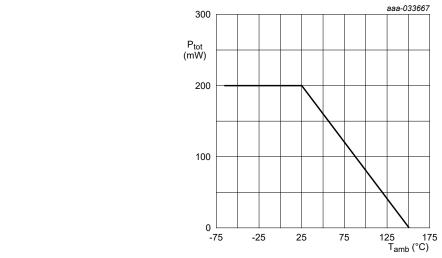
In accordance with the Absolute Maximum Rating System (IEC 60134).

Symbol	Parameter	Conditions		Min	Max	Unit
V_{CBO}	collector-base voltage	open emitter		-	50	V
V_{CEO}	collector-emitter voltage	open base		-	50	V
V _{EBO}	emitter-base voltage	open collector		-	6	V
VI	input voltage	positive		-	40	V
		negative		-	-6	V
Io	output current			-	100	mA
P _{tot}	total power dissipation	T _{amb} ≤ 25 °C	[1]	-	200	mW
Tj	junction temperature			-	150	°C
T _{amb}	ambient temperature			-65	150	°C
T _{stg}	storage temperature			-65	150	°C

 $^{[1] \}quad \text{Device mounted on an FR4 Printed-Circuit Board (PCB), single-sided, 35 } \mu\text{m copper, tin-plated and standard footprint.}$

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50 V, 100 mA NPN resistor-equipped transistor; R1 = 10 k Ω , R2 = 47 k Ω



FR4 PCB, single-sided, 35 µm copper, tin-plated and standard footprint

Fig. 1. Power derating curve

9. Thermal characteristics

Table 6. Thermal characteristics

Symbol	Parameter	Conditions		Min	Тур	Max	Unit
R _{th(j-a)}	thermal resistance from junction to ambient	in free air	[1]	-	-	625	K/W

[1] Device mounted on an FR4 PCB, single-sided, 35 μm copper, tin-plated and standard footprint.

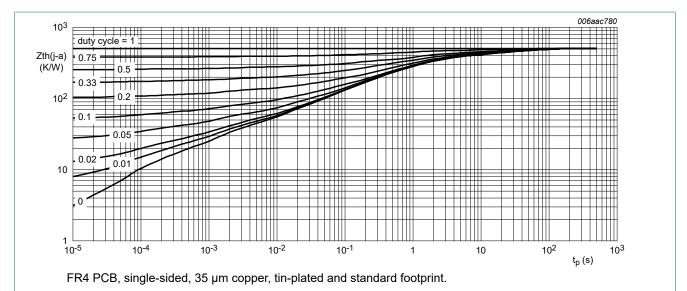


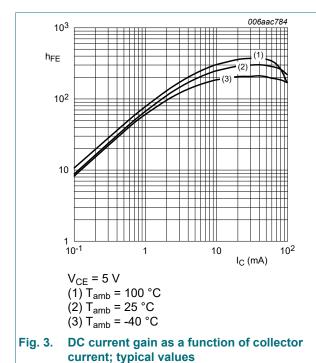
Fig. 2. Transient thermal impedance from junction to ambient as a function of pulse duration; typical values

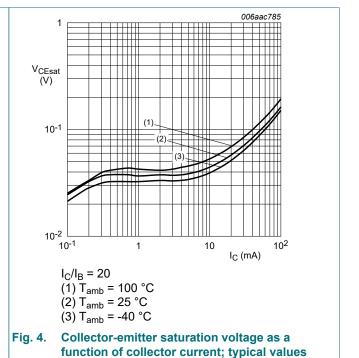
10. Characteristics

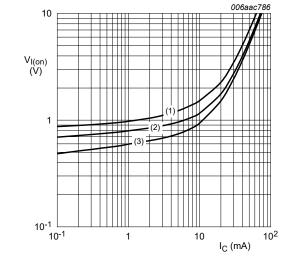
Table 7. Characteristics

Symbol	Parameter	Conditions		Min	Тур	Max	Unit
$V_{(BR)CBO}$	collector-base breakdown voltage	$I_C = 100 \ \mu A; I_E = 0 \ A; T_{amb} = 25 \ ^{\circ}C$		50	-	-	V
V _{(BR)CEO}	collector-emitter breakdown voltage	$I_C = 2 \text{ mA}; I_B = 0 \text{ A}; T_{amb} = 25 \text{ °C}$		50	-	-	V
I _{CBO}	collector-base cut-off current	_{CB} = 50 V; I _E = 0 A; T _{amb} = 25 °C		-	-	100	nA
I _{CEO}	collector-emitter cut-off	V _{CE} = 30 V; I _B = 0 A; T _{amb} = 25 °C		-	-	100	nA
	current	V _{CE} = 30 V; I _B = 0 A; T _j = 150 °C		-	-	5	μΑ
I _{EBO}	emitter-base cut-off current	$V_{EB} = 5 \text{ V}; I_{C} = 0 \text{ A}; T_{amb} = 25 \text{ °C}$		-	-	150	μA
h _{FE}	DC current gain	V _{CE} = 5 V; I _C = 5 mA; T _{amb} = 25 °C		100	-	-	
V _{CEsat}	collector-emitter saturation voltage	$I_C = 5 \text{ mA}; I_B = 0.25 \text{ mA}; T_{amb} = 25 ^{\circ}\text{C}$		-	-	100	mV
V _{I(off)}	off-state input voltage	V _{CE} = 5 V; I _C = 100 μA; T _{amb} = 25 °C		-	0.7	0.5	V
V _{I(on)}	on-state input voltage	$V_{CE} = 0.3 \text{ V}; I_{C} = 1 \text{ mA}; T_{amb} = 25 ^{\circ}\text{C}$		1.4	8.0	-	V
R1	bias resistor 1 (input)		[1]	7	10	13	kΩ
R2/R1	bias resistor ratio		[1]	3.7	4.7	5.7	
C _c	collector capacitance	$V_{CB} = 10 \text{ V}; I_E = 0 \text{ A}; i_e = 0 \text{ A}; f = 1 \text{ MHz}; $ $T_{amb} = 25 \text{ °C}$		-	-	2.5	pF
f _T	transition frequency	V_{CE} = 5 V; I_{C} = 10 mA; f = 100 MHz; T_{amb} = 25 °C	[2]	-	230	-	MHz

- [1] See "Section 11: Test information" for resistor calculation and test conditions.
- [2] Characteristics of built-in transistor.



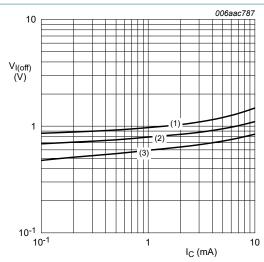




 $V_{CE} = 0.3 V$

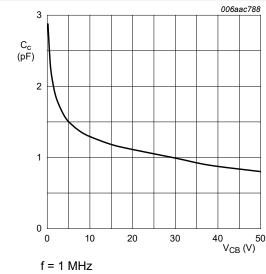
(1) T_{amb} = -40 °C (2) T_{amb} = 25 °C (3) T_{amb} = 100 °C

Fig. 5. On-state input voltage as a function of collector | Fig. 6. current; typical values



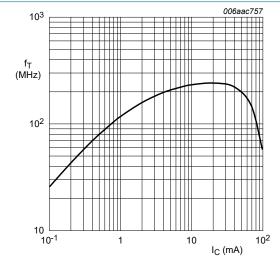
V_{CE} = 5 V (1) T_{amb} = -40 °C (2) T_{amb} = 25 °C (3) T_{amb} = 100 °C

Off-state input voltage as a function of collector current; typical values



 T_{amb} = 25 °C

Fig. 7. Collector capacitance as a function of collectorbase voltage; typical values



 V_{CE} = 5 V; T_{amb} = 25 °C

Fig. 8. Transition frequency as a function of collector current; typical values of built-in transistor

11. Test information

Quality information

This product has been qualified in accordance with the Automotive Electronics Council (AEC) standard Q101 - Stress test qualification for discrete semiconductors, and is suitable for use in automotive applications.

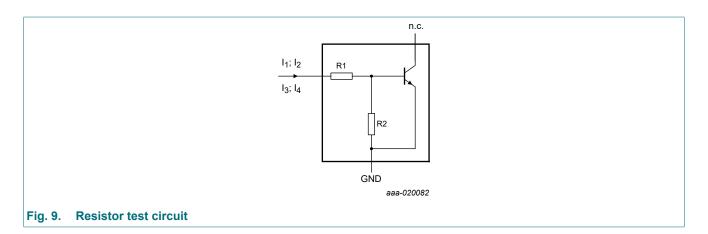
Resistor calculation

· Calculation of bias resistor 1 (R1)

$$R1 = \frac{V(I12) - V(I11)}{I12 - I11}$$

· Calculation of bias resistor ratio (R2/R1)

$$\frac{R2}{R1} = \frac{V(I4) - V(I3)}{R1 \cdot (I4 - I3)} - 1$$



Resistor test conditions

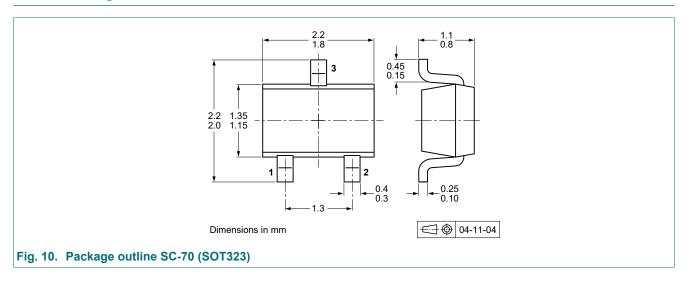
Table 8. Resistor test conditions

Type number	R1 (kΩ)	R2 (kΩ)	Test conditions			
			I _{I1}	I ₁₂	I ₁₃	I ₁₄
PDTC114YU-Q	10	47	90 μΑ	140 µA	-55 µA	-105 µA

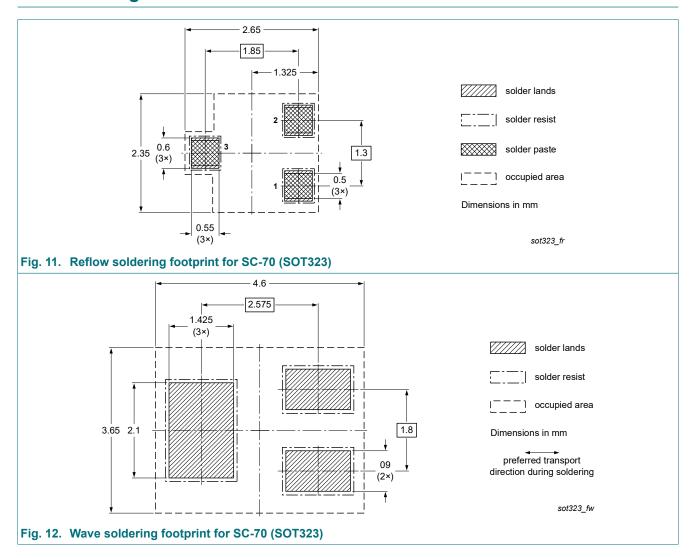
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50 V, 100 mA NPN resistor-equipped transistor; R1 = 10 k Ω , R2 = 47 k Ω

12. Package outline



13. Soldering



14. Revision history

Table 9. Revision history

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Data sheet ID	Release date		Change notice	Supersedes		
PDTC114YU-Q v.2	20230425	Product data sheet	-	PDTC114YU-Q v.1		
Modifications:	 Characteristic 	Characteristics: Value corrected for I _{CEO} at 25°C.				
PDTC114YU-Q v.1	20220308	Product data sheet	-	-		

15. Legal information

Data sheet status

Document status [1][2]	Product status [3]	Definition
Objective [short] data sheet	Development	This document contains data from the objective specification for product development.
Preliminary [short] data sheet	Qualification	This document contains data from the preliminary specification.
Product [short] data sheet	Production	This document contains the product specification.

- Please consult the most recently issued document before initiating or completing a design.
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