
# PIMC31

## 500 mA, 50 V NPN/PNP double resistor-equipped transistor; R1 = 1 kΩ, R2 = 10 kΩ

8 October 2024 **Product data sheet**

## 1. General description

500 mA, 50 V NPN/PNP double Resistor-Equipped Transistor (RET) in a small SOT457 (SC-74) Surface-Mounted Device (SMD) plastic package.

NPN/NPN complement: PIMN31

## 2. Features and benefits

- 500 mA output current capability
- Built-in bias resistors
- Simplifies circuit design
- Reduces component count
- Reduces pick and place costs

## 3. Applications

- Digital application in automotive and industrial segments
- Switching loads

## 4. Quick reference data

**Table 1. Quick reference data**

| Symbol | Parameter | Conditions | | Min | Typ | Max | Unit |
|---|---|---|---|---|---|---|---|
| **Per transistor** | | | | | | | |
| $V_{CEO}$ | collector-emitter voltage | open base | [1] | - | - | 50 | V |
| $I_O$ | output current | | [1] | - | - | 500 | mA |
| R1 | bias resistor 1 (input) | | [2] | 0.7 | 1 | 1.3 | kΩ |
| R2/R1 | bias resistor ratio | | [2] | 9 | 10 | 11 | |

[1] For the PNP transistor with negative polarity.
[2] See section "Test information" for resistor calculation and test conditions.

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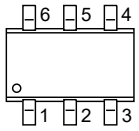
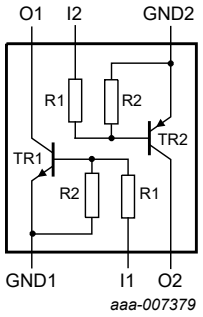
# 5. Pinning information

**Table 2. Pinning information**

| Pin | Symbol | Description | Simplified outline | Graphic symbol |
|---|---|---|---|---|
| 1 | GND1 | GND (emitter) TR1 |  TSOP6 (SOT457) |  |
| 2 | I1 | input (base) TR1 | | |
| 3 | O2 | output (collector) TR2 | | |
| 4 | GND2 | GND (emitter) TR2 | | |
| 5 | I2 | input (base) TR2 | | |
| 6 | O1 | output (collector) TR1 | | |



# 6. Ordering information

**Table 3. Ordering information**

| Type number | Package | | |
|---|---|---|---|
| | Name | Description | Version |
| PIMC31 | TSOP6 | plastic, surface-mounted package (SC-74; TSOP6); 6 leads | SOT457 |
| PIMC31/A001 | TSOP6 | plastic, surface-mounted package (SC-74; TSOP6); 6 leads | SOT457 |

# 7. Marking

**Table 4. Marking codes**

| Type number | Marking code |
|---|---|
| PIMC31 | ZH |
| PIMC31/A001 | ZH |

# 8. Limiting values

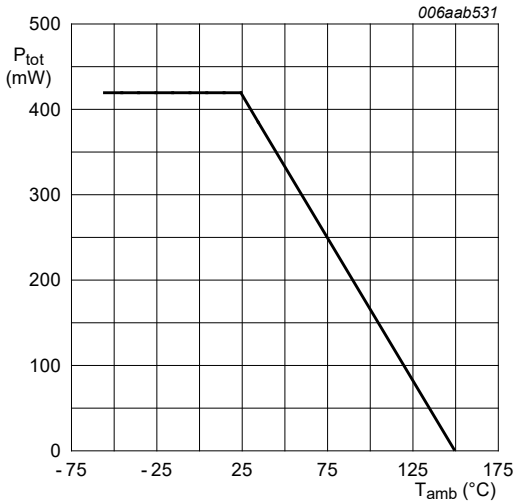
**Table 5. Limiting values**

*In accordance with the Absolute Maximum Rating System (IEC 60134).*

| Symbol | Parameter | Conditions | | Min | Max | Unit |
|---|---|---|---|---|---|---|
| **Per transistor** | | | | | | |
| $V_{CBO}$ | collector-base voltage | open emitter | [1] | - | 50 | V |
| $V_{CEO}$ | collector-emitter voltage | open base | [1] | - | 50 | V |
| $V_{EBO}$ | emitter-base voltage | open collector | [1] | - | 5 | V |
| $V_I$ | input voltage | TR1 (NPN) | | -5 | 10 | V |
| | | TR2 (PNP) | | -10 | 5 | V |
| $I_O$ | output current | | [1] | - | 500 | mA |
| $P_{tot}$ | total power dissipation | $T_{amb} \leq 25$ °C | [2] | - | 290 | mW |
| **Per device** | | | | | | |
| $P_{tot}$ | total power dissipation | $T_{amb} \leq 25$ °C | [2] | - | 420 | mW |

| Symbol | Parameter | Conditions | | Min | Max | Unit |
|---|---|---|---|---|---|---|
| $T_j$ | junction temperature | | | - | 150 | °C |
| $T_{amb}$ | ambient temperature | | | -55 | 150 | °C |
| $T_{stg}$ | storage temperature | | | -65 | 150 | °C |

[1] For the PNP transistor with negative polarity.
[2] Device mounted on an FR4 Printed-Circuit Board (PCB), single-sided, 35 µm copper, tin-plated and standard footprint.




FR4 PCB, single-sided, 35 µm copper, tin-plated and standard footprint

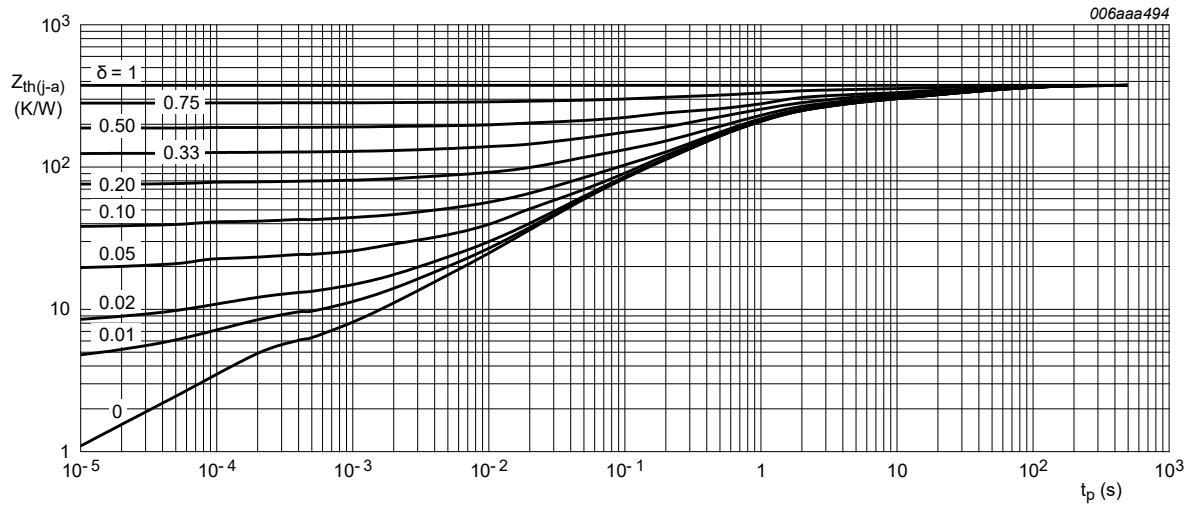
**Fig. 1. Per device: Power derating curve**

## 9. Thermal characteristics

**Table 6. Thermal characteristics**

| Symbol | Parameter | Conditions | | Min | Typ | Max | Unit |
|---|---|---|---|---|---|---|---|
| **Per transistor** | | | | | | | |
| $R_{th(j-a)}$ | thermal resistance from junction to ambient | in free air | [1] | - | - | 431 | K/W |
| $R_{th(j-sp)}$ | thermal resistance from junction to solder point | | | - | - | 105 | K/W |
| **Per device** | | | | | | | |
| $R_{th(j-a)}$ | thermal resistance from junction to ambient | in free air | [1] | - | - | 298 | K/W |

[1] Device mounted on an FR4 PCB, single-sided, 35 µm copper, tin-plated and standard footprint.




FR4 PCB, single-sided, 35µm copper, tin-plated and standard footprint

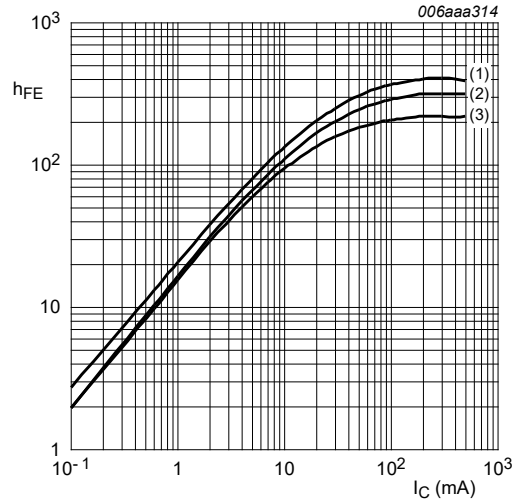
**Fig. 2. Per transistor: Transient thermal impedance from junction to ambient as a function of pulse duration; typical values**

## 10. Characteristics

**Table 7. Characteristics**

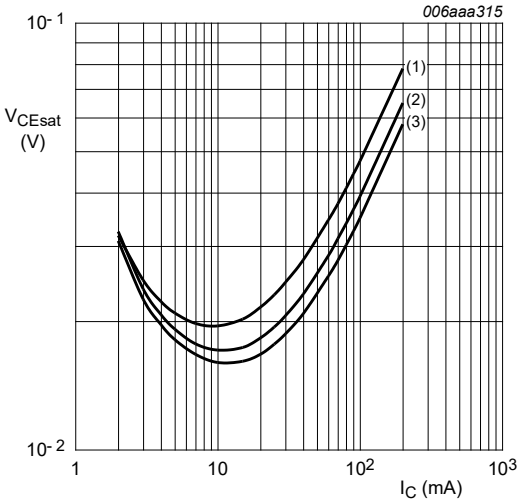
| Symbol | Parameter | Conditions | | Min | Typ | Max | Unit |
|---|---|---|---|---|---|---|---|
| **Per transistor** | | | | | | | |
| $V_{(BR)CBO}$ | collector-base breakdown voltage | $I_C$ = 100 µA; $I_E$ = 0 A; $T_{amb}$ = 25 °C | [1] | 50 | - | - | V |
| $V_{(BR)CEO}$ | collector-emitter breakdown voltage | $I_C$ = 2 mA; $I_B$ = 0 A; $T_{amb}$ = 25 °C | [1] | 50 | - | - | V |
| $I_{CBO}$ | collector-base cut-off current | $V_{CB}$ = 50 V; $I_E$ = 0 A; $T_{amb}$ = 25 °C | [1] | - | - | 100 | nA |
| $I_{CEO}$ | collector-emitter cut-off current | $V_{CE}$ = 50 V; $I_B$ = 0 A; $T_{amb}$ = 25 °C | [1] | - | - | 0.5 | µA |
| $I_{EBO}$ | emitter-base cut-off current | $V_{EB}$ = 5 V; $I_C$ = 0 A; $T_{amb}$ = 25 °C | [1] | - | - | 0.72 | mA |
| $h_{FE}$ | DC current gain | $V_{CE}$ = 5 V; $I_C$ = 50 mA; $T_{amb}$ = 25 °C | [1] | 70 | - | - | |
| $V_{CEsat}$ | collector-emitter saturation voltage | $I_C$ = 50 mA; $I_B$ = 2.5 mA; $T_{amb}$ = 25 °C | [1] | - | - | 300 | mV |
| $V_{I(off)}$ | off-state input voltage | $V_{CE}$ = 5 V; $I_C$ = 100 µA | [1] | 0.3 | 0.6 | 1 | V |
| $V_{I(on)}$ | on-state input voltage | $V_{CE}$ = 0.3 V; $I_C$ = 20 mA; $T_{amb}$ = 25 °C | [1] | 0.4 | 0.8 | 1.4 | V |
| R1 | bias resistor 1 (input) | | [2] | 0.7 | 1 | 1.3 | kΩ |
| R2/R1 | bias resistor ratio | | [2] | 9 | 10 | 11 | |
| **TR1 (NPN)** | | | | | | | |
| $C_c$ | collector capacitance | $V_{CB}$ = 10 V; $I_E$ = 0 A; $i_e$ = 0 A; f = 1 MHz; $T_{amb}$ = 25 °C | | - | 7 | - | pF |
| **TR2 (PNP)** | | | | | | | |
| $C_c$ | collector capacitance | $V_{CB}$ = -10 V; $I_E$ = 0 A; $i_e$ = 0 A; f = 1 MHz; $T_{amb}$ = 25 °C | | - | 11 | - | pF |

[1] For the PNP transistor with negative polarity.
[2] See section "Test information" for resistor calculation and test conditions.



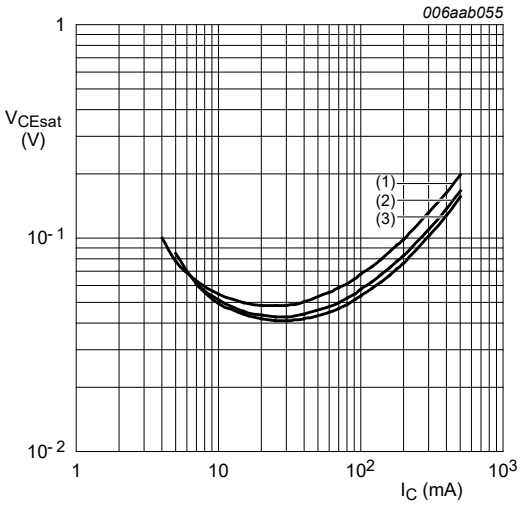

$V_{CE}$ = 5 V
(1) $T_{amb}$ = 100 °C
(2) $T_{amb}$ = 25 °C
(3) $T_{amb}$ = −40 °C

**Fig. 3. TR1 (NPN): DC current gain as a function of collector current; typical values**



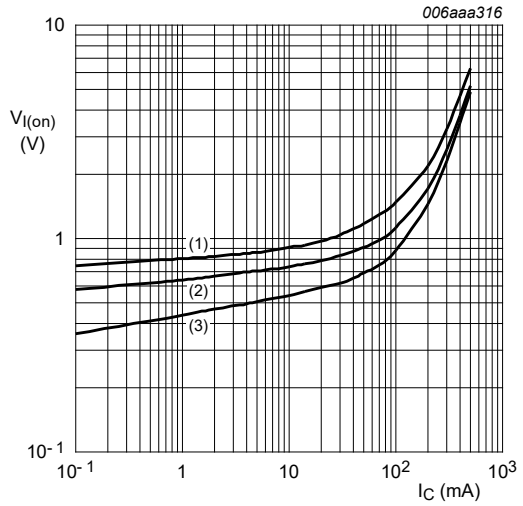

$I_C/I_B$ = 20
(1) $T_{amb}$ = 100 °C
(2) $T_{amb}$ = 25 °C
(3) $T_{amb}$ = −40 °C

**Fig. 4. TR1 (NPN): Collector-emitter saturation voltage as a function of collector current; typical values**



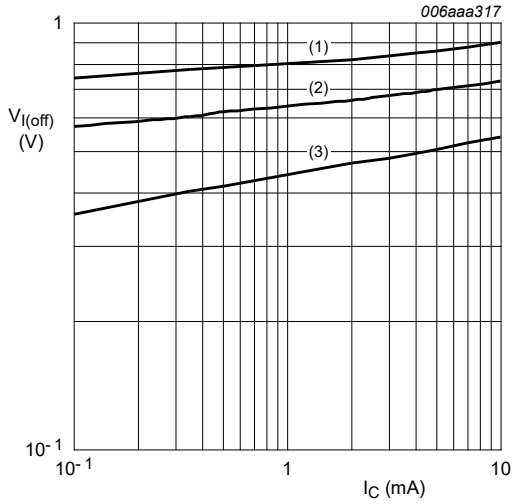

$I_C/I_B$ = 50
(1) $T_{amb}$ = 100 °C
(2) $T_{amb}$ = 25 °C
(3) $T_{amb}$ = −40 °C

**Fig. 5. TR1 (NPN): Collector-emitter saturation voltage as a function of collector current; typical values**



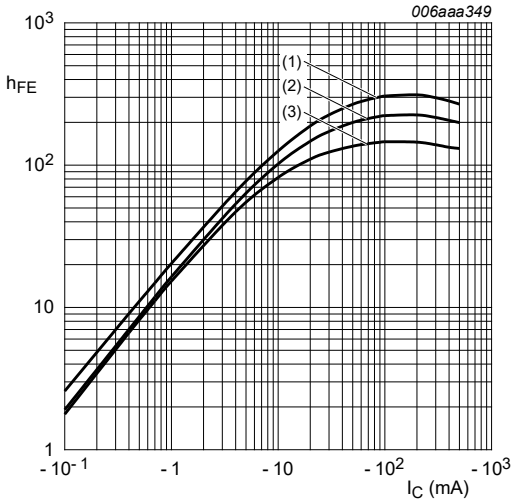

$V_{CE}$ = 0.3 V
(1) $T_{amb}$ = -40 °C
(2) $T_{amb}$ = 25 °C
(3) $T_{amb}$ = 100 °C

**Fig. 6. TR1 (NPN): On-state input voltage as a function of collector current; typical values**



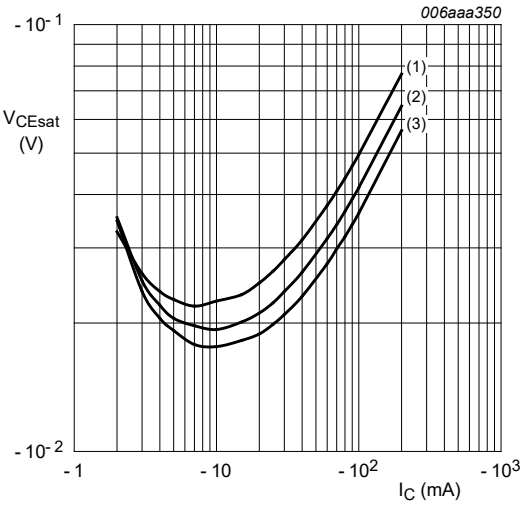

$V_{CE}$ = 5 V
(1) $T_{amb}$ = -40 °C
(2) $T_{amb}$ = 25 °C
(3) $T_{amb}$ = 100 °C

**Fig. 7. TR1 (NPN): Off-state input voltage as a function of collector current; typical values**



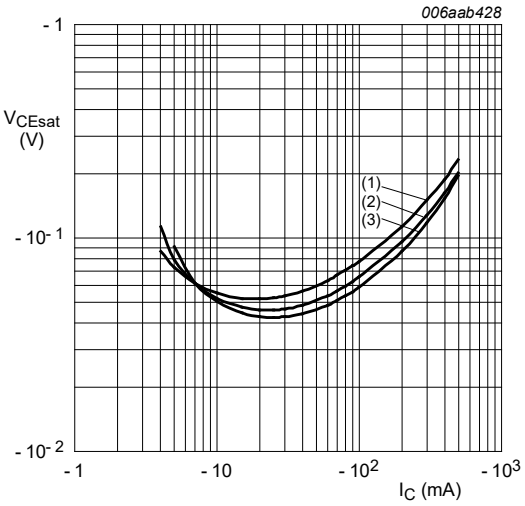

$V_{CE}$ = -5 V
(1) $T_{amb}$ = 100 °C
(2) $T_{amb}$ = 25 °C
(3) $T_{amb}$ = −40 °C

**Fig. 8. TR2 (PNP): DC current gain as a function of collector current; typical values**



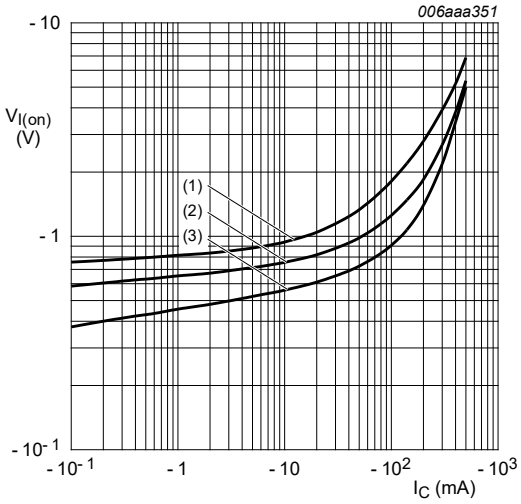

$I_C/I_B$ = 20
(1) $T_{amb}$ = 100 °C
(2) $T_{amb}$ = 25 °C
(3) $T_{amb}$ = −40 °C

**Fig. 9. TR2 (PNP): Collector-emitter saturation voltage as a function of collector current; typical values**



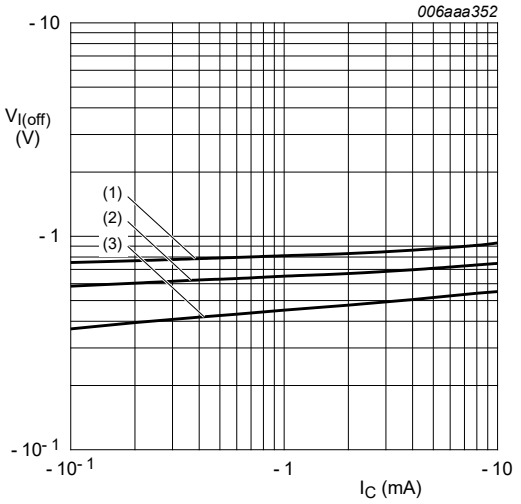

$I_C/I_B$ = 50
(1) $T_{amb}$ = 100 °C
(2) $T_{amb}$ = 25 °C
(3) $T_{amb}$ = −40 °C

**Fig. 10. TR2 (PNP): Collector-emitter saturation voltage as a function of collector current; typical values**




$V_{CE}$ = -0.3 V
(1) $T_{amb}$ = -40 °C
(2) $T_{amb}$ = 25 °C
(3) $T_{amb}$ = 100 °C

**Fig. 11. TR2 (PNP): On-state input voltage as a function of collector current; typical values**




$V_{CE}$ = -5 V
(1) $T_{amb}$ = -40 °C
(2) $T_{amb}$ = 25 °C
(3) $T_{amb}$ = 100 °C

**Fig. 12. TR2 (PNP): Off-state input voltage as a function of collector current; typical values**

## 11. Package outline

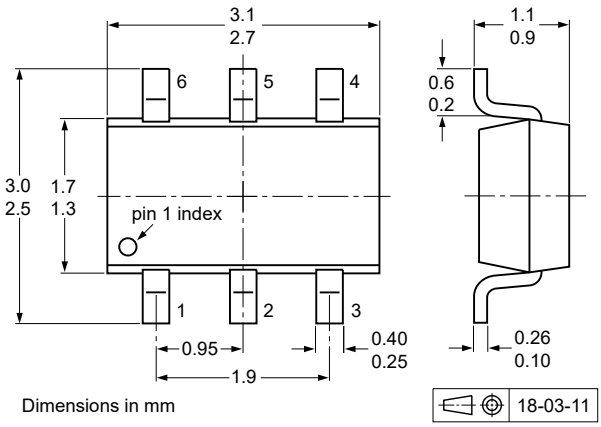



**Fig. 13. Package outline TSOP6 (SOT457)**

## 12. Soldering

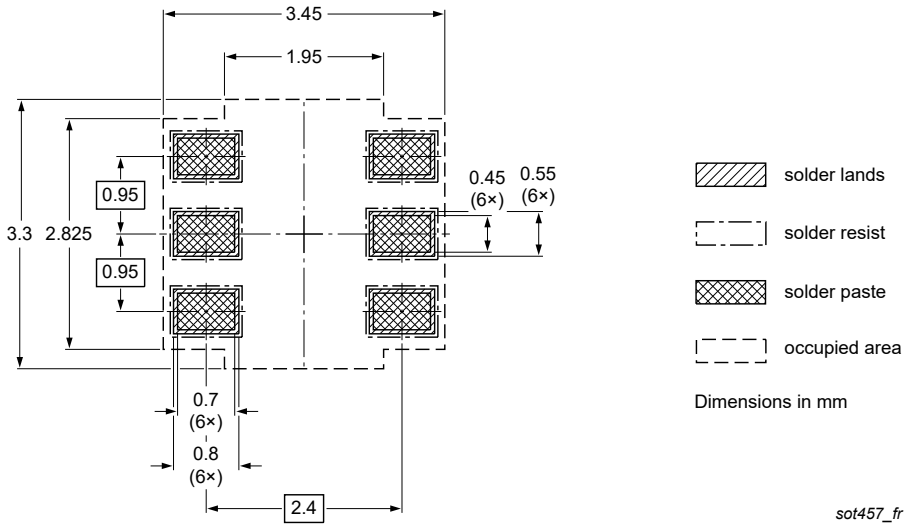



**Fig. 14. Reflow soldering footprint for TSOP6 (SOT457)**

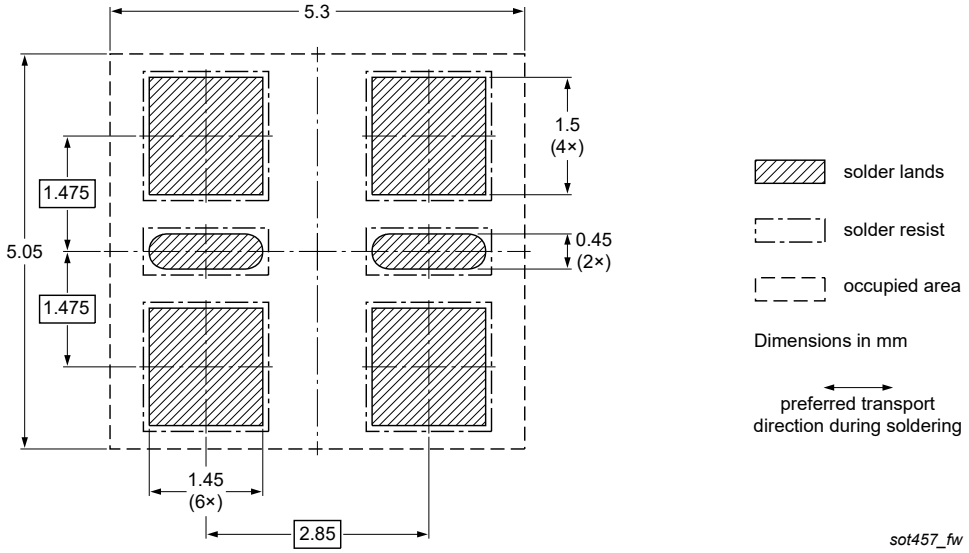



**Fig. 15. Wave soldering footprint for TSOP6 (SOT457)**

# 13. Revision history

**Table 8. Revision history**

| Data sheet ID | Release date | Data sheet status | Change notice | Supersedes |
|---|---|---|---|---|
| PIMC31 v.2 | 20241008 | Product data sheet | - | PIMC31 v.1 |
| Modifications: | • Product(s) changed to non-automotive qualification. Please refer to nexperia.com for automotive (-Q) product alternative(s).<br>• The format of this data sheet has been redesigned to comply with the identity guidelines of Nexperia.<br>• Legal texts have been adapted to the new company name where appropriate.<br>• Section "Packing information" removed. | | | |
| PIMC31 v.1 | 20090324 | Product data sheet | - | - |

# 14. Legal information

## Data sheet status

| Document status [1][2] | Product status [3] | Definition |
|---|---|---|
| Objective [short] data sheet | Development | This document contains data from the objective specification for product development. |
| Preliminary [short] data sheet | Qualification | This document contains data from the preliminary specification. |
| Product [short] data sheet | Production | This document contains the product specification. |

[1] Please consult the most recently issued document before initiating or completing a design.
[2] The term 'short data sheet' is explained in section "Definitions".
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