# Plastic Medium-Power Complementary Silicon Transistors

# BDX53B, BDX53C (NPN), BDX54B, BDX54C (PNP)

These devices are designed for general−purpose amplifier and low−speed switching applications.

### Features

- High DC Current Gain −
  $h_{FE}$ = 2500 (Typ) @ $I_C$ = 4.0 Adc
- Collector Emitter Sustaining Voltage − @ 100 mAdc
  $V_{CEO(sus)}$ = 80 Vdc (Min) − BDX53B, 54B
  = 100 Vdc (Min) − BDX53C, 54C
- Low Collector−Emitter Saturation Voltage −
  $V_{CE(sat)}$ = 2.0 Vdc (Max) @ $I_C$ = 3.0 Adc
  = 4.0 Vdc (Max) @ $I_C$ = 5.0 Adc
- Monolithic Construction with Built−In Base−Emitter Shunt Resistors
- These Devices are Pb−Free and are RoHS Compliant*

### MAXIMUM RATINGS

| Rating | Symbol | Value | Unit |
|---|---|---|---|
| Collector−Emitter Voltage<br>BDX53B, BDX54B<br>BDX53C, BDX54C | $V_{CEO}$ | <br>80<br>100 | Vdc |
| Collector−Base Voltage<br>BDX53B, BDX54B<br>BDX53C, BDX54C | $V_{CB}$ | <br>80<br>100 | Vdc |
| Emitter−Base Voltage | $V_{EB}$ | 5.0 | Vdc |
| Collector Current − Continuous<br>− Peak | $I_C$ | 8.0<br>12 | Adc |
| Base Current | $I_B$ | 0.2 | Adc |
| Total Device Dissipation @ $T_C$ = 25°C<br>Derate above 25°C | $P_D$ | 65<br>0.48 | W<br>W/°C |
| Operating and Storage Junction Temperature Range | $T_J$, $T_{stg}$ | −65 to +150 | °C |

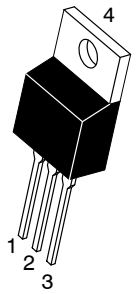
Stresses exceeding those listed in the Maximum Ratings table may damage the device. If any of these limits are exceeded, device functionality should not be assumed, damage may occur and reliability may be affected.

### THERMAL CHARACTERISTICS

| Characteristic | Symbol | Max | Unit |
|---|---|---|---|
| Thermal Resistance, Junction−to−Ambient | $R_{\theta JA}$ | 70 | °C/W |
| Thermal Resistance, Junction−to−Case | $R_{\theta JC}$ | 1.92 | °C/W |

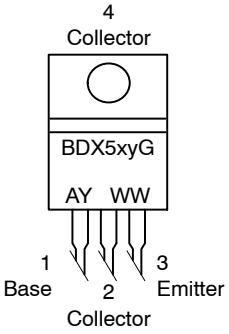
*For additional information on our Pb−Free strategy and soldering details, please download the **onsemi** Soldering and Mounting Techniques Reference Manual, SOLDERRM/D.

## DARLINGTON 8 AMPERE COMPLEMENTARY SILICON POWER TRANSISTORS 80−100 VOLTS, 65 WATTS




**TO−220**
**CASE 221A**
**STYLE 1**

### MARKING DIAGRAM & PIN ASSIGNMENT




BDX5xy = Device Code
x = 3 or 4
y = B or C
A = Assembly Location
Y = Year
WW = Work Week
G = Pb−Free Package

### ORDERING INFORMATION

See detailed ordering and shipping information in the package dimensions section on page 6 of this data sheet.

NOTE: Some of the devices on this data sheet have been **DISCONTINUED**. Please refer to the table on page 6.

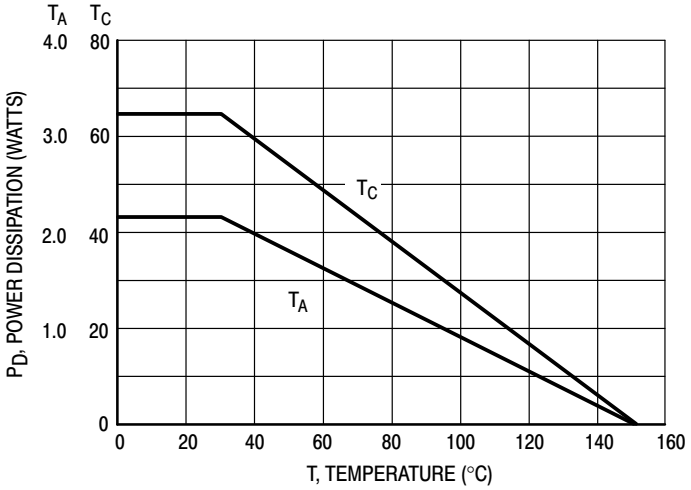



**Figure 1. Power Derating**

**ELECTRICAL CHARACTERISTICS** ($T_C$ = 25°C unless otherwise noted)

| Characteristic | | Symbol | Min | Max | Unit |
|---|---|---|---|---|---|
| **OFF CHARACTERISTICS** | | | | | |
| Collector−Emitter Sustaining Voltage (Note 1)<br>($I_C$ = 100 mAdc, $I_B$ = 0) | BDX53B, BDX54B<br>BDX53C, BDX54C | $V_{CEO(sus)}$ | <br>80<br>100 | <br>–<br>– | Vdc |
| Collector Cutoff Current<br>($V_{CE}$ = 40 Vdc, $I_B$ = 0)<br>($V_{CE}$ = 50 Vdc, $I_B$ = 0) | <br>BDX53B, BDX54B<br>BDX53C, BDX54C | $I_{CEO}$ | <br>–<br>– | <br>0.5<br>0.5 | mAdc |
| Collector Cutoff Current<br>($V_{CB}$ = 80 Vdc, $I_E$ = 0)<br>($V_{CB}$ = 100 Vdc, $I_E$ = 0) | <br>BDX53B, BDX54B<br>BDX53C, BDX54C | $I_{CBO}$ | <br>–<br>– | <br>0.2<br>0.2 | mAdc |
| **ON CHARACTERISTICS** (Note 1) | | | | | |
| DC Current Gain<br>($I_C$ = 3.0 Adc, $V_{CE}$ = 3.0 Vdc) | | $h_{FE}$ | 750 | – | – |
| Collector−Emitter Saturation Voltage<br>($I_C$ = 3.0 Adc, $I_B$ = 12 mAdc) | | $V_{CE(sat)}$ | –<br>– | 2.0<br>4.0 | Vdc |
| Base−Emitter Saturation Voltage<br>($I_C$ = 3.0 Adc, $I_C$ = 12 mA) | | $V_{BE(sat)}$ | – | 2.5 | Vdc |
| **DYNAMIC CHARACTERISTICS** | | | | | |
| Small−Signal Current Gain<br>($I_C$ = 3.0 Adc, $V_{CE}$ = 4.0 Vdc, f = 1.0 MHz) | | $h_{fe}$ | 4.0 | – | – |
| Output Capacitance<br>($V_{CB}$ = 10 Vdc, $I_E$ = 0, f = 0.1 MHz) | <br>BDX53B, 53C<br>BDX54B, 54C | $C_{ob}$ | <br>–<br>– | <br>300<br>200 | pF |

Product parametric performance is indicated in the Electrical Characteristics for the listed test conditions, unless otherwise noted. Product performance may not be indicated by the Electrical Characteristics if operated under different conditions.

1. Pulse Test: Pulse Width ≤ 300 μs, Duty Cycle ≤ 2%.

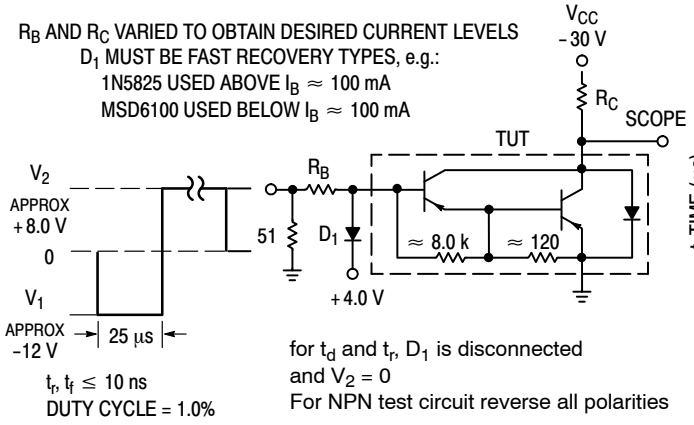



**Figure 2. Switching Time Test Circuit**

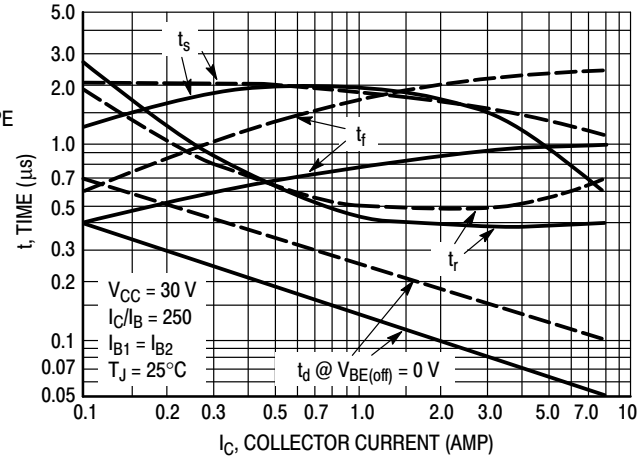



**Figure 3. Switching Times**

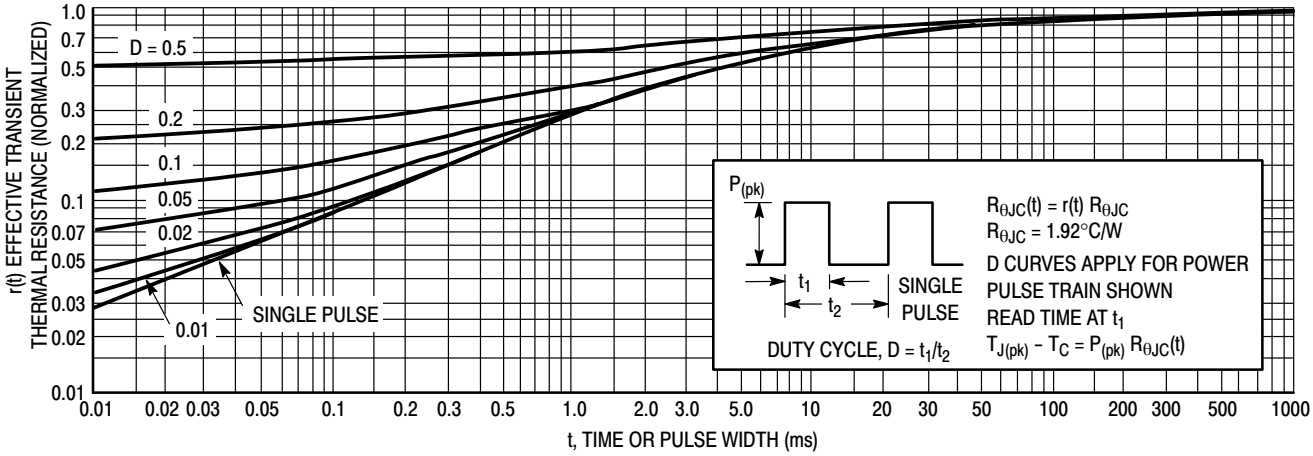



**Figure 4. Thermal Response**

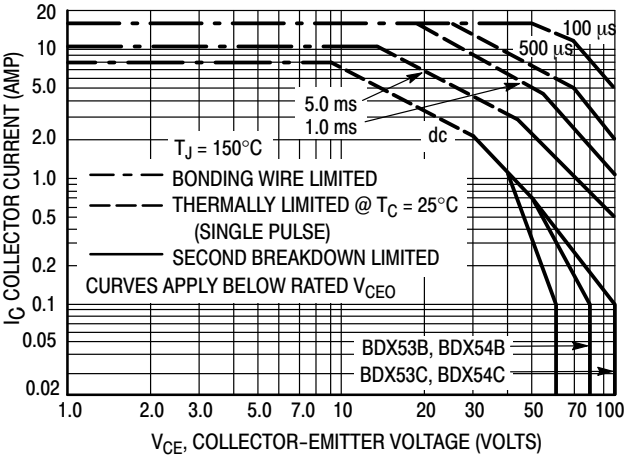



**Figure 5. Active−Region Safe Operating Area**

There are two limitations on the power handling ability of a transistor average junction temperature and second breakdown. Safe operating area curves indicate $I_C - V_{CE}$ limits of the transistor that must be observed for reliable operation, i.e., the transistor must not be subjected to greater dissipation than the curves indicate.

The data of Figure 5 is based on $T_{J(pk)}$ = 150°C; $T_C$ is variable depending on conditions. Second breakdown pulse limits are valid for duty cycles to 10% provided $T_{J(pk)} < 150°C$. $T_{J(pk)}$ may be calculated from the data in Figure 4. At high case temperatures, thermal limitations will reduce the power that can be handled to values less than the limitations imposed by second breakdown.

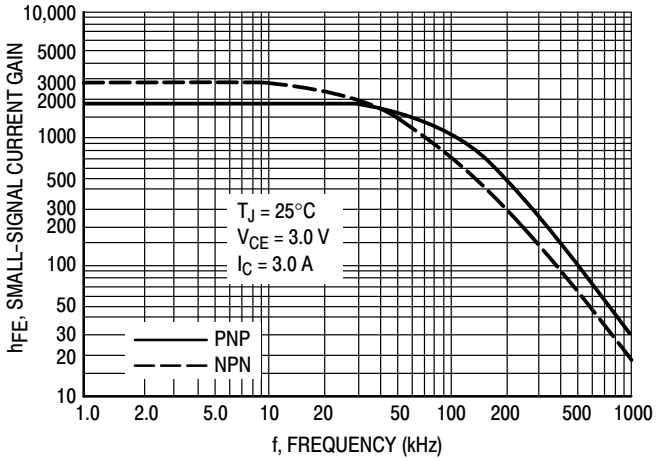



Figure 6. Small-Signal Current Gain

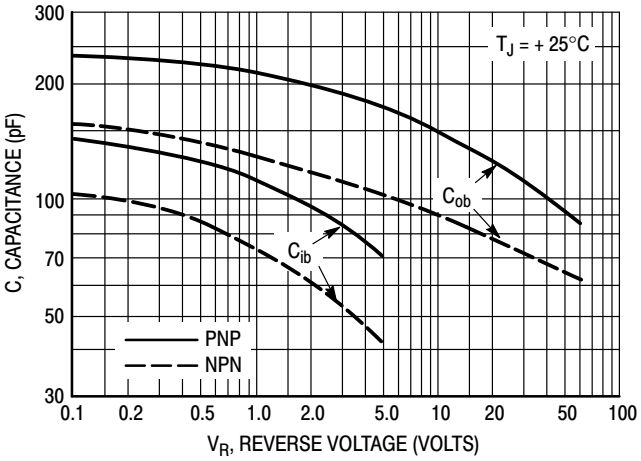
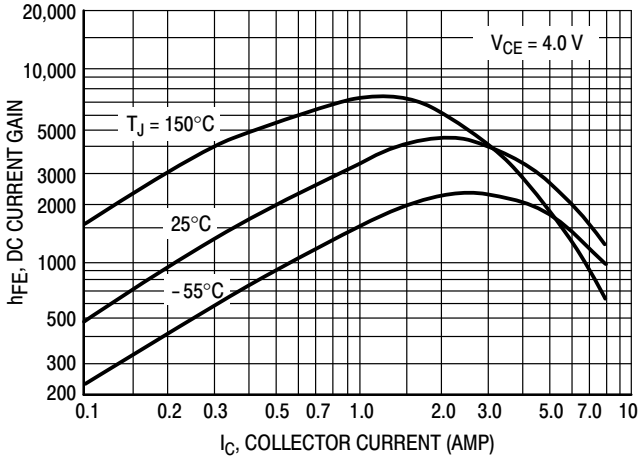



Figure 7. Capacitance

**NPN**
**BDX53B, 53C**




**PNP**
**BDX54B, 54C**

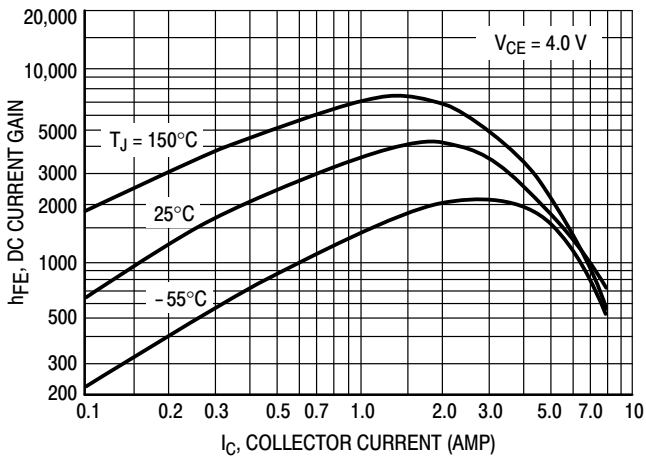
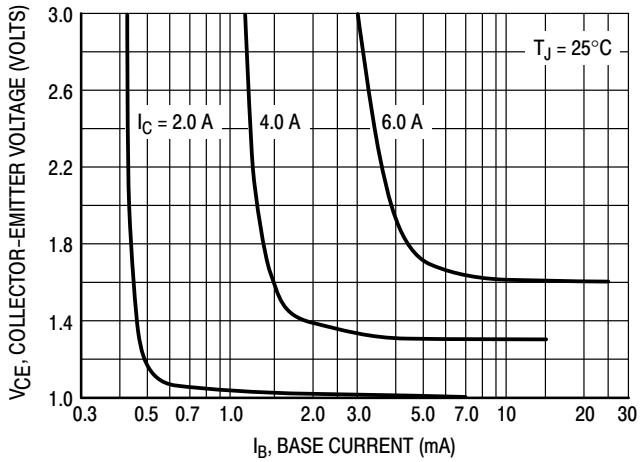



Figure 8. DC Current Gain



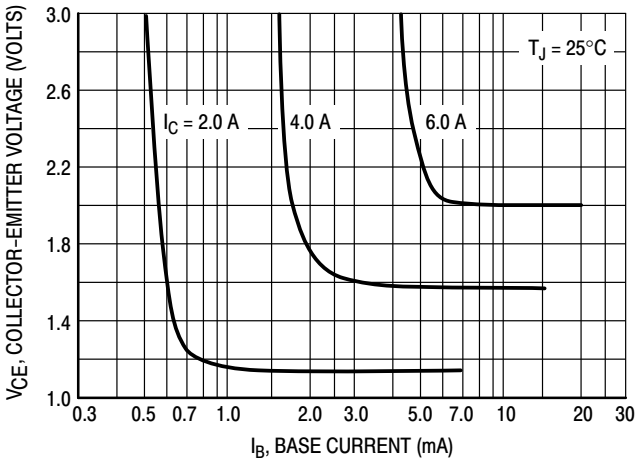




Figure 9. Collector Saturation Region

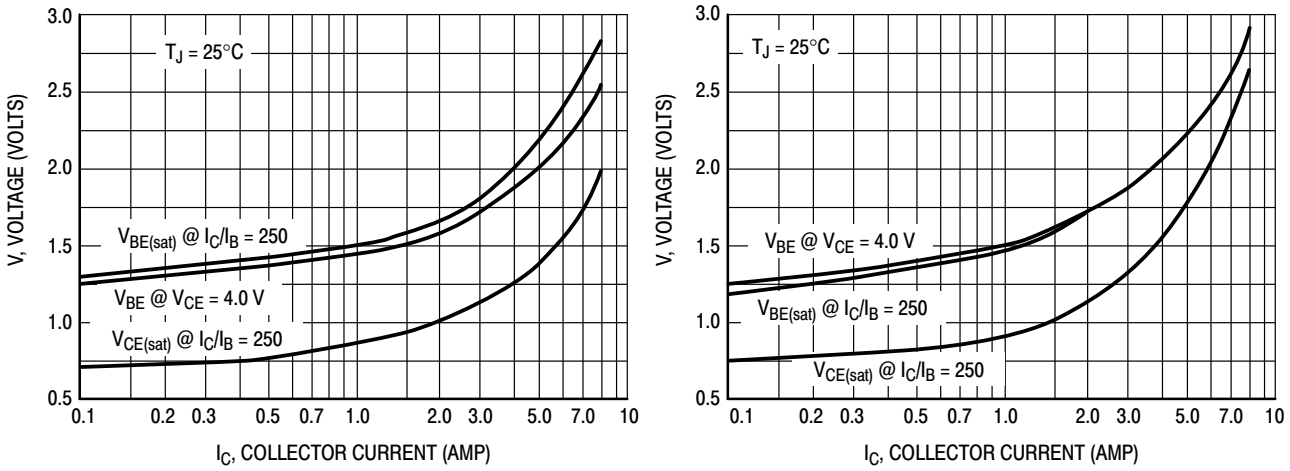



**Figure 10. “On” Voltages**

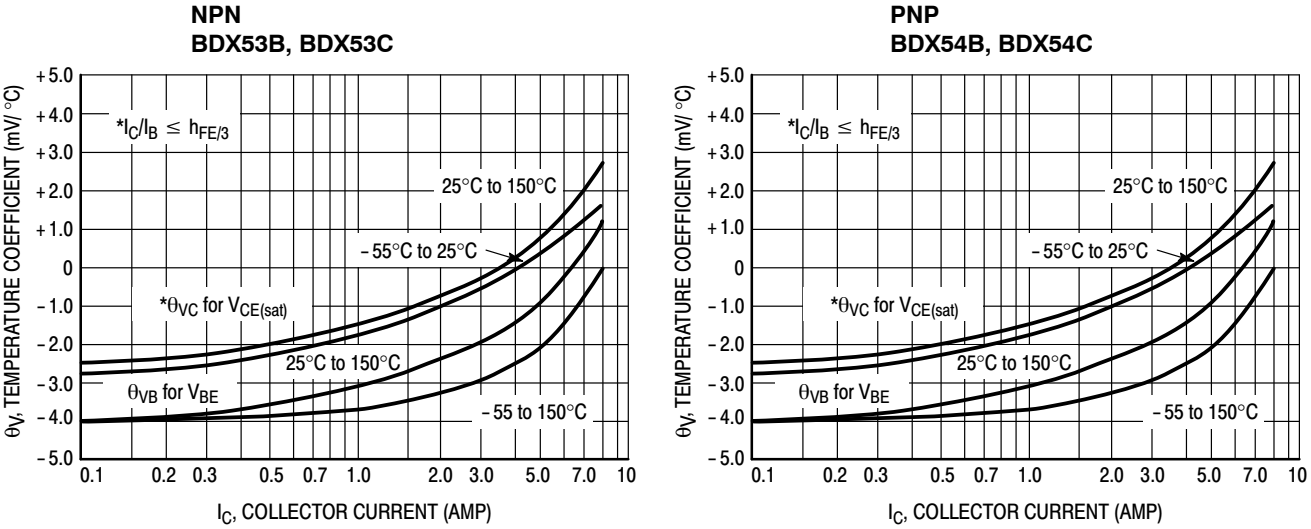



**Figure 11. Temperature Coefficients**

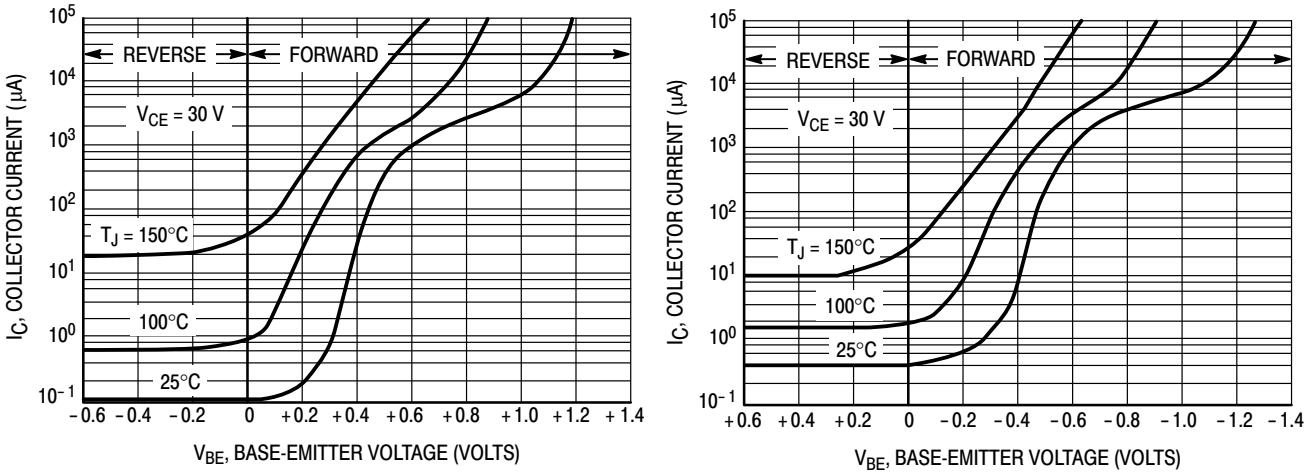



**Figure 12. Collector Cut−Off Region**


**Figure 13. Darlington Schematic**

## ORDERING INFORMATION

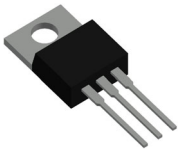
| Device | Package | Shipping† |
|---|---|---|
| BDX53BG | TO−220<br>(Pb−Free) | 50 Units / Rail |
| BDX53CG | TO−220<br>(Pb−Free) | 50 Units / Rail |

**DISCONTINUED** (Note 2)

| | | |
|---|---|---|
| BDX54BG | TO−220<br>(Pb−Free) | 50 Units / Rail |
| BDX54CG | TO−220<br>(Pb−Free) | 50 Units / Rail |

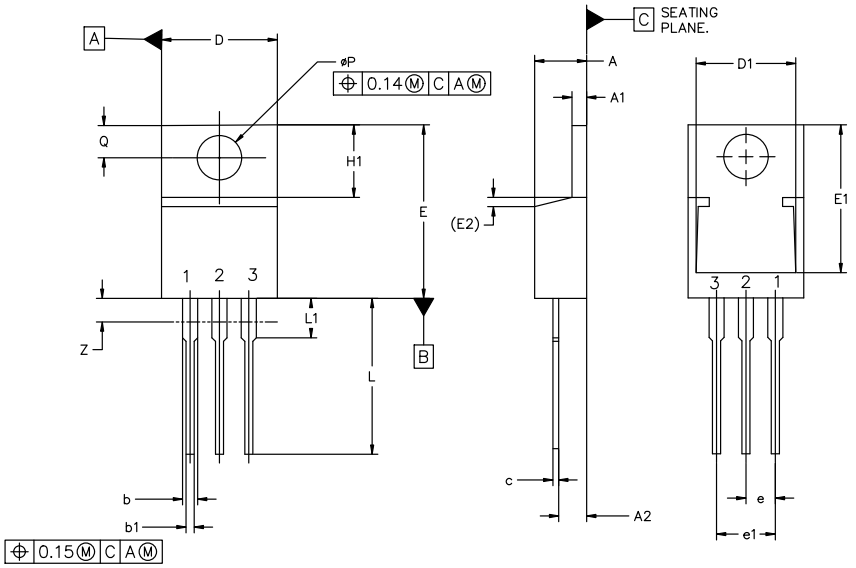
†For information on tape and reel specifications, including part orientation and tape sizes, please refer to our Tape and Reel Packaging Specifications Brochure, BRD8011/D.

2. **DISCONTINUED:** These devices are not recommended for new design. Please contact your **onsemi** representative for information. The most current information on these devices may be available on www.onsemi.com.



**TO−220−3 10.10x15.12x4.45, 2.54P**
CASE 221A
ISSUE AL

DATE 05 FEB 2025




| MILLIMETERS | | | |
|---|---|---|---|
| DIM | MIN | NOM | MAX |
| A | 4.07 | 4.45 | 4.83 |
| A1 | 1.15 | 1.28 | 1.41 |
| A2 | 2.04 | 2.42 | 2.79 |
| b | 1.15 | 1.34 | 1.52 |
| b1 | 0.64 | 0.80 | 0.96 |
| c | 0.36 | 0.49 | 0.61 |
| D | 9.66 | 10.10 | 10.53 |
| D1 | 8.43 | 8.63 | 8.83 |
| E | 14.48 | 15.12 | 15.75 |
| E1 | 12.58 | 12.78 | 12.98 |
| E2 | 1.27 REF | | |

| MILLIMETERS | | | |
|---|---|---|---|
| DIM | MIN | NOM | MAX |
| e | 2.42 | 2.54 | 2.66 |
| e1 | 4.83 | 5.08 | 5.33 |
| H1 | 5.97 | 6.22 | 6.47 |
| L | 12.70 | 13.49 | 14.27 |
| L1 | 2.80 | 3.45 | 4.10 |
| Q | 2.54 | 2.79 | 3.04 |
| øP | 3.60 | 3.85 | 4.09 |
| Z | −.−− | −.−− | 3.48 |

NOTES:
1. DIMENSIONING AND TOLERANCING PER ASME Y14.5M, 2018.
2. CONTROLLING DIMENSION: MILLIMETERS.
3. DIMENSION Z DEFINES A ZONE WHERE ALL BODY AND LEAD IRREGULARITIES ARE ALLOWED.

STYLE 1:
PIN 1. BASE
2. COLLECTOR
3. EMITTER
4. COLLECTOR

STYLE 2:
PIN 1. BASE
2. EMITTER
3. COLLECTOR
4. EMITTER

STYLE 3:
PIN 1. CATHODE
2. ANODE
3. GATE
4. ANODE

STYLE 4:
PIN 1. MAIN TERMINAL 1
2. MAIN TERMINAL 2
3. GATE
4. MAIN TERMINAL 2

STYLE 5:
PIN 1. GATE
2. DRAIN
3. SOURCE
4. DRAIN

STYLE 6:
PIN 1. ANODE
2. CATHODE
3. ANODE
4. CATHODE

STYLE 7:
PIN 1. CATHODE
2. ANODE
3. CATHODE
4. ANODE

STYLE 8:
PIN 1. CATHODE
2. ANODE
3. EXTERNAL TRIP/DELAY
4. ANODE

STYLE 9:
PIN 1. GATE
2. COLLECTOR
3. EMITTER
4. COLLECTOR

STYLE 10:
PIN 1. GATE
2. SOURCE
3. DRAIN
4. SOURCE

STYLE 11:
PIN 1. DRAIN
2. SOURCE
3. GATE
4. SOURCE

STYLE 12:
PIN 1. MAIN TERMINAL 1
2. MAIN TERMINAL 2
3. GATE
4. NOT CONNECTED

| | | |
|---|---|---|
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| **DESCRIPTION:** | **TO−220−3 10.10x15.12x4.45, 2.54P** | **PAGE 1 OF 1** |

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