

# NPN Silicon Transistor

## BF720T1G, SBF720T1G, BF720T3G

### Features

- AEC-Q101 Qualified and PPAP Capable
- S Prefix for Automotive and Other Applications Requiring Unique Site and Control Change Requirements
- These Devices are Pb-Free, Halogen Free/BFR Free and are RoHS Compliant\*

### MAXIMUM RATINGS

Rating	Symbol	Value	Unit
Collector – Emitter Voltage	$V_{CEO}$	300	Vdc
Collector – Base Voltage	$V_{CBO}$	300	Vdc
Collector – Emitter Voltage	$V_{CER}$	300	Vdc
Emitter – Base Voltage	$V_{EBO}$	5.0	Vdc
Collector Current	$I_C$	100	mAdc
Total Power Dissipation up to $T_A = 25^\circ\text{C}$	$P_D$	1.5	W
Storage Temperature Range	$T_{stg}$	-65 to +150	$^\circ\text{C}$
Junction Temperature	$T_J$	150	$^\circ\text{C}$

### THERMAL CHARACTERISTICS

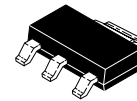
Characteristic	Symbol	Max	Unit
Thermal Resistance, Junction-to-Ambient (Note 2)	$R_{\theta JA}$	83.3	$^\circ\text{C/W}$

Stresses exceeding those listed in the Maximum Ratings table may damage the device. If any of these limits are exceeded, device functionality should not be assumed, damage may occur and reliability may be affected.

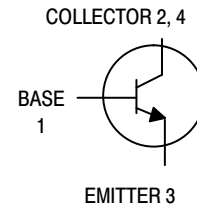
2. Device mounted on a glass epoxy printed circuit board 1.575 in. x 1.575 in. x 0.059 in.; mounting pad for the collector lead min. 0.93 in<sup>2</sup>.

\*For additional information on our Pb-Free strategy and soldering details, please download the **onsemi** Soldering and Mounting Techniques Reference Manual, SOLDERRM/D.

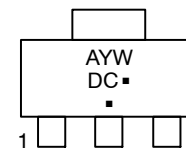
## NPN SILICON TRANSISTOR SURFACE MOUNT



SOT-223 (TO-261)  
CASE 318E  
STYLE 1



### MARKING DIAGRAM



A = Assembly Location  
Y = Year  
W = Work Week  
DC = Device Code  
▪ = Pb-Free Package

(Note: Microdot may be in either location)

### ORDERING INFORMATION

Device	Package	Shipping <sup>†</sup>
BF720T1G	SOT-223 (Pb-Free)	1,000 / Tape & Reel
SBF720T1G	SOT-223 (Pb-Free)	1,000 / Tape & Reel

### DISCONTINUED (Note 1)

BF720T3G	SOT-223 (Pb-Free)	4,000 / Tape & Reel
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<sup>†</sup>For information on tape and reel specifications, including part orientation and tape sizes, please refer to our Tape and Reel Packaging Specification Brochure, BRD8011/D.

1. **DISCONTINUED:** This device is not recommended for new design. Please contact your **onsemi** representative for information. The most current information on this device may be available on [www.onsemi.com](http://www.onsemi.com).

# BF720T1G, SBF720T1G, BF720T3G

## ELECTRICAL CHARACTERISTICS ( $T_A = 25^\circ\text{C}$ unless otherwise noted)

Characteristics	Symbol	Min	Max	Unit
<b>OFF CHARACTERISTICS</b>				
Collector-Emitter Breakdown Voltage ( $I_C = 1.0\text{ mA}$ , $I_B = 0$ )	$V_{(BR)CEO}$	300	–	Vdc
Collector-Base Breakdown Voltage ( $I_C = 100\text{ }\mu\text{A}$ , $I_E = 0$ )	$V_{(BR)CBO}$	300	–	Vdc
Collector-Emitter Breakdown Voltage ( $I_C = 100\text{ }\mu\text{A}$ , $R_{BE} = 2.7\text{ k}\Omega$ )	$V_{(BR)CER}$	300	–	Vdc
Emitter-Base Breakdown Voltage ( $I_E = 10\text{ }\mu\text{A}$ , $I_C = 0$ )	$V_{(BR)EBO}$	5.0	–	Vdc
Collector-Base Cutoff Current ( $V_{CB} = 200\text{ Vdc}$ , $I_E = 0$ )	$I_{CBO}$	–	10	nAdc
Collector-Emitter Cutoff Current ( $V_{CE} = 250\text{ Vdc}$ , $R_{BE} = 2.7\text{ k}\Omega$ ) ( $V_{CE} = 200\text{ Vdc}$ , $R_{BE} = 2.7\text{ k}\Omega$ , $T_J = 150^\circ\text{C}$ )	$I_{CER}$	– –	50 10	nAdc $\mu\text{Adc}$
<b>ON CHARACTERISTICS</b>				
DC Current Gain ( $I_C = 25\text{ mA}$ , $V_{CE} = 20\text{ Vdc}$ )	$h_{FE}$	50	–	–
Collector-Emitter Saturation Voltage ( $I_C = 30\text{ mA}$ , $I_B = 5.0\text{ mA}$ )	$V_{CE(sat)}$	–	0.6	Vdc
<b>DYNAMIC CHARACTERISTICS</b>				
Current-Gain – Bandwidth Product ( $I_C = 10\text{ mA}$ , $V_{CE} = 10\text{ Vdc}$ , $f = 35\text{ MHz}$ )	$f_T$	60	–	MHz
Feedback Capacitance ( $V_{CE} = 30\text{ Vdc}$ , $I_C = 0$ , $f = 1.0\text{ MHz}$ )	$C_{re}$	–	1.6	pF

# BF720T1G, SBF720T1G, BF720T3G

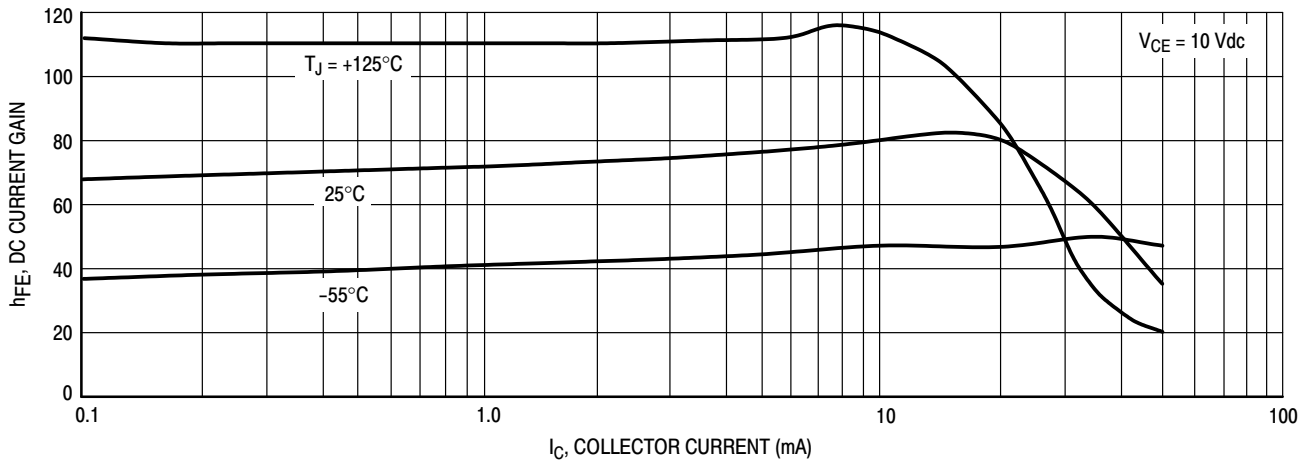


Figure 1. DC Current Gain

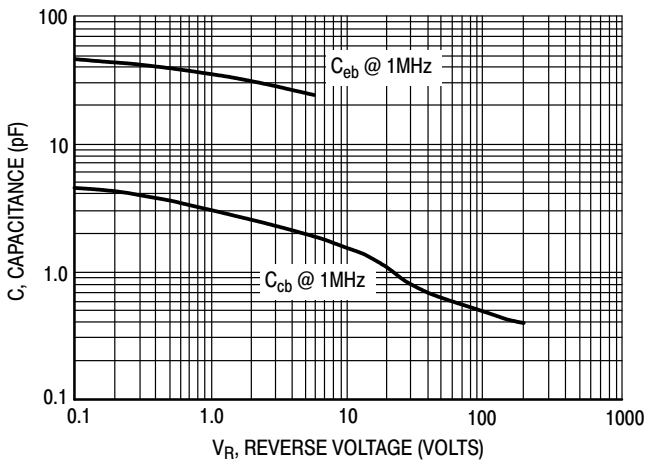


Figure 2. Capacitance

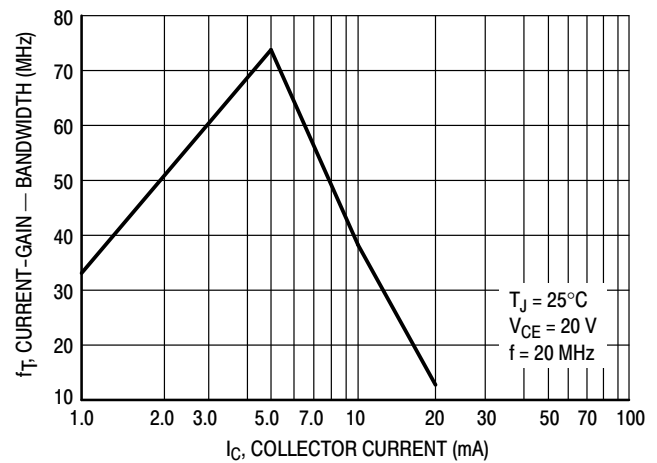


Figure 3. Current-Gain – Bandwidth

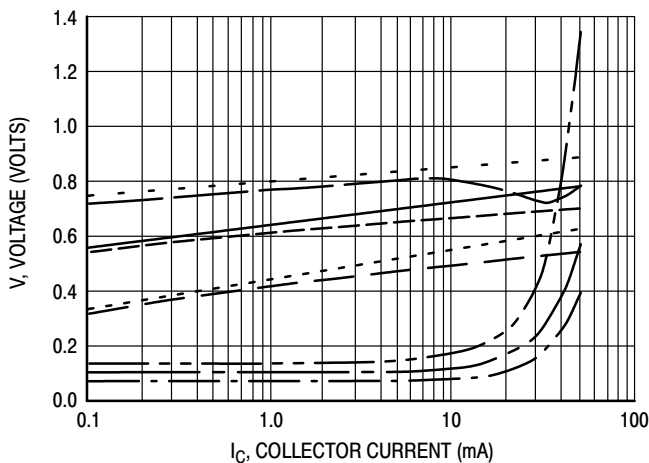


Figure 4. "ON" Voltages

- $V_{CE(sat)}$  @  $25^\circ\text{C}$ ,  $I_C/I_B = 10$
- $V_{CE(sat)}$  @  $125^\circ\text{C}$ ,  $I_C/I_B = 10$
- $V_{CE(sat)}$  @  $-55^\circ\text{C}$ ,  $I_C/I_B = 10$
- $V_{BE(sat)}$  @  $25^\circ\text{C}$ ,  $I_C/I_B = 10$
- $V_{BE(sat)}$  @  $125^\circ\text{C}$ ,  $I_C/I_B = 10$
- $V_{BE(sat)}$  @  $-55^\circ\text{C}$ ,  $I_C/I_B = 10$
- $V_{BE(on)}$  @  $25^\circ\text{C}$ ,  $V_{CE} = 10 \text{ V}$
- $V_{BE(on)}$  @  $125^\circ\text{C}$ ,  $V_{CE} = 10 \text{ V}$
- $V_{BE(on)}$  @  $-55^\circ\text{C}$ ,  $V_{CE} = 10 \text{ V}$



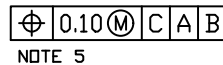
SCALE 1:1

SOT-223 (TO-261)  
CASE 318E-04  
ISSUE R

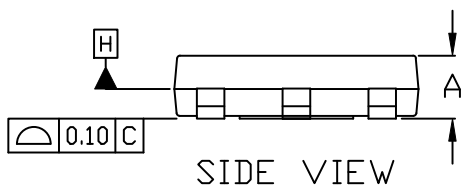
DATE 02 OCT 2018



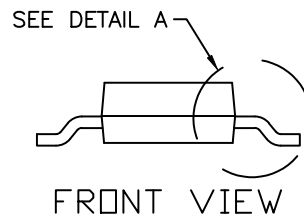
TOP VIEW



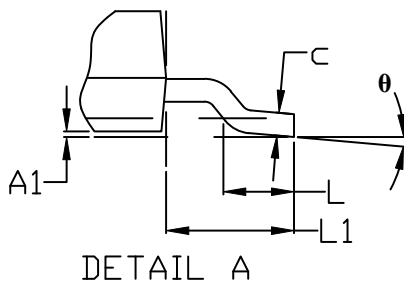
NOTE 5



SIDE VIEW



FRONT VIEW

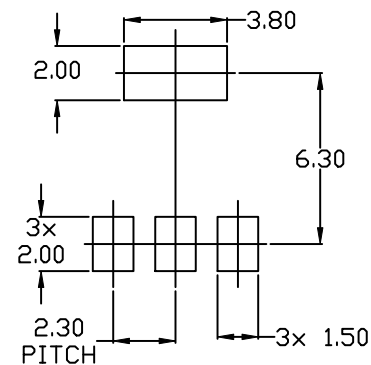


DETAIL A

NOTES:

1. DIMENSIONING AND TOLERANCING PER ASME Y14.5M, 1994.
2. CONTROLLING DIMENSION: MILLIMETERS
3. DIMENSIONS D & E DO NOT INCLUDE MOLD FLASH, PROTRUSIONS OR GATE BURRS. MOLD FLASH, PROTRUSIONS OR GATE BURRS SHALL NOT EXCEED 0.200MM PER SIDE.
4. DATUMS A AND B ARE DETERMINED AT DATUM H.
5. A1 IS DEFINED AS THE VERTICAL DISTANCE FROM THE SEATING PLANE TO THE LOWEST POINT OF THE PACKAGE BODY.
6. POSITIONAL TOLERANCE APPLIES TO DIMENSIONS b AND b1.

MILLIMETERS			
DIM	MIN.	NOM.	MAX.
A	1.50	1.63	1.75
A1	0.02	0.06	0.10
b	0.60	0.75	0.89
b1	2.90	3.06	3.20
c	0.24	0.29	0.35
D	6.30	6.50	6.70
E	3.30	3.50	3.70
e	2.30 BSC		
L	0.20	---	---
L1	1.50	1.75	2.00
He	6.70	7.00	7.30
θ	0°	---	10°



RECOMMENDED MOUNTING  
FOOTPRINT

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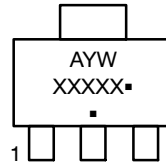
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**SOT-223 (TO-261)**  
**CASE 318E-04**  
**ISSUE R**

DATE 02 OCT 2018

<b>STYLE 1:</b> PIN 1. BASE 2. COLLECTOR 3. EMITTER 4. COLLECTOR	<b>STYLE 2:</b> PIN 1. ANODE 2. CATHODE 3. NC 4. CATHODE	<b>STYLE 3:</b> PIN 1. GATE 2. DRAIN 3. SOURCE 4. DRAIN	<b>STYLE 4:</b> PIN 1. SOURCE 2. DRAIN 3. GATE 4. DRAIN	<b>STYLE 5:</b> PIN 1. DRAIN 2. GATE 3. SOURCE 4. GATE
<b>STYLE 6:</b> PIN 1. RETURN 2. INPUT 3. OUTPUT 4. INPUT	<b>STYLE 7:</b> PIN 1. ANODE 1 2. CATHODE 3. ANODE 2 4. CATHODE	<b>STYLE 8:</b> CANCELLED	<b>STYLE 9:</b> PIN 1. INPUT 2. GROUND 3. LOGIC 4. GROUND	<b>STYLE 10:</b> PIN 1. CATHODE 2. ANODE 3. GATE 4. ANODE
<b>STYLE 11:</b> PIN 1. MT 1 2. MT 2 3. GATE 4. MT 2	<b>STYLE 12:</b> PIN 1. INPUT 2. OUTPUT 3. NC 4. OUTPUT	<b>STYLE 13:</b> PIN 1. GATE 2. COLLECTOR 3. EMITTER 4. COLLECTOR		

**GENERIC  
MARKING DIAGRAM\***



A = Assembly Location  
 Y = Year  
 W = Work Week  
 XXXXX = Specific Device Code  
 ■ = Pb-Free Package

(Note: Microdot may be in either location)  
 \*This information is generic. Please refer to device data sheet for actual part marking. Pb-Free indicator, "G" or microdot "■", may or may not be present. Some products may not follow the Generic Marking.

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