BUL642D2

High Speed, High Gain Bipolar NPN Transistor with Integrated Collector-Emitter and Built-in Efficient Antisaturation Network

The BUL642D2 is a state−of−the−art High Speed High Gain Bipolar Transistor (H2BIP). Tight dynamic characteristics and lot to lot minimum spread (150 ns on storage time) make it ideally suitable for Light Ballast Application. A new development process brings avalanche energy capability, making the device extremely rugged.

Features

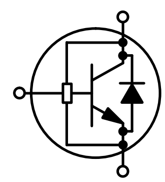
- Low Base Drive Requirement
- High Peak DC Current Gain (55 Typical) @ I_C = 300 mA/5 V
- Extremely Low Storage Time Min/Max Guarantees Due to the H2BIP Structure which Minimizes the Spread
- Integrated Collector−Emitter Free Wheeling Diode
- Fully Characterized Dynamic V_{CEsat}
- "Six Sigma" Process Providing Tight and Reproducible Parameter Spreads
- Avalanche Energy 20 mJ Typical Capability
- Pb−Free Package is Available*

*For additional information on our Pb−Free strategy and soldering details, please download the ON Semiconductor Soldering and Mounting Techniques Reference Manual, SOLDERRM/D.

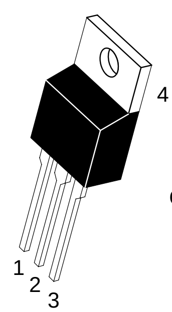
ON Semiconductor®

http://onsemi.com

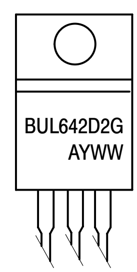
3 AMPERES
825 VOLTS
75 WATTS
POWER TRANSISTOR



MARKING DIAGRAM



TO−220AB
CASE 221A
STYLE 1



BUL642D2	= Device Code
A	= Assembly Location
Y	= Year
WW	= Work Week
G	= Pb−Free Package

ORDERING INFORMATION

Device	Package	Shipping
BUL642D2	TO−220	50 Units/Rail
BUL642D2G	TO−220 (Pb−Free)	50 Units/Rail

MAXIMUM RATINGS

Rating	Symbol	Value	Unit
Collector−Emitter Sustaining Voltage	V_{CEO}	440	Vdc
Collector−Base Breakdown Voltage	V_{CES}	825	Vdc
Emitter−Base Voltage	V_{EBO}	11	Vdc
Collector Current − Continuous − Peak (Note 1)	I_C I_{CM}	3.0 8.0	Adc
Base Current − Continuous − Peak (Note 1)	I_B I_{BM}	2.0 4.0	Adc
*Total Device Dissipation @ T_C = 25°C *Derate above 25°C	P_D	75 0.6	W W/°C
Operating and Storage Temperature	T_J, T_{stg}	−65 to +150	°C

Maximum ratings are those values beyond which device damage can occur. Maximum ratings applied to the device are individual stress limit values (not normal operating conditions) and are not valid simultaneously. If these limits are exceeded, device functional operation is not implied, damage may occur and reliability may be affected.

TYPICAL GAIN

Rating	Symbol	Value	Unit
Typical Gain @ I_C = 1 A, V_{CE} = 2 V Typical A, V_{CE} = 1 V	h_{FE} h_{FE}	45 50	− −

THERMAL CHARACTERISTICS

Characteristic	Symbol	Value	Unit
Thermal Resistance, Junction−to−Case	$R_{\theta JC}$	1.6	°C/W
Thermal Resistance, Junction−to−Ambient	$R_{\theta JA}$	62.5	°C/W
Maximum Lead Temperature for Soldering Purposes: 1/8 in. from Case for 5 seconds	T_L	260	°C

1. Pulse Test: Pulse Width = 5.0 ms, Duty Cycle = 10%

ELECTRICAL CHARACTERISTICS (T_C = 25°C unless otherwise noted)

Characteristic				Symbol	Min	Typ	Max	Unit
OFF CHARACTERISTICS								
Collector−Emitter Sustaining Voltage (I_C = 200 mA, L = 25 mH)				$V_{CEO(sus)}$	440	–	–	Vdc
Collector−Base Breakdown Voltage (I_{CBO} = 1 mA)				V_{CBO}	825	–	–	Vdc
Emitter−Base Breakdown Voltage (I_{EBO} = 1 mA)				V_{EBO}	11	–	–	Vdc
Collector Cutoff Current (V_{CE} = Rated V_{CEO}, I_B = 0)			@ T_C = 25°C @ T_C = 125°C	I_{CEO}	– –	– –	200 1000	μAdc
Collector Cutoff Current (V_{CE} = Rated V_{CES}, V_{EB} = 0)			@ T_C = 25°C @ T_C = 125°C	I_{CES}	– –	– –	100 1000	μAdc
Emitter−Cutoff Current (V_{EB} = 10 Vdc, I_C = 0)				I_{EBO}	–	–	100	μAdc
ON CHARACTERISTICS								
Base−Emitter Saturation Voltage (IC = 0.5 Adc, I_B = 100 mAdc (I_C = 1 Adc, I_B = 0.2 Adc)				$V_{BE(sat)}$	– –	– –	1.1 1.5	Vdc
Collector−Emitter Saturation Voltage (I_C = 0.5 Adc, I_B = 50 mAdc) (I_C = 2 Adc, I_B = 0.2 Adc)				$V_{CE(sat)}$	– –	– –	0.5 1.5	Vdc
DC Current Gain (I_C = 0.5 Adc, V_{CE} = 1 Vdc) (I_C = 0.5 Adc, V_{CE} = 3 Vdc)				h_{FE}	16 18	– –	– –	–
DYNAMIC SATURATION VOLTAGE								
Dynamic Saturation Voltage:	I_C = 0.5 Adc I_{B1} = 50 mAdc V_{CC} = 125 Vdc	@ 1 μs	@ T_C = 25°C @ T_C = 125°C	$V_{CE(dsat)}$	– –	2.0 5.0	– –	V
		@ 3 μs	@ T_C = 25°C		– –	0.2 1.3	– –	
	I_C = 1 Adc I_{B1} = 100 mAdc V_{CC} = 300 Vdc	@ 1 μs	@ T_C = 25°C @ T_C = 125°C		– –	4.5 10	– –	
		@ 3 μs	@ T_C = 25°C		– –	1.0 3.0	– –	
DYNAMIC CHARACTERISTICS								
Current Gain Bandwidth I_C = 0.5 Adc, V_{CE} = 10 Vdc, f = 1 MHz				f_T	–	13	–	MHz
Output Capacitance @ V_{cb} = 10 V, I_E = 0, f = 1 MHz				C_{ob}	–	70	150	pF
Input Capacitance @ V_{EB} = 8 V, f = 1 MHz				C_{ib}	–	500	1000	pF
DIODE CHARACTERISTICS								
Forward Diode Voltage (I_{EC} = 0.5 Adc) (I_{EC} = 1.0 Adc)				V_{EC}	– –	0.8 1.0	1.5 2.0	V
SWITCHING CHARACTERISTICS: Resistive Load (D.C. ≤ 10%, Pulse Width = 70 μs)								
Delay Time			I_C = 0.5 Adc	t_d	–	60	400	ns
Rise Time			I_{B1} = 45 mA	t_r	–	160	1100	ns
Storage Time			I_{B2} = 500 mA	t_s	–	0.5	1400	μs
Fall Time			V_{CC} = 125 V	t_f	–	0.4	600	ns

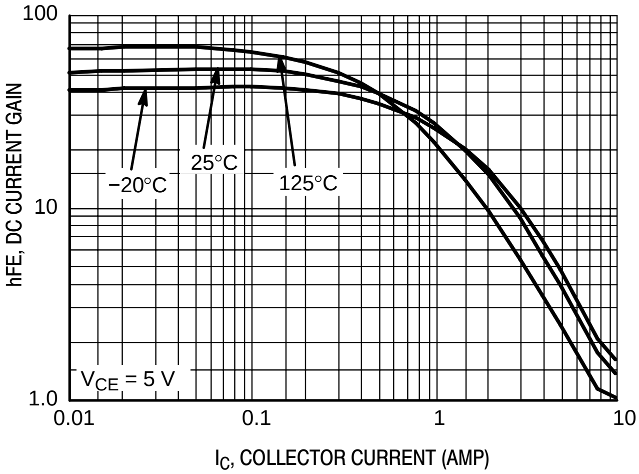


Figure 1. DC Current Gain

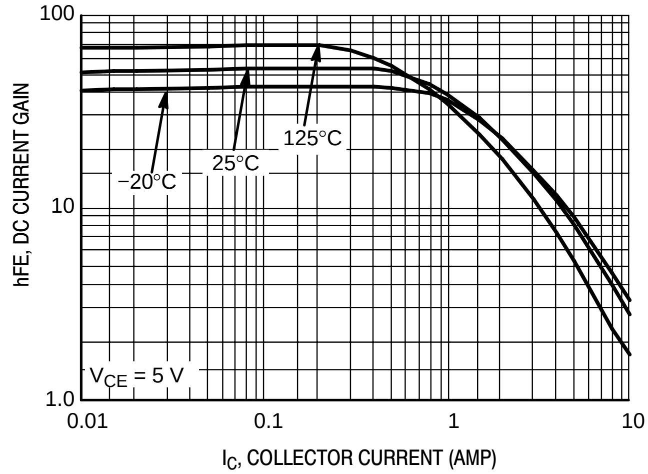


Figure 2. DC Current Gain

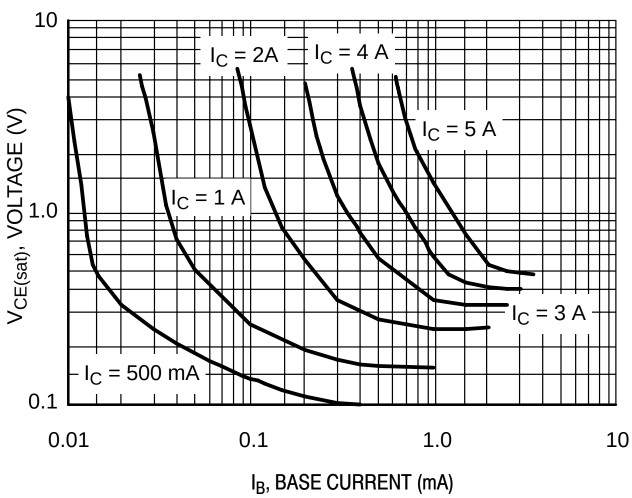


Figure 3. Collector Saturation Region

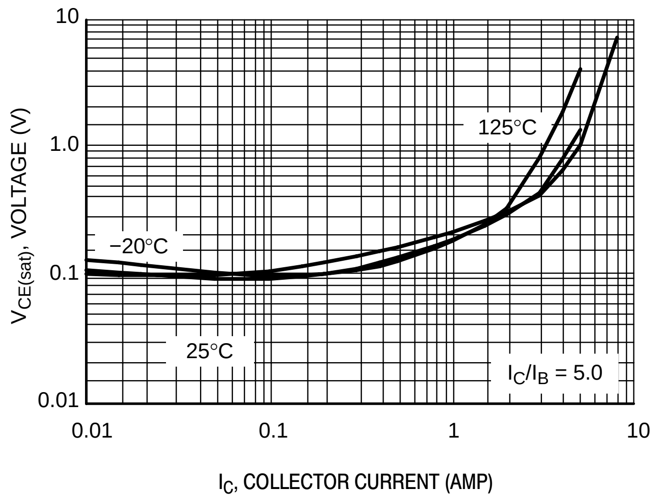


Figure 4. Collector−Emitter Saturation Voltage

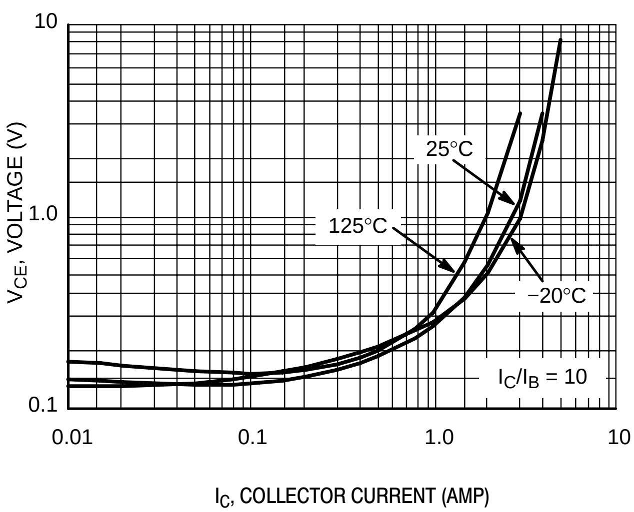


Figure 5. Collector−Emitter Saturation Voltage

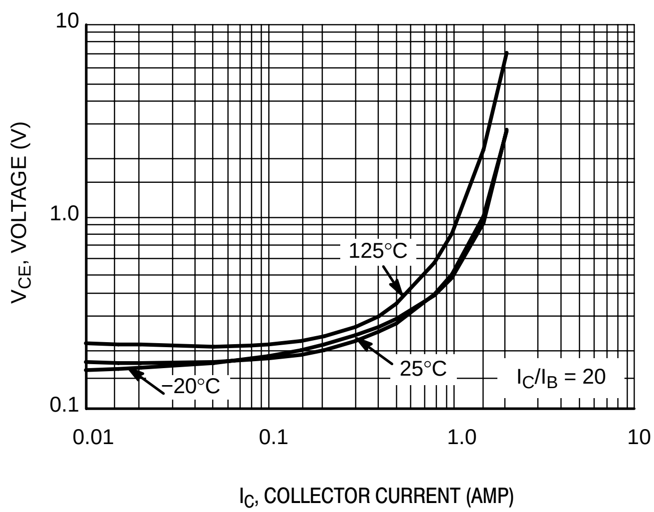


Figure 6. Collector−Emitter Saturation Voltage

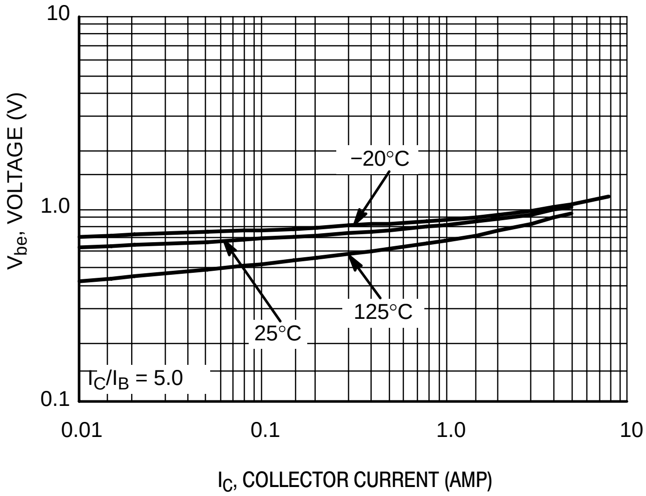


Figure 7. Base−Emitter Saturation Voltage

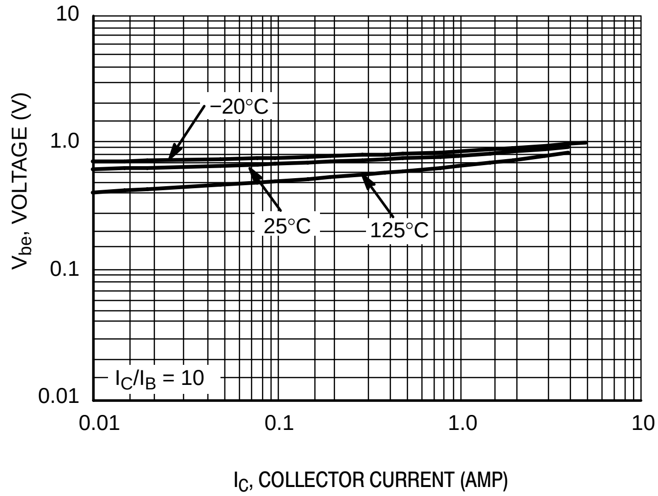


Figure 8. Base−Emitter Saturation Voltage

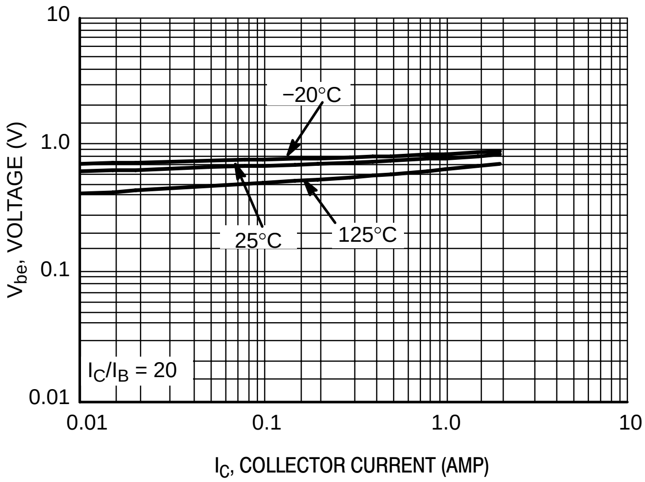


Figure 9. Base−Emitter Saturation Voltage

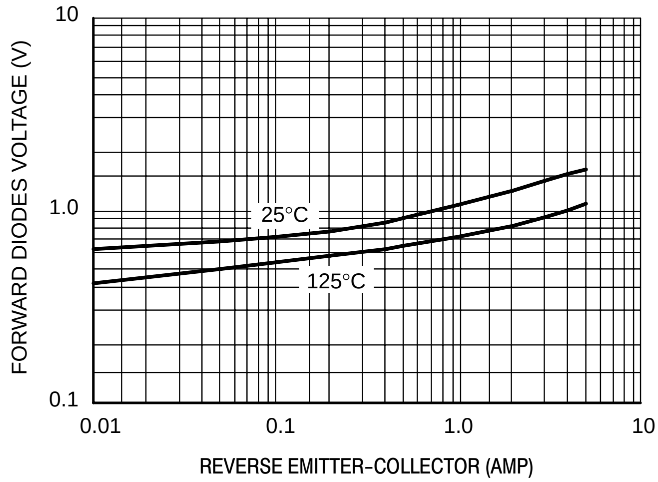


Figure 10. Forward Diode Voltage

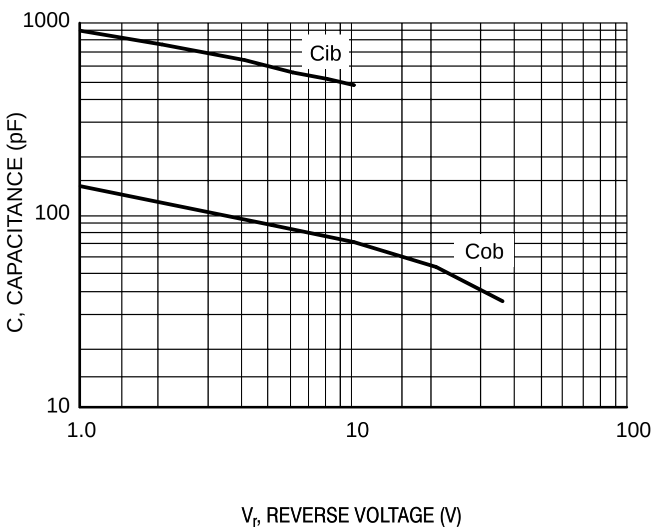


Figure 11. Capacitance

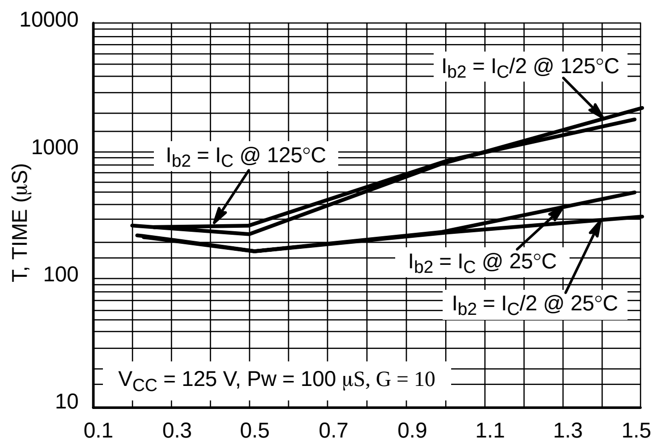


Figure 12. Resistive Switch Time, Storage Time T_{ON}

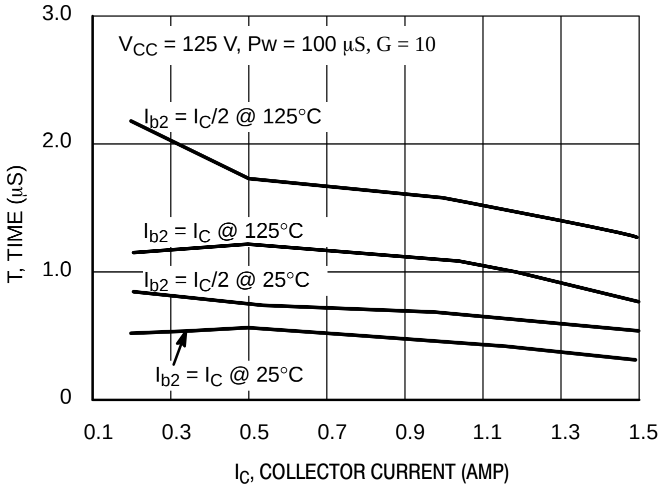


Figure 13. Resistive Switch Time, Storage Time

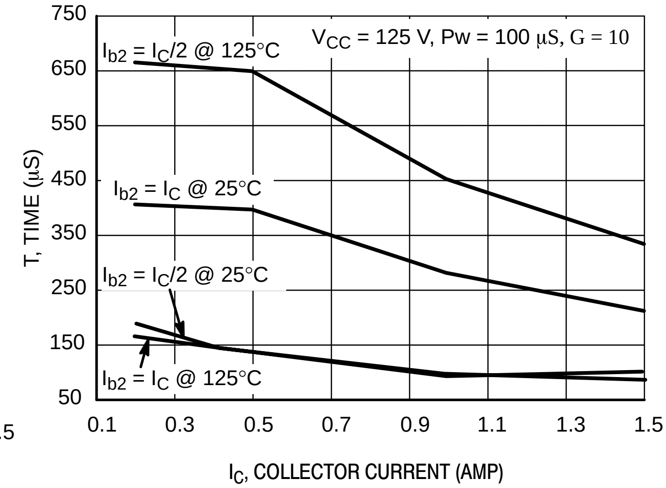


Figure 14. Resistive Switch Time, Fall Time

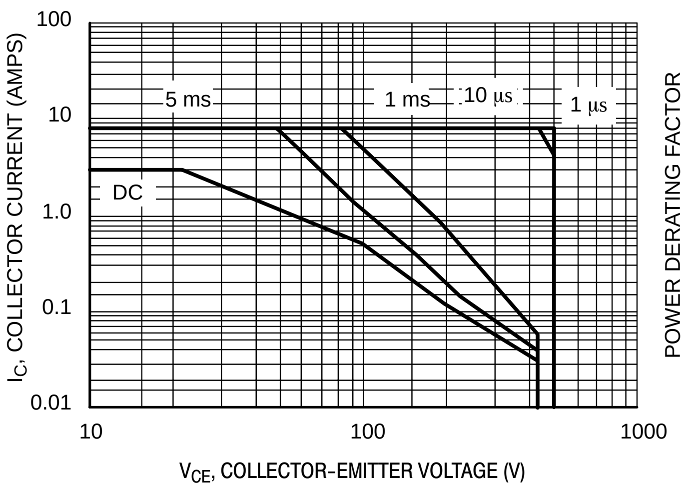


Figure 15.

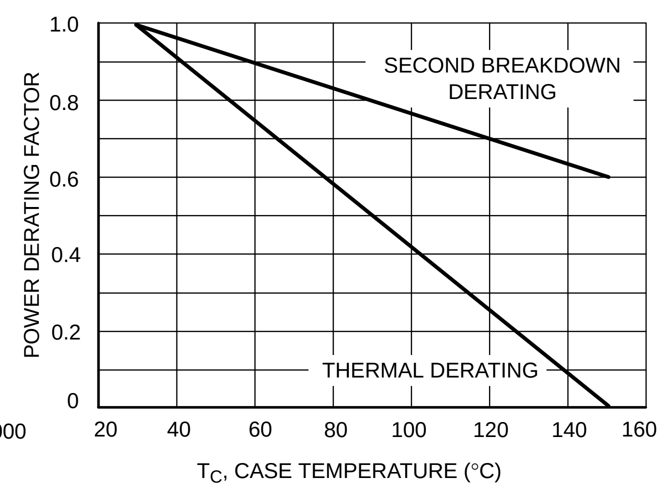
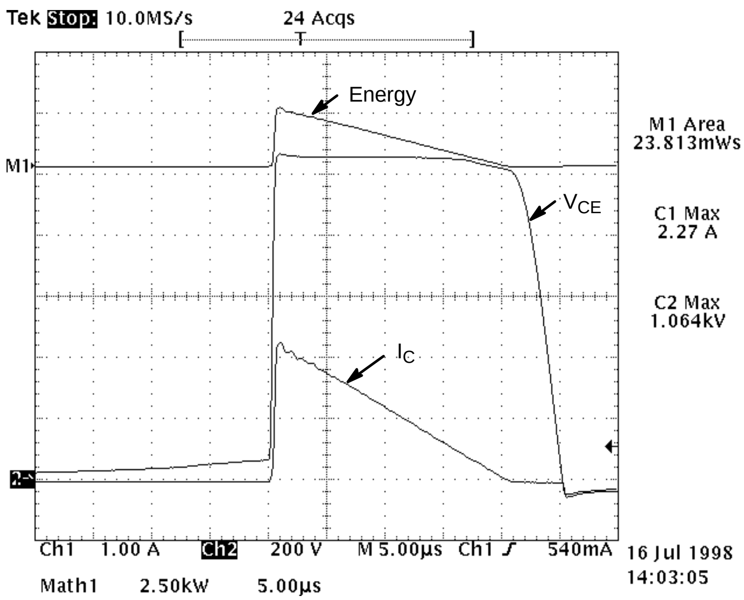


Figure 16. Power Derating

There are two limitations on the power handling ability of a transistor: average junction temperature and second breakdown. Safe operating area curves indicate I_C-V_{CE} limits of the transistor that must be observed for reliable operation; i.e., the transistor must not be subjected to greater dissipation than the curves indicate. The data of Figure 15 is based on $T_C = 25°C$; $T_{j(pk)}$ is variable depending on power level. Second breakdown pulse limits do not derate like thermal limitations. Allowable current at the voltages shown on Figure 10 may be found at any case temperature by using the appropriate curve on Figure 16.

$T_{j(pk)}$ may be calculated from the data in Figure 18. At any case temperatures, thermal limitations will reduce the power that can be handled to values less than the limitations imposed by second breakdown.



NPD CHARACTERIZATION LAB

Figure 17. Typical Avalanche Energy Test/Waveforms

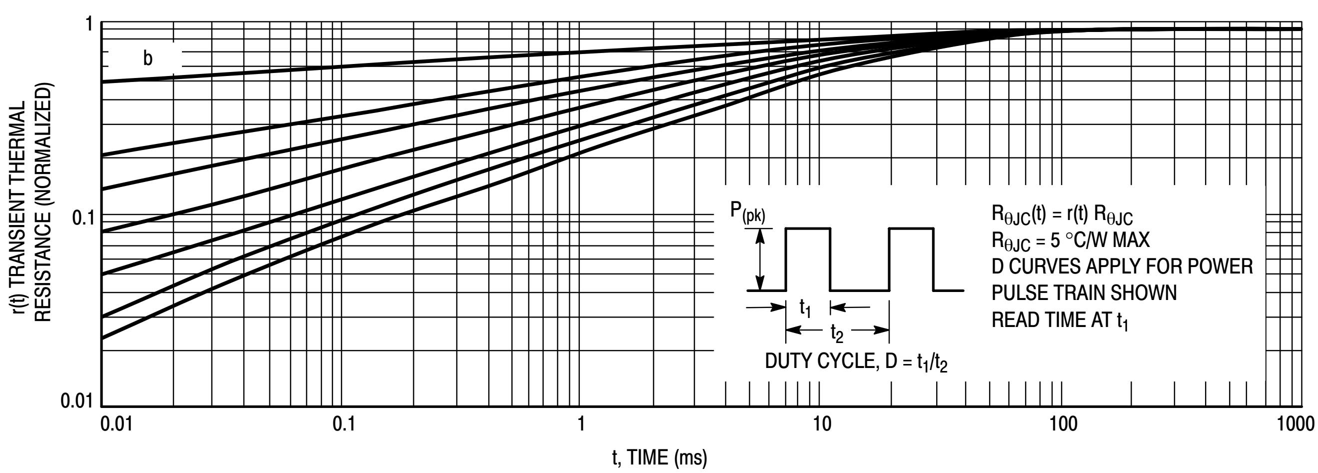


Figure 18. Thermal Response

ADDITIONAL INFORMATION

TECHNICAL PUBLICATIONS:
Technical Library: www.onsemi.com/design/resources/technical−documentation
onsemi Website: www.onsemi.com

ONLINE SUPPORT: www.onsemi.com/support
For additional information, please contact your local Sales Representative at www.onsemi.com/support/sales