

# Complementary Bias Resistor Transistors

## R1 = 2.2/47 kΩ, R2 = 47 kΩ

### NPN and PNP Transistors with Monolithic Bias Resistor Network

## NSVBC143JPDXV6

This series of digital transistors is designed to replace a single device and its external resistor bias network. The Bias Resistor Transistor (BRT) contains a single transistor with a monolithic bias network consisting of two resistors; a series base resistor and a base-emitter resistor. The BRT eliminates these individual components by integrating them into a single device. The use of a BRT can reduce both system cost and board space.

### Features

- Simplifies Circuit Design
- Reduces Board Space
- Reduces Component Count
- NSV Prefix for Automotive and Other Applications Requiring Unique Site and Control Change Requirements; AEC-Q101 Qualified and PPAP Capable\*
- These Devices are Pb-Free, Halogen Free/BFR Free and are RoHS Compliant

### MAXIMUM RATINGS

(T<sub>A</sub> = 25°C both polarities Q<sub>1</sub> (PNP) & Q<sub>2</sub> (NPN), unless otherwise noted)

Rating	Symbol	Max	Unit
Collector-Base Voltage	V <sub>CBO</sub>	50	Vdc
Collector-Emitter Voltage	V <sub>CEO</sub>	50	Vdc
Collector Current – Continuous	I <sub>C</sub>	100	mAdc
Input Forward Voltage	V <sub>IN(fwd)</sub>	12	Vdc
Input Reverse Voltage	V <sub>IN(rev)</sub>	5	Vdc

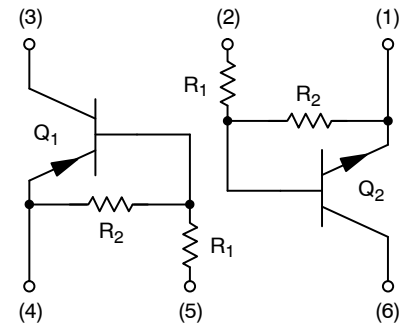
Stresses exceeding those listed in the Maximum Ratings table may damage the device. If any of these limits are exceeded, device functionality should not be assumed, damage may occur and reliability may be affected.

### ORDERING INFORMATION

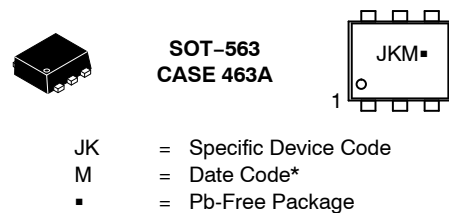
Device	Package	Shipping†
NSVBC143JPDXV6T5G	SOT-563	8,000/Tape & Reel
NSVBC143JPDXV6T1G	SOT-563	4,000/Tape & Reel

†For information on tape and reel specifications, including part orientation and tape sizes, please refer to our Tape and Reel Packaging Specifications Brochure, BRD8011/D.

### PIN CONNECTIONS



### MARKING DIAGRAM



# NSVBC143JPDXV6

## THERMAL CHARACTERISTICS

Characteristic	Symbol	Max	Unit
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### NSVBC143JPDXV6 (SOT-563) ONE JUNCTION HEATED

Total Device Dissipation T <sub>A</sub> = 25°C (Note 1) Derate above 25°C (Note 1)	P <sub>D</sub>	357 2.9	mW mW/°C
Thermal Resistance, Junction to Ambient (Note 1)	R <sub>θJA</sub>	350	°C/W

### NSVBC143JPDXV6 (SOT-563) BOTH JUNCTION HEATED (Note 2)

Total Device Dissipation T <sub>A</sub> = 25°C (Note 1) Derate above 25°C (Note 1)	P <sub>D</sub>	500 4.0	mW mW/°C
Thermal Resistance, Junction to Ambient (Note 1)	R <sub>θJA</sub>	250	°C/W
Junction and Storage Temperature Range	T <sub>J</sub> , T <sub>stg</sub>	-55 to +150	°C

- FR-4 @ Minimum Pad.
- Both junction heated values assume total power is sum of two equally powered channels.

# NSVBC143JPD XV6

## ELECTRICAL CHARACTERISTICS (T<sub>A</sub> = 25°C both polarities Q<sub>1</sub> (PNP) & Q<sub>2</sub> (NPN), unless otherwise noted)

Characteristic	Symbol	Min	Typ	Max	Unit
<b>OFF CHARACTERISTICS</b>					
Collector-Base Cutoff Current (V <sub>CB</sub> = 50 V, I <sub>E</sub> = 0)	I <sub>CBO</sub>	–	–	100	nAdc
Collector-Emitter Cutoff Current (V <sub>CE</sub> = 50 V, I <sub>B</sub> = 0)	I <sub>CEO</sub>	–	–	500	nAdc
Emitter-Base Cutoff Current (V <sub>EB</sub> = 6.0 V, I <sub>C</sub> = 0)	I <sub>EBO</sub>	–	–	0.2	mAdc
Collector-Base Breakdown Voltage (I <sub>C</sub> = 10 μA, I <sub>E</sub> = 0)	V <sub>(BR)CBO</sub>	50	–	–	Vdc
Collector-Emitter Breakdown Voltage (Note 3) (I <sub>C</sub> = 2.0 mA, I <sub>B</sub> = 0)	V <sub>(BR)CEO</sub>	50	–	–	Vdc

## ON CHARACTERISTICS

DC Current Gain (Note 3) (I <sub>C</sub> = 5.0 mA, V <sub>CE</sub> = 10 V)	h <sub>FE</sub>	80	140	–	
Collector-Emitter Saturation Voltage (Note 3) (I <sub>C</sub> = 10 mA, I <sub>B</sub> = 0.3 mA)	V <sub>CE(sat)</sub>	–	–	0.25	V
Input Voltage (Off) (V <sub>CE</sub> = 5.0 V, I <sub>C</sub> = 100 μA) (NPN) (V <sub>CE</sub> = 5.0 V, I <sub>C</sub> = 100 μA) (PNP)	V <sub>i(off)</sub>	– –	1.2 0.6	0.8 0.5	Vdc
Input Voltage (On) (V <sub>CE</sub> = 0.3 V, I <sub>C</sub> = 2.0 mA) (NPN) (V <sub>CE</sub> = 0.3 V, I <sub>C</sub> = 5.0 mA) (PNP)	V <sub>i(on)</sub>	3.0 1.1	1.6 0.8	– –	Vdc
Output Voltage (On) (V <sub>CC</sub> = 5.0 V, V <sub>B</sub> = 3.5 V, R <sub>L</sub> = 1.0 kΩ) (NPN) (V <sub>CC</sub> = 5.0 V, V <sub>B</sub> = 2.5 V, R <sub>L</sub> = 1.0 kΩ) (PNP)	V <sub>OL</sub>	– –	– –	0.2 0.2	Vdc
Output Voltage (Off) (V <sub>CC</sub> = 5.0 V, V <sub>B</sub> = 0.5 V, R <sub>L</sub> = 1.0 kΩ)	V <sub>OH</sub>	4.9	–	–	Vdc
Input Resistor (NPN) Input Resistor (PNP)	R <sub>I</sub>	32.9 1.5	47 2.2	61.1 2.9	kΩ
Resistor Ratio (NPN) Resistor Ratio (PNP)	R <sub>1</sub> /R <sub>2</sub>	0.8 0.038	1.0 0.047	1.2 0.056	

Product parametric performance is indicated in the Electrical Characteristics for the listed test conditions, unless otherwise noted. Product performance may not be indicated by the Electrical Characteristics if operated under different conditions.

3. Pulsed Condition: Pulse Width = 300 ms, Duty Cycle ≤ 2%.

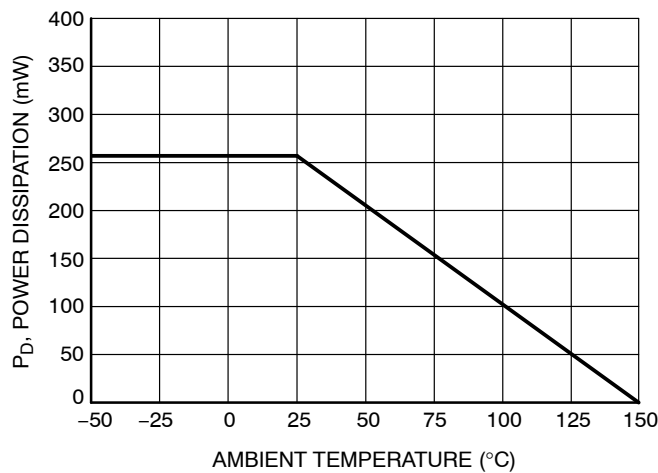


Figure 1. Derating Curve

TYPICAL CHARACTERISTICS – NPN TRANSISTOR

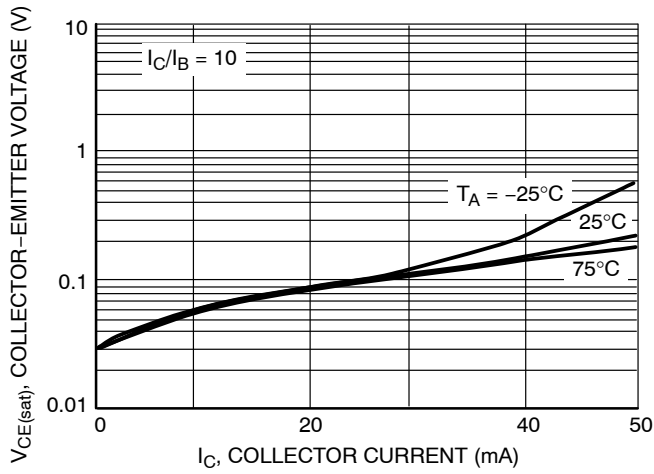


Figure 2.  $V_{CE(sat)}$  vs.  $I_C$

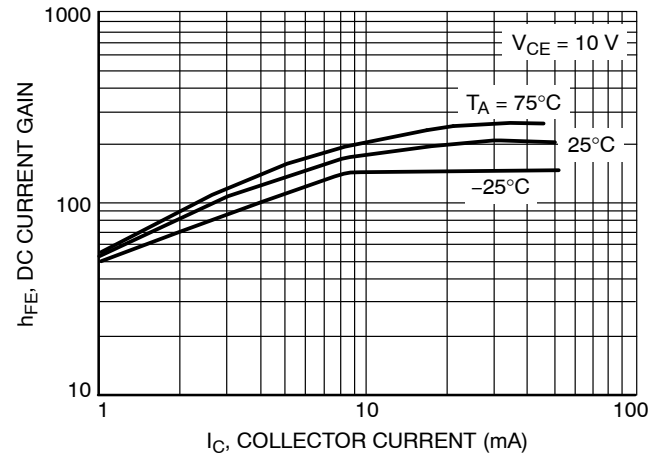


Figure 3. DC Current Gain

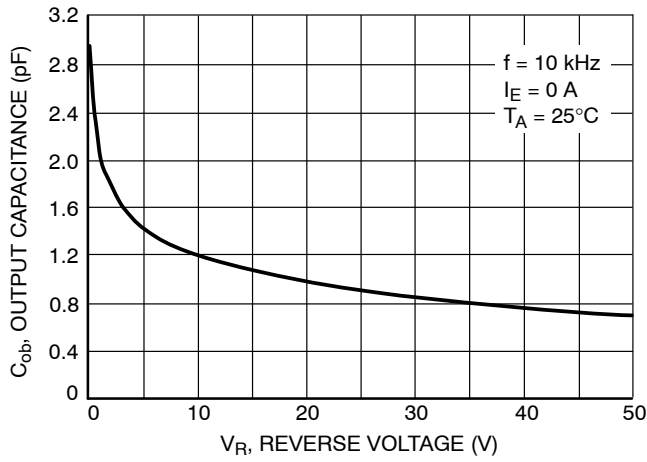


Figure 4. Output Capacitance

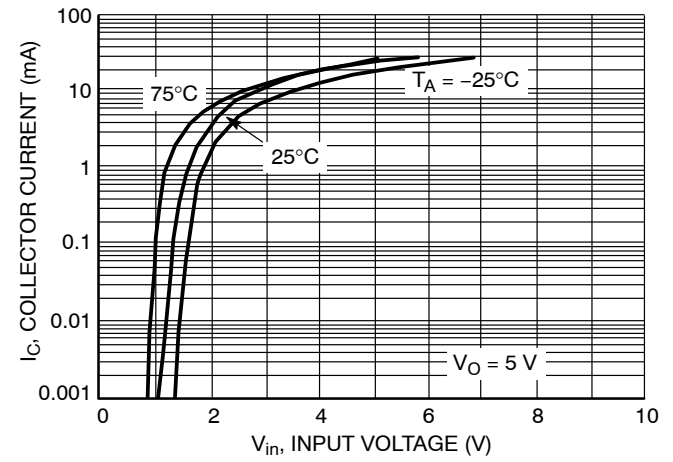


Figure 5. Output Current vs. Input Voltage

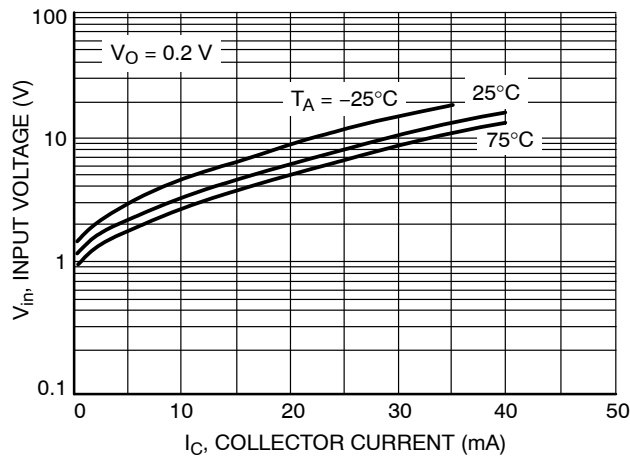


Figure 6. Input Voltage vs. Output Current

TYPICAL CHARACTERISTICS – PNP TRANSISTOR

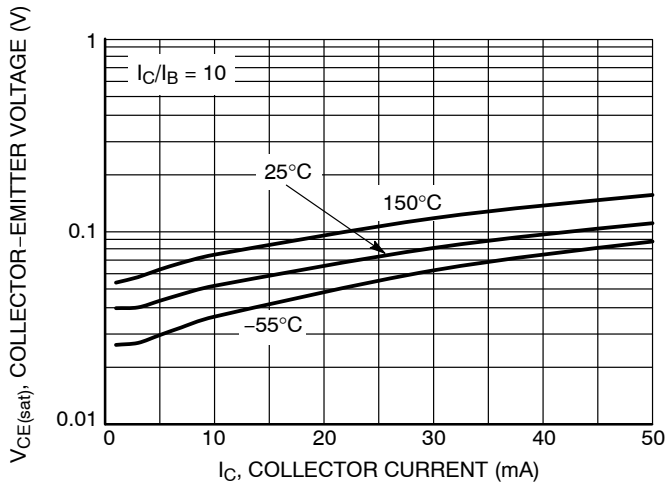


Figure 7.  $V_{CE(sat)}$  vs.  $I_C$

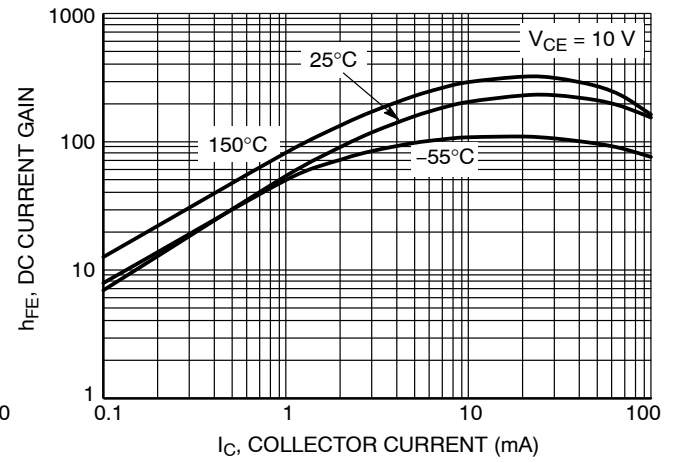


Figure 8. DC Current Gain

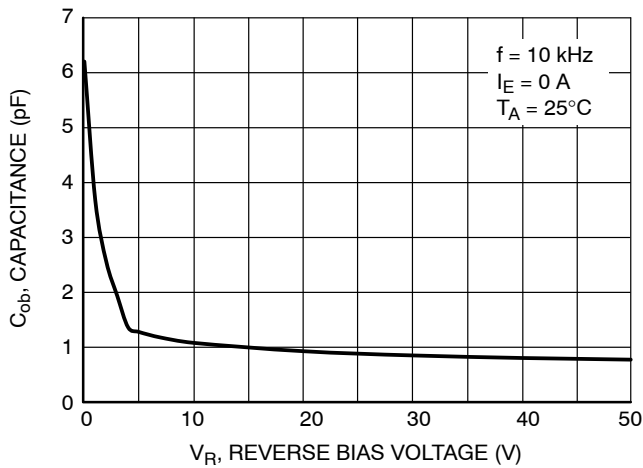


Figure 9. Output Capacitance

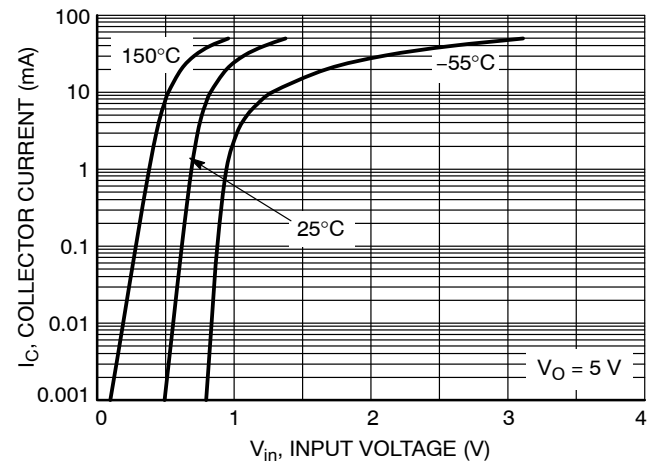


Figure 10. Output Current vs. Input Voltage

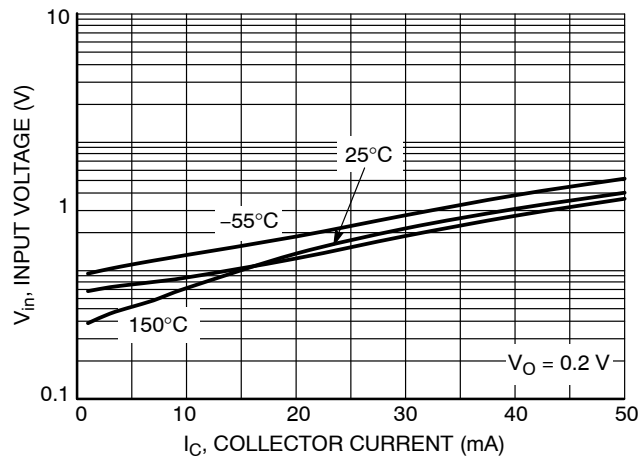


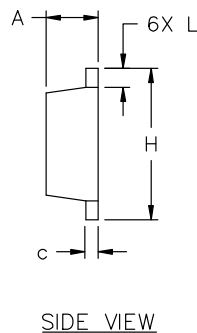
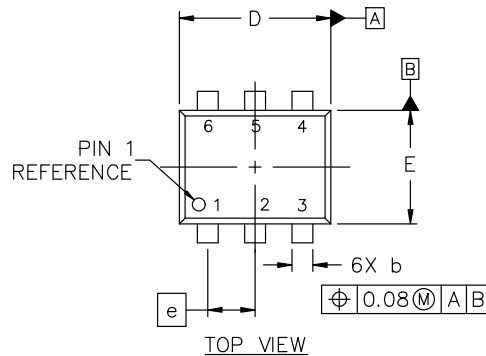
Figure 11. Input Voltage vs. Output Current


**SOT-563-6 1.60x1.20x0.55, 0.50P**  
**CASE 463A**  
**ISSUE J**

15 FEB 2024

## NOTES:

1. DIMENSIONING AND TOLERANCING CONFORM TO ASME Y14.5-2018.
2. ALL DIMENSION ARE IN MILLIMETERS.
3. MAXIMUM LEAD THICKNESS INCLUDES LEAD FINISH THICKNESS. MINIMUM LEAD THICKNESS IS THE MINIMUM THICKNESS OF BASE MATERIAL.



DIM	MILLIMETERS		
	MIN.	NOM.	MAX.
A	0.50	0.55	0.60
b	0.17	0.22	0.27
c	0.08	0.13	0.18
D	1.50	1.60	1.70
E	1.10	1.20	1.30
e	0.50 BSC		
H	1.50	1.60	1.70
L	0.10	0.20	0.30

STYLE 1:  
PIN 1. EMITTER 1  
2. BASE 1  
3. COLLECTOR 2  
4. EMITTER 2  
5. BASE 2  
6. COLLECTOR 1

STYLE 2:  
PIN 1. EMITTER 1  
2. EMITTER 2  
3. BASE 2  
4. COLLECTOR 2  
5. BASE 1  
6. COLLECTOR 1

STYLE 3:  
PIN 1. CATHODE 1  
2. CATHODE 1  
3. ANODE/ANODE 2  
4. CATHODE 2  
5. CATHODE 2  
6. ANODE/ANODE 1

STYLE 4:  
PIN 1. COLLECTOR  
2. COLLECTOR  
3. BASE  
4. EMITTER  
5. COLLECTOR  
6. COLLECTOR

STYLE 5:  
PIN 1. CATHODE  
2. CATHODE  
3. ANODE  
4. ANODE  
5. CATHODE  
6. CATHODE

STYLE 6:  
PIN 1. CATHODE  
2. ANODE  
3. CATHODE  
4. CATHODE  
5. CATHODE  
6. CATHODE

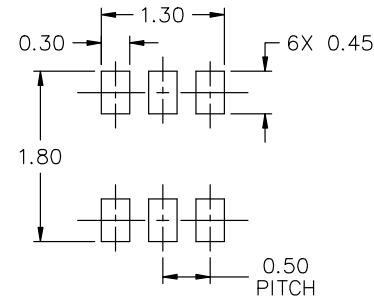
STYLE 7:  
PIN 1. CATHODE  
2. ANODE  
3. CATHODE  
4. CATHODE  
5. ANODE  
6. CATHODE

STYLE 8:  
PIN 1. DRAIN  
2. DRAIN  
3. GATE  
4. SOURCE  
5. DRAIN  
6. DRAIN

STYLE 9:  
PIN 1. SOURCE 1  
2. GATE 1  
3. DRAIN 2  
4. SOURCE 2  
5. GATE 2  
6. DRAIN 1

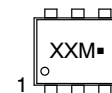
STYLE 10:  
PIN 1. CATHODE 1  
2. N/C  
3. CATHODE 2  
4. ANODE 2  
5. N/C  
6. ANODE 1

STYLE 11:  
PIN 1. EMITTER 2  
2. BASE 2  
3. COLLECTOR 1  
4. EMITTER 1  
5. BASE 1  
6. COLLECTOR 2



## RECOMMENDED MOUNTING FOOTPRINT\*

- \* FOR ADDITIONAL INFORMATION ON OUR Pb-FREE STRATEGY AND SOLDERING DETAILS, PLEASE DOWNLOAD THE ON SEMICONDUCTOR SOLDERING AND MOUNTING TECHNIQUES REFERENCE MANUAL, SOLDERM/D.

**GENERIC MARKING DIAGRAM\***


XX = Specific Device Code

M = Month Code

▪ = Pb-Free Package

\*This information is generic. Please refer to device data sheet for actual part marking. Pb-Free indicator, "G" or microdot "▪", may or may not be present. Some products may not follow the Generic Marking.

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