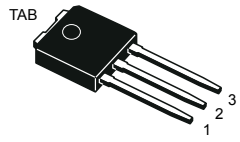
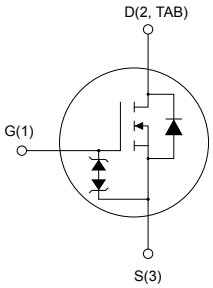
N-channel 620 V, 0.95 Ω typ., 5.5 A MDmesh K3 Power MOSFET in an IPAK package



IPAK



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Features

Order code	V_{DS}	$R_{DS(on)}$ max.	I_D
STU6N62K3	620 V	1.2 Ω	5.5 A

- 100% avalanche tested
- Extremely high dv/dt capability
- Very low intrinsic capacitance
- Improved diode reverse recovery characteristics
- Zener-protected

Applications

- Switching applications

Description

This MDmesh K3 Power MOSFET is the result of improvements applied to STMicroelectronics' MDmesh technology, combined with a new optimized vertical structure. This device boasts an extremely low on-resistance, superior dynamic performance and high avalanche capability, rendering it suitable for the most demanding applications.

Product status link
STU6N62K3

Product summary	
Order code	STU6N62K3
Marking	6N62K3
Package	IPAK
Packing	Tube

1 Electrical ratings

Table 1. Absolute maximum ratings

Symbol	Parameter	Value	Unit
V_{DS}	Drain-source voltage	620	V
V_{GS}	Gate-source voltage	±30	V
I_D	Drain current (continuous) at T_C = 25 °C	5.5	A
	Drain current (continuous) at T_C = 100 °C	3	
I_{DM} (1)	Drain current (pulsed)	22	A
P_{TOT}	Total power dissipation at T_C = 25 °C	90	W
ESD	Gate-source human body model (R=1.5 kΩ, C=100 pF)	2.5	kV
dv/dt (2)	Peak diode recovery voltage slope	12	V/ns
T_{stg}	Storage temperature range	-55 to 150	°C
T_J	Operating junction temperature range		°C

1. *Pulse width limited by safe operating area.*
2. *I_{SD} ≤ 5.5 A, di/dt ≤ 400 A/µs, V_{DS} (peak) ≤ $V_{(BR)DSS}$, V_{DD} = 80% $V_{(BR)DSS}$.*

Table 2. Thermal data

Symbol	Parameter	Value	Unit
R_{thJC}	Thermal resistance, junction-to-case	1.39	°C/W
R_{thJA}	Thermal resistance, junction-to-ambient	100	°C/W

Table 3. Avalanche characteristics

Symbol	Parameter	Value	Unit
I_{AR}	Avalanche current, repetitive or not repetitive (pulse width is limited by T_J max.)	5.5	A
E_{AS}	Single pulse avalanche energy (starting T_J = 25 °C, I_D = I_{AR}, V_{DD} = 50 V)	140	mJ

2 Electrical characteristics

T_C = 25 °C unless otherwise specified.

Table 4. On/off states

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
$V_{(BR)DSS}$	Drain-source breakdown voltage	I_D = 1 mA, V_{GS} = 0 V	620			V
I_{DSS}	Zero gate voltage drain current	V_{GS} = 0 V, V_{DS} = 620 V			0.8	µA
		V_{GS} = 0 V, V_{DS} = 620 V, T_C = 125 °C (1)			50	
I_{GSS}	Gate body leakage current	V_{DS} = 0 V, V_{GS} = ±20 V			±9	µA
$V_{GS(th)}$	Gate threshold voltage	V_{DS} = V_{GS}, I_D = 50 µA	3	3.75	4.5	V
$R_{DS(on)}$	Static drain-source on-resistance	V_{GS} = 10 V, I_D = 2.8 A		0.95	1.2	Ω

1. *Specified by design, not tested in production.*

Table 5. Dynamic

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
C_{iss}	Input capacitance	V_{DS} = 50 V, f = 1 MHz, V_{GS} = 0 V	-	875	-	pF
C_{oss}	Output capacitance		-	100	-	pF
C_{rss}	Reverse transfer capacitance		-	17	-	pF
$C_{oss(er)}$(1)	Equivalent output capacitance energy related	V_{DS} = 0 to 480 V, V_{GS} = 0 V	-	28	-	pF
$C_{oss(tr)}$(2)	Equivalent output capacitance time related		-	63	-	pF
R_G	Intrinsic gate resistance	f = 1 MHz open drain	-	3.5	-	Ω
Q_g	Total gate charge	V_{DD} = 496 V, I_D = 5.5 A, V_{GS} = 0 to 10 V (see Figure 15. Test circuit for gate charge behavior)	-	34	-	nC
Q_{gs}	Gate-source charge		-	4	-	nC
Q_{gd}	Gate-drain charge		-	22	-	nC

1. *$C_{oss(er)}$ is a constant capacitance value that gives the same stored energy as C_{oss} while V_{DS} is rising from 0 to 80% V_{DSS}.*
2. *$C_{oss(tr)}$ is a constant capacitance value that gives the same charging time as C_{oss} while V_{DS} is rising from 0 to 80% V_{DSS}.*

Table 6. Switching times

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
$t_{d(on)}$	Turn-on delay time	V_{DD} = 310 V, I_D = 2.75 A, R_G = 4.7 Ω, V_{GS} = 10 V (see Figure 14. Test circuit for resistive load switching times and Figure 19. Switching time waveform)	-	22	-	ns
t_r	Rise time		-	12	-	ns
$t_{d(off)}$	Turn-off delay time		-	49	-	ns
t_f	Fall time		-	20	-	ns

Table 7. Source-drain diode

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
I_{SD}	Source-drain current		-		5.5	A
I_{SDM} (1)	Source-drain current (pulsed)		-		27	A
V_{SD} (2)	Forward on voltage	I_{SD} = 5.5 A, V_{GS} = 0 V	-		1.5	V
t_{rr}	Reverse recovery time	I_{SD} = 5.5 A, di/dt = 100 A/µs	-	290		ns
Q_{rr}	Reverse recovery charge	V_{DD} = 60 V	-	1.9		µC
I_{RRM}	Reverse recovery current	(see Figure 16. Test circuit for inductive load switching and diode recovery times)	-	13.5		A
t_{rr}	Reverse recovery time	I_{SD} = 5.5 A, di/dt = 100 A/µs	-	335		ns
Q_{rr}	Reverse recovery charge	V_{DD} = 60 V, T_J = 150 °C	-	2.4		µC
I_{RRM}	Reverse recovery current	(see Figure 16. Test circuit for inductive load switching and diode recovery times)	-	14.5		A

1. *Pulse width limited by safe operating area.*
2. *Pulsed: pulse duration = 300 µs, duty cycle 1.5%.*

2.1 Electrical characteristics (curves)

Figure 1. Safe operating area

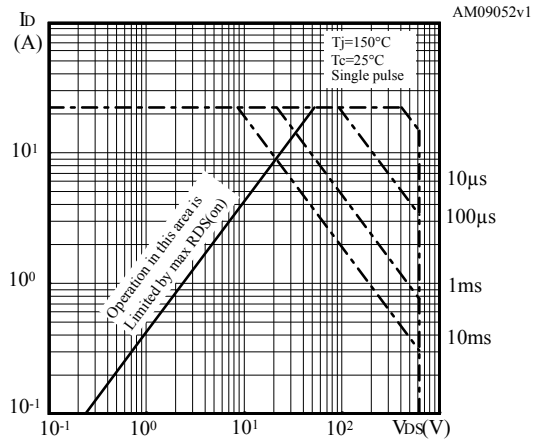


Figure 2. Normalized transient thermal impedance

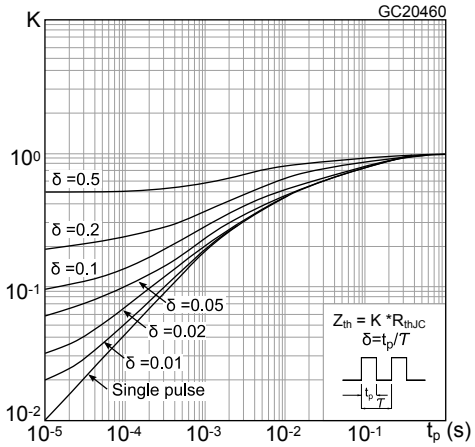


Figure 3. Typical output characteristics

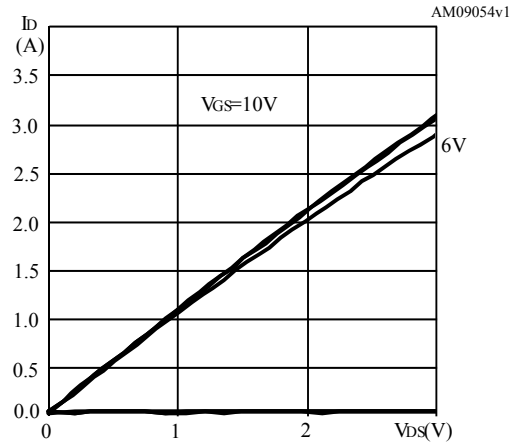


Figure 4. Typical transfer characteristics

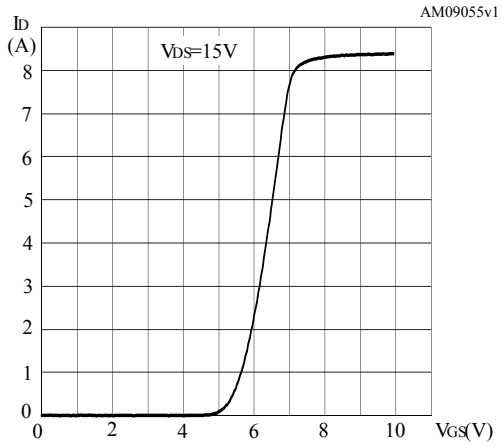


Figure 5. Typical gate charge characteristics

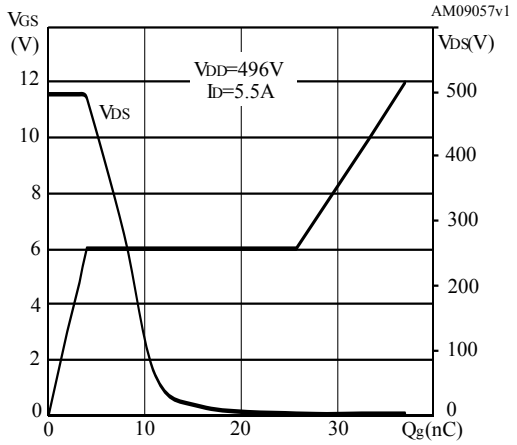


Figure 6. Typical capacitance characteristics

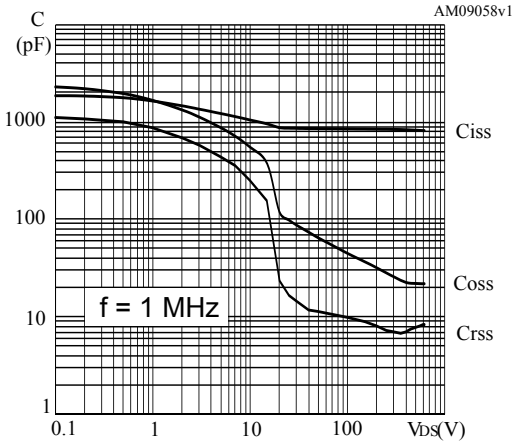


Figure 7. Normalized gate threshold vs temperature

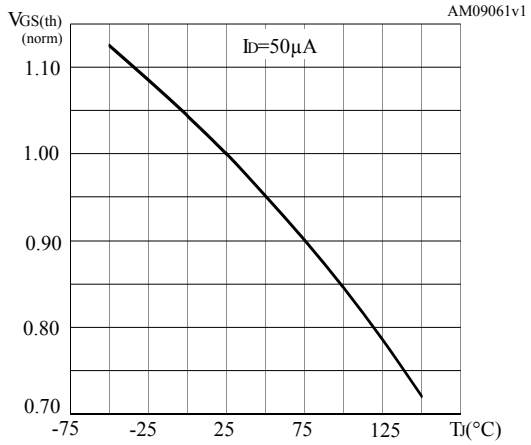


Figure 8. Normalized breakdown voltage vs temperature

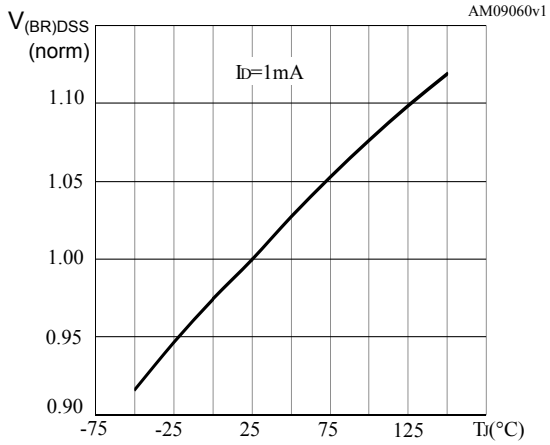


Figure 9. Typical drain-source on-resistance

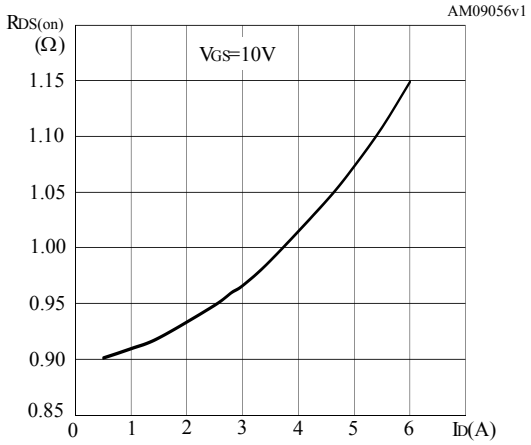


Figure 10. Normalized on-resistance vs temperature

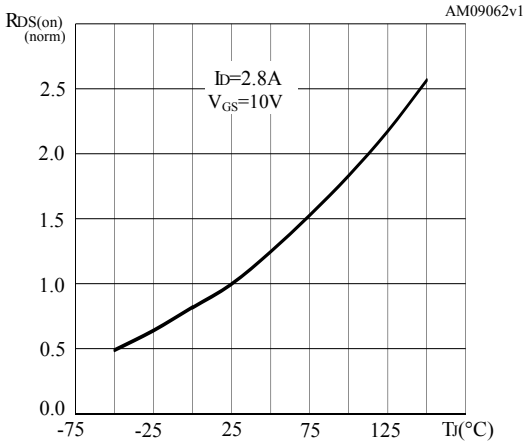


Figure 11. Typical output capacitance stored energy

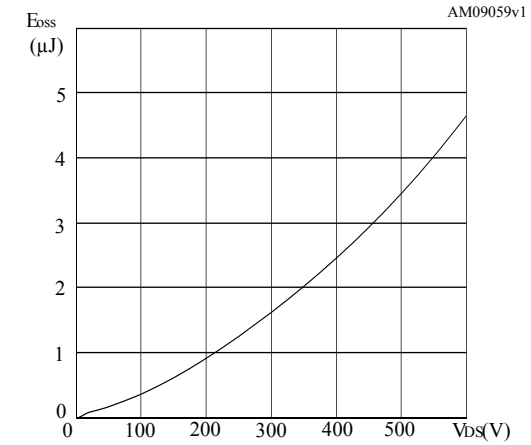


Figure 12. Typical reverse diode forward characteristics

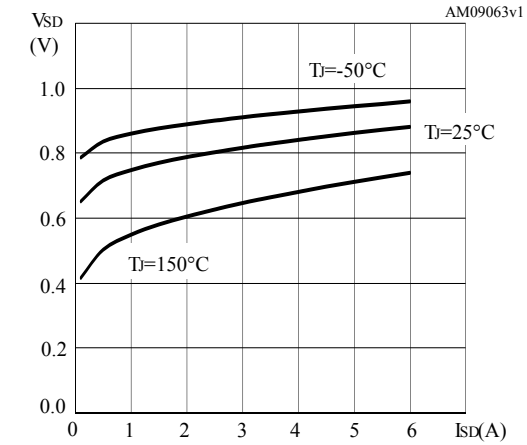
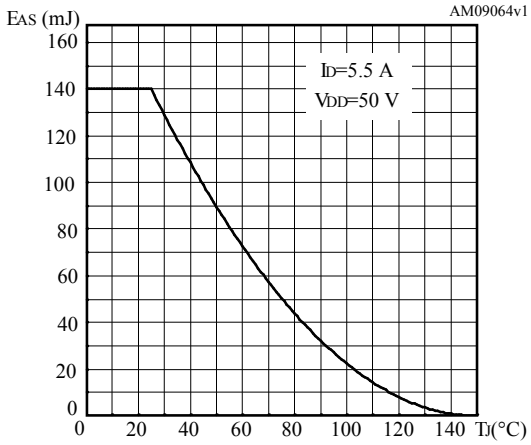


Figure 13. **Maximum avalanche energy vs temperature**



3 Test circuits

Figure 14. Test circuit for resistive load switching times

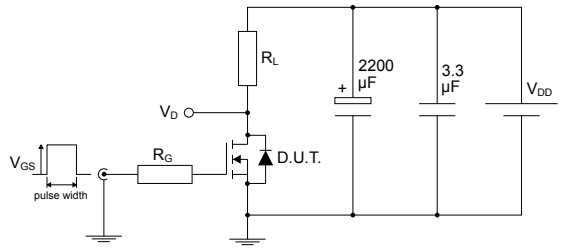


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Figure 15. Test circuit for gate charge behavior

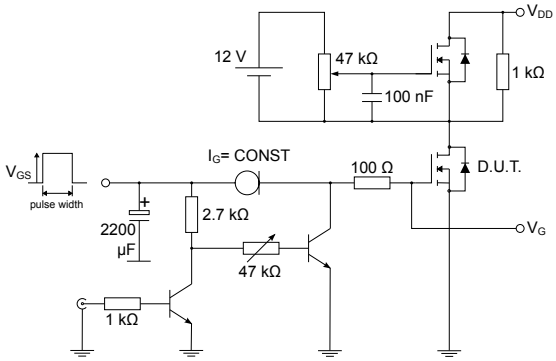

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Figure 16. Test circuit for inductive load switching and diode recovery times

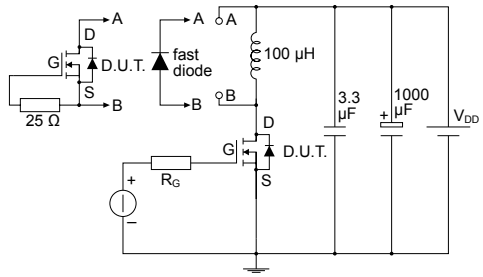

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Figure 17. Unclamped inductive load test circuit

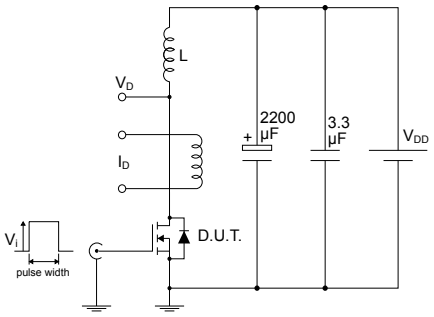

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Figure 18. Unclamped inductive waveform

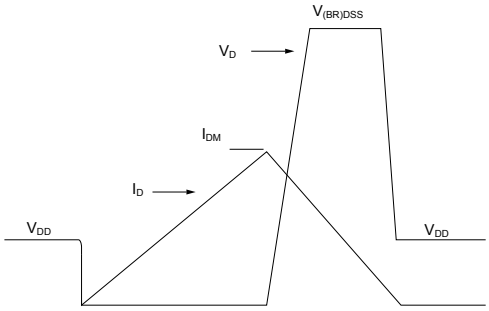

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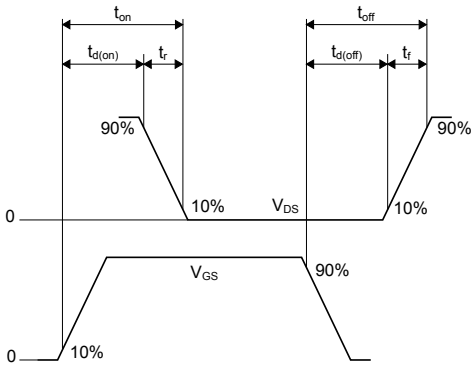
Figure 19. Switching time waveform



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4 Package information

In order to meet environmental requirements, ST offers these devices in different grades of ECOPACK packages, depending on their level of environmental compliance. ECOPACK specifications, grade definitions and product status are available at: www.st.com. ECOPACK is an ST trademark.

4.1 IPAK (TO-251) type E package information

Figure 20. IPAK (TO-251) type E package outline

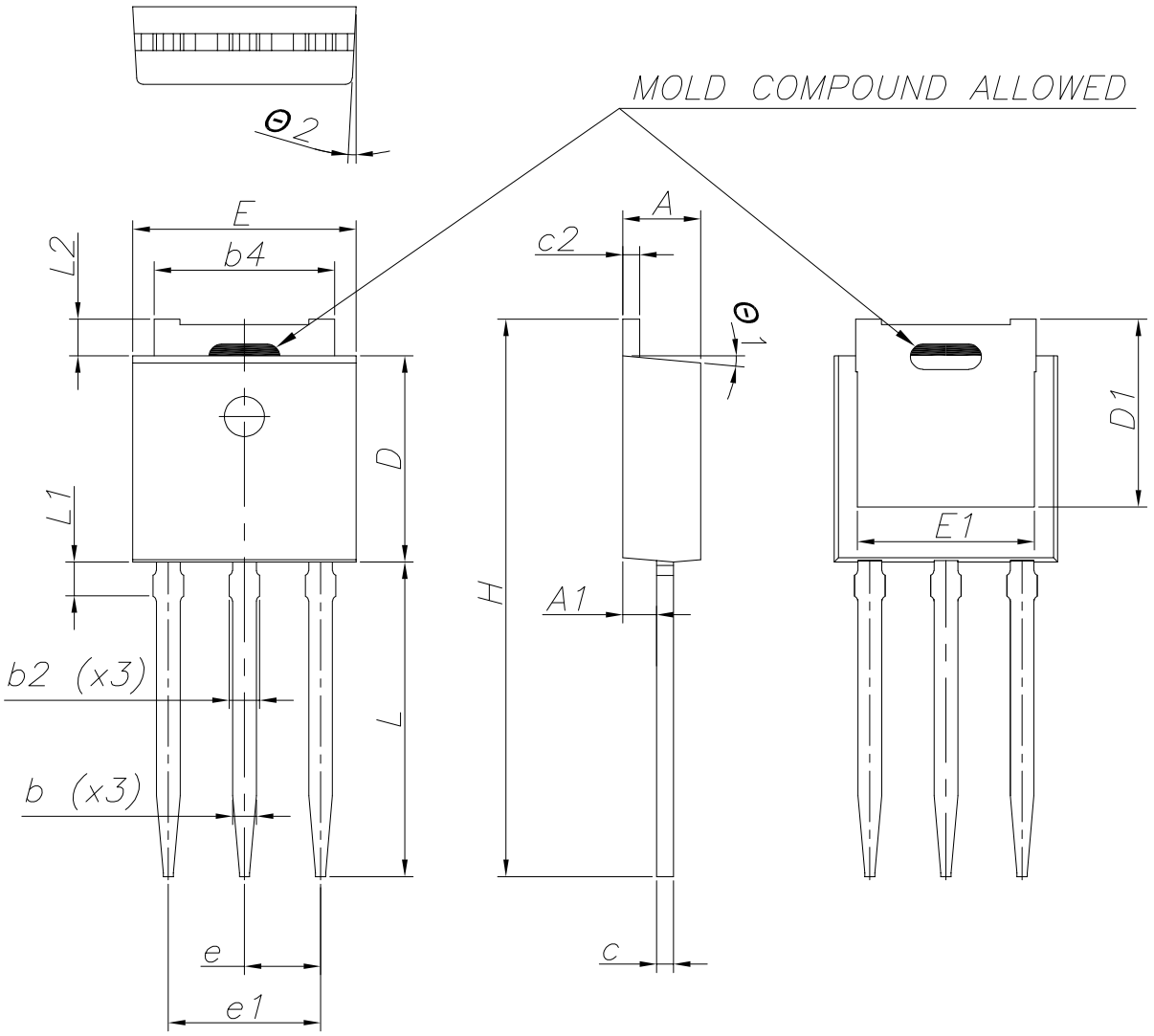

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Table 8. **IPAK (TO-251) type E package mechanical data**

Dim.	mm		
	Min.	Typ.	Max.
A	2.20	2.30	2.35
A1	0.90	1.00	1.10
b	0.66		0.79
b2			0.90
b4	5.23	5.33	5.43
c	0.46		0.59
c2	0.46		0.59
D	6.00	6.10	6.20
D1	5.30	5.53	5.75
E	6.50	6.60	6.70
E1	5.05	5.23	5.40
e	2.20	2.25	2.30
e1	4.40	4.50	4.60
H	16.18	16.48	16.78
L	9.00	9.30	9.60
L1	0.80	1.00	1.20
L2	0.90	1.08	1.25
Θ1	3°	5°	7°
Θ2	1°	3°	5°

Revision history

Table 9. **Document revision history**

Date	Revision	Changes
19-May-2006	1	First release.
02-May-2011	2	R_G value has been updated.
06-Dec-2011	3	Removed p/n STD6N62K3 in DPAK.
03-Aug-2012	4	Added package, mechanical data: I²PAKFP Updated *Table 1: Device summary*, *Table 2: Absolute maximum ratings*, *Table 3: Thermal data*, *Table 4: On /off states*, *Table 13: IPAK (TO-251) mechanical data* and *Figure 29: IPAK (TO-251) drawing* Minor text changes.
16-Oct-2023	5	The part numbers STF6N62K3, STFI6N62K3, STI6N62K3 and STP6N62K3 have been moved to separate datasheets and the document has been updated accordingly. Removed Gate-source Zener diode table. Updated Section 4 Package information. Minor text changes.

Contents