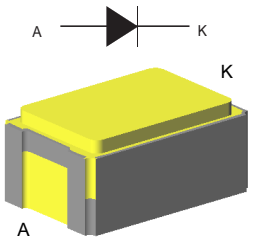
Aerospace 40 V, 3 A Schottky diode in LCC-2B package



Leadless chip carrier 2 (LCC-2B)

Features

- Low forward voltage drop: V_F = 0.485 V at 3 A and +25 °C
- Very small conduction losses
- Ultrafast switchings with negligible losses
- High thermal conductivity materials
- Surface mount hermetic package
- Radiation performance
  - 150 krad (Si) low dose rate
  - 3 Mrad (Si) high dose rate
- ESCC qualified: detail specification 5106/020

Product status link
1N5822U

Product summary	
$I_{F(AV)}$	3 A
V_{RRM}	40 V
V_F(max.)	0.485 V
T_J(max.)	150 °C

Applications

- Satellite and spacecraft power systems
- Switch mode power supply
- 5 V flyback or forward converter output rectification
- DC motor chopper free wheeling diode
- Reverse polarity protection
- Redundancy OR-Ing diode

Description

The 1N5822U Schottky diode is ESCC qualified. It is housed in a surface mount hermetically sealed ceramic LCC-2B package whose footprint is fully compatible with industry standard as D5B.

Its full planar technology allows superior performances and high reliability up to 150 °C junction temperature.

This diode is ESCC qualified, which makes it eligible for use in space programs. It is typically used in switching mode power supplies, high frequency DC-to-DC converters or low voltage step-down chopper drive to perform secondary rectification, redundancy OR-Ing, free wheeling diode or reverse polarity protection.

1 Characteristics

Table 1. Absolute ratings (limiting values)

Symbol	Parameter		Value	Unit
V_{RRM}	Repetitive peak reverse voltage		40	V
V_{RWM} (1)	Peak working reverse voltage		40	V
$I_{F(RMS)}$	RMS forward current		10	A
$I_{F(AV)}$	Average forward current	$T_C \geq 139$ °C, $\delta = 0.5$	3	A
I_{FSM}	Non repetitive surge forward current	t_p = 10 ms sinusoidal	80	A
T_{stg}	Storage temperature range		-65 to +150	°C
T_j	Maximum operating junction temperature(2)		150	°C
T_{sol}	Maximum soldering temperature(3)		245	°C
ESD	Electro static discharge, air discharge, HBM model, class 3B		8	kV

1. *See Figure 1.*
2. *$(dP_{tot}/dT_j) < (1/R_{th(j-a)})$ condition to avoid thermal runaway for a diode on its own heatsink.*
3. *Maximum duration 5 s. The same package cannot be re-soldered until 3 minutes have elapsed after initial soldering.*

Figure 1. V_{RRM} and V_{RWM} definition with their waveform

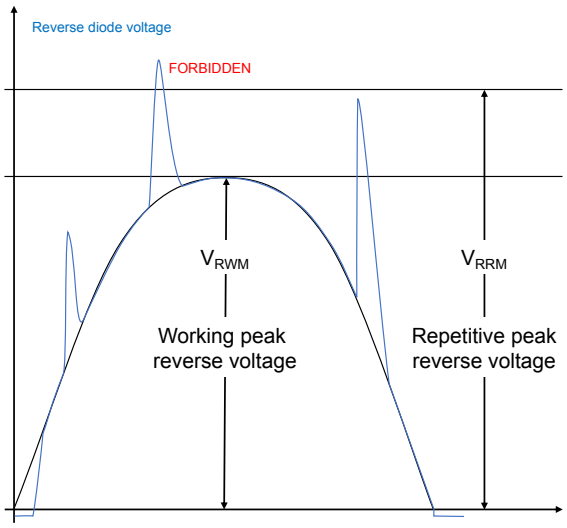


Table 2. Thermal parameters

Symbol	Parameter	Max. value	Unit
$R_{th(j-c)}$	Junction to case	7	°C/W

For more information, please refer to the application note:

- AN5088: Rectifiers thermal management, handling and mounting recommendation

Table 3. Static electrical characteristics

Symbol	Parameter	Test conditions		Min.	Typ.	Max.	Unit
I_R (1)	Reverse leakage current	T_j = -55 °C	V_R = 40 V	-	-	40	µA
		T_j = 25 °C		-	-	80	
		T_j = 100 °C		-	-	12	mA
V_F (2)	Forward voltage drop	T_j = 25 °C	I_F = 1 A	-	-	0.4	V
		T_j = -55 °C	I_F = 3 A			0.56	
		T_j = 25 °C		-	-	0.485	
		T_j = 100 °C		-	-	0.455	
		T_j = 25 °C	I_F = 9.4 A	-	-	0.70	

1. *Pulse test: t_p = 5 ms, δ < 2%*
2. *Pulse test: t_p = 680 µs, δ < 2%*

To evaluate the conduction losses, use the following equation:

$P = 0.32 \times I_{F(AV)} + 0.050 \times I_F{}^2{}_{(RMS)}$

For more information, please refer to the following application notes related to the power losses:

- AN604: Calculation of conduction losses in a power rectifier
- AN4021: Calculation of reverse losses on a power diode

Table 4. Dynamic characteristics

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
C_j	Total diode capacitance	V_R = 5 V, F = 1 MHz			240	pF

1.1 Characteristics (curves)

Figure 2. Average forward power dissipation versus average forward current

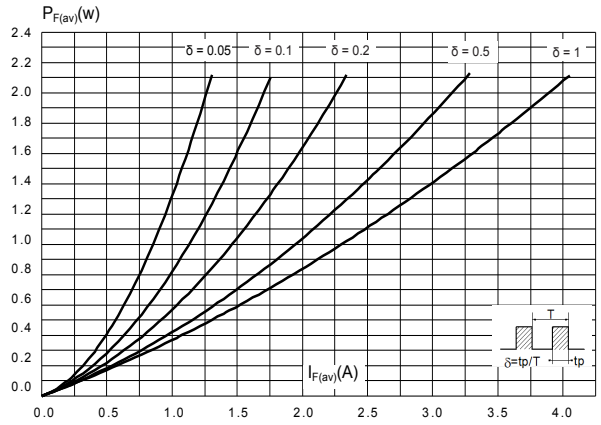


Figure 3. Average forward current versus ambient temperature (δ = 0.5)

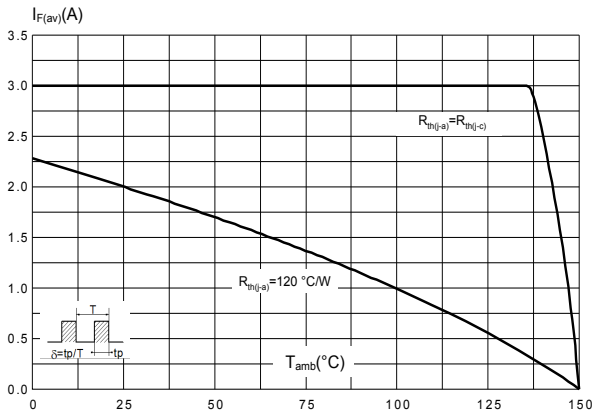


Figure 4. Non repetitive surge peak forward current versus total pulse burst duration (maximum values)

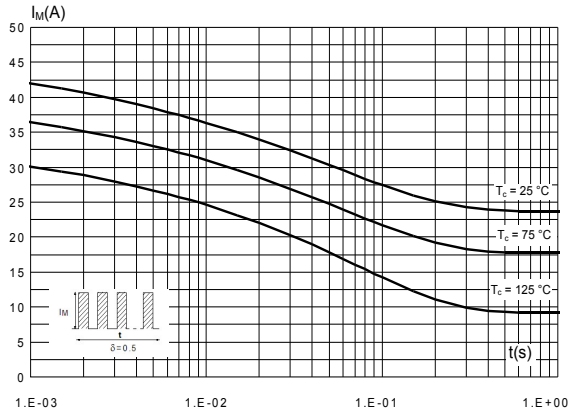


Figure 5. Relative variation of thermal impedance junction to case versus single square pulse duration

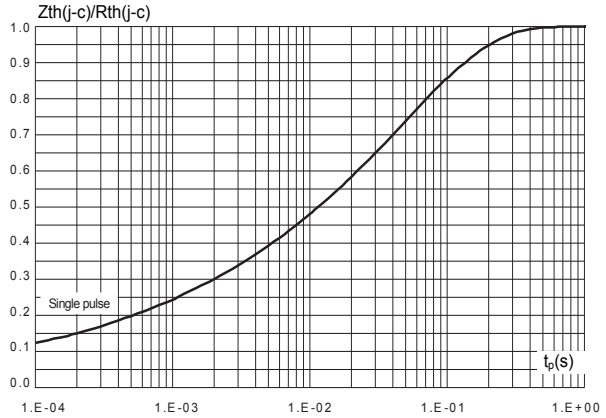


Figure 6. Reverse leakage current versus reverse voltage applied (typical values)

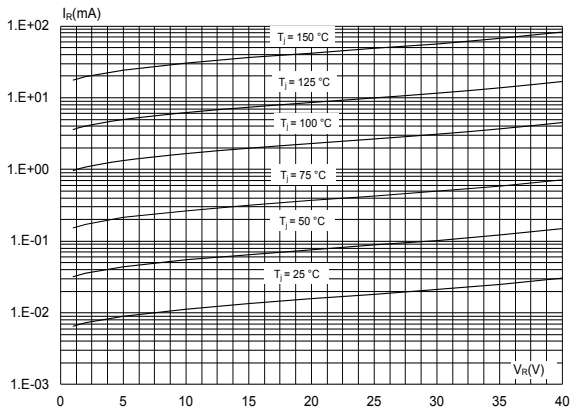


Figure 7. Forward voltage drop versus forward current (typical values)

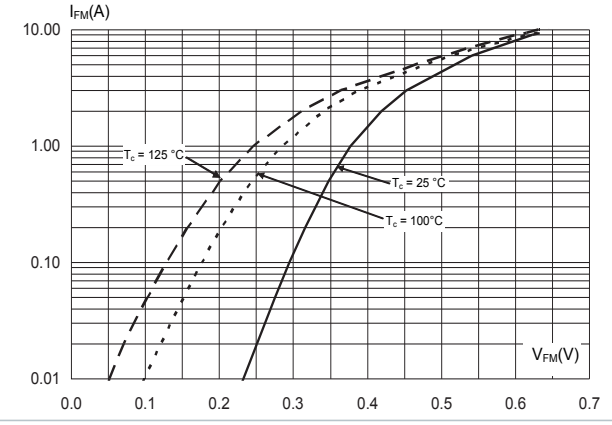
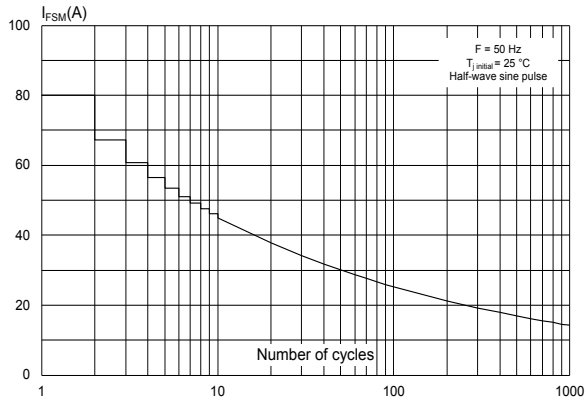


Figure 8. **Non repetitive surge peak forward current versus number of cycles**



2 Radiation

The technology of the STMicroelectronics Rad-Hard rectifier's diodes is intrinsically highly resistant to radiative environments. For further information refer the ECSS-Q-ST-60-15C1 radiation hardness assurance standard.

The product radiation hardness assurance is supported by a total ionisation dose (TID) characterization at high dose and low dose rates.

2.1 Total ionisation dose

A characterization at both high and low dose rates (HDR and LDR) is done on two sets of 15 samples housed in LCC-2B, 5 reverse biased, 5 forward biased and 5 unbiased.

The irradiation is done according to the ESCC 22900 specification, at 620krad/h for the high dose rate HDR test and at 0.220 krad/h for the low rate LDR test.

Both pre-irradiation and post-irradiation performances are tested using the same circuitry and the same test conditions for a direct comparison (T_{amb} = 22 ±3 °C unless otherwise specified).

The following parameters are measured:

- Before irradiation
- After irradiation (target 3 Mrad (Si) HDR or 150 krad(Si) LDR)
- After 24 hours at room temperature
- After 168 hours of annealing at 100 °C

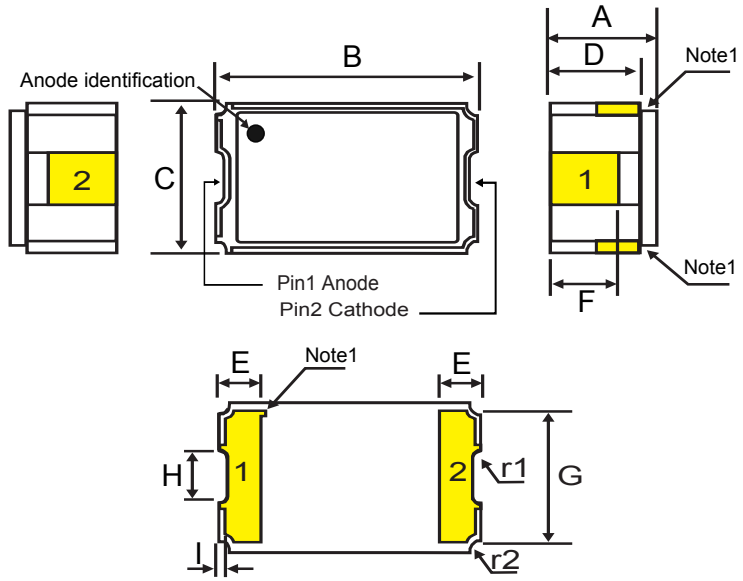
3 Package information

To meet environmental requirements, ST offers these devices in different grades of ECOPACK packages, depending on their level of environmental compliance. ECOPACK specifications, grade definitions, and product status are available at: www.st.com. ECOPACK is an ST trademark.

3.1 LCC-2B package information

The LCC-2B package is available with two lead tinning versions : Gold plated or SnPb 63/37 solder dip leads. Its metallic lid is electrically floating and not connected to any pin. Connecting it to ground doesn't affect the electrical characteristics.

Figure 9. LCC-2B package outline



Note 1: The anode is identified by metalization in two top internal angles and the index mark.

Table 5. LCC-2B package mechanical data

Ref.	Dimensions					
	Millimeters			Inches (for reference only)		
	Min.	Typ.	Max.	Min.	Typ.	Max.
A	2.04	2.23	2.42	0.080	0.088	0.095
B	5.27	5.40	5.60	0.207	0.213	0.220
C	3.49	3.62	3.76	0.137	0.143	0.150
D	1.71	1.90	2.09	0.067	0.075	0.082
E	0.48		0.71	0.019		0.028
F		1.4			0.055	
G		3.32			0.131	
H		1.82			0.072	
I		0.15			0.006	
r1		0.15			0.006	
r2		0.20			0.008	

Dimension data specified for the gold plated version and the solder dip version before tinning.

4 Ordering information

Table 6. Ordering information

Order code	ESCC detail specification	Quality level	Package	Lead finishing	Product marking	Mass	Base qty.	Packing
1N5822UB1	-	Engineering model	LCC-2B	Gold	1N5822UB1	180 mg	50	Wafle pack
1N5822U01B	5106/020/01	Flight model		Gold	510602001			
1N5822U02B	5106/020/02	Flight model		Solder dip	510602002			

Note: Contact ST sales office for information about the specific conditions for products in die form.

5 Other information

5.1 Product marking description

Here below is described the marking of the package of both the engineering and flight models.

Figure 10. ESCC flight model marking outline

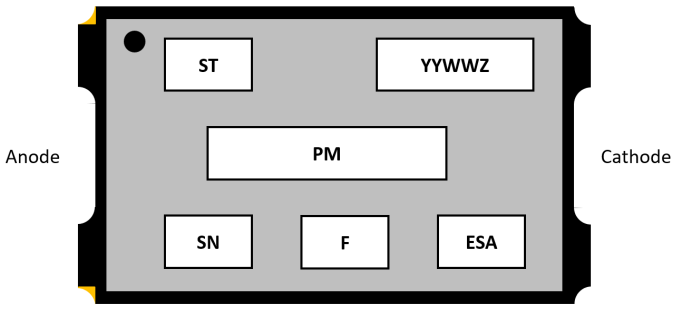


Table 7. ESCC flight model marking

Field	Description
ST	ST logo
YYWWZ	Date code and lot index in the week(1)
PM	Product marking
SN	Serialization number
F	Country of origin
ESA	ESA logo

1. *YY = two-digit year, WW = two-digit week, Z = lot week index.*

Figure 11. Engineering model marking outline

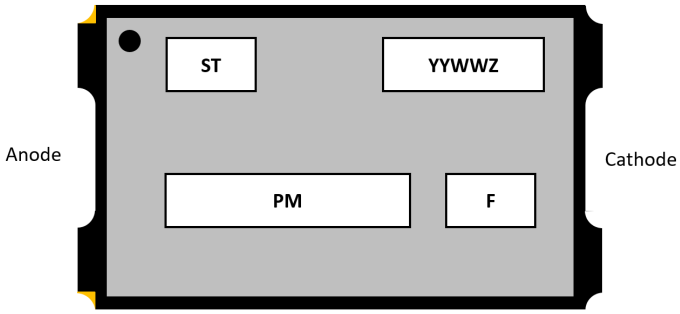


Table 8. Engineering model marking

Field	Description
ST	ST logo
YYWWZ	Date code and lot index in the week(1)
PM	Product marking
F	Country of origin

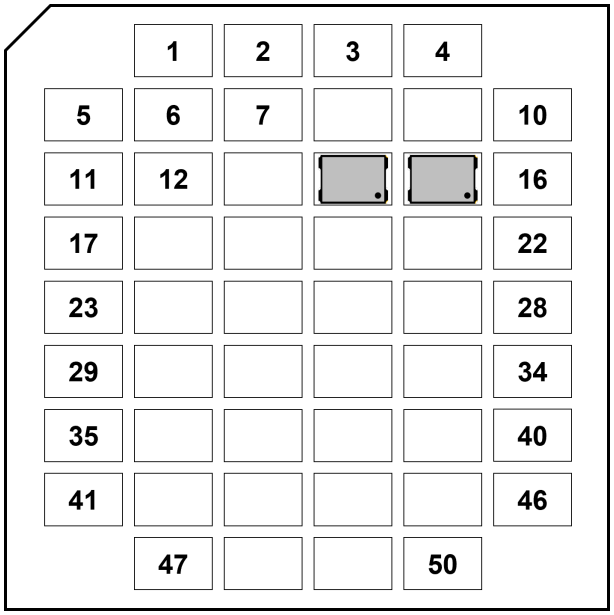
1. *YY = two-digit year, WW = two-digit week, Z = lot week index.*

5.2 Packing information

The 1N5822U versions are delivered in a 50-position, 50 x 50 mm² waffle pack consecutively populated from position 1.

The Figure 12 shows how to identify position 1, the orientation of the product in the waffle pack.

Figure 12. 1N5822 waffle pack outline



The diode anode is on the right pin of the device, and the anode identification dot is orientated at the opposite of the waffle pack truncated corner.

5.3 Documentation

In the Table 9 is a summary of the documentation provided with each type of products.

Table 9. Documentation provided for each type of product

Quality level	Documentation
Engineering model	Certificate of conformance including : • Customer name • Customer purchase order number • ST sales order number and item • ST commercial product code • Quantity delivered • Date code • Reference data sheet • Reference to TN1181 on engineering models • ST Rennes assembly lot ID
Flight model	Certificate of conformance including : • Customer name • Customer purchase order number • ST sales order number and item • ST commercial product code • Quantity delivered • Date code • Serial numbers • Wafer diffusion plant location and wafer size • Wafer diffusion lot ID number and wafer ID number • Reference of the applicable ESCC qualification maintenance lot • Reference to the ESCC detail specification • ST Rennes assembly lot ID number

Revision history

Table 10. **Document revision history**

Date	Revision	Changes
10-Aug-2009	1	First issue.
25-Sep-2011	2	Updated ESCC status in Features and added footnote to Table 3.
8-Nov-2013	3	Updated Table 1, Table 2, Table 5 and Table 7 and inserted Other information.
08-Dec-2015	4	Updated Table 7 and reformatted to current standard.
21-Mar-2023	5	Updated *features*, *description*, and *Section 5 Other information*. Added application and *Section 5.2 Packing information*. Minor text changes.
30-Oct-2023	6	Updated *Table 6*. Minor text changes.
23-Nov-2023	7	Updated *Features*.
14-Nov-2024	8	Updated Figure 9.

Contents