N-channel 600 V, 800 mΩ typ., 5 A MDmesh II Power MOSFET in an IPAK package

IPAK

AM01475v1_noZen

Features
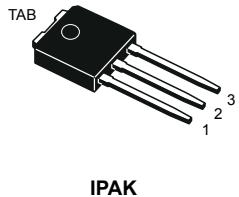
Order code	V_{DS}	$R_{DS(on)}$ max.	I_D
STU7NM60N	600 V	900 mΩ	5 A

- 100% avalanche tested
- Low input capacitance and gate charge
- Low gate input resistance

Applications

- Switching applications

Description

This device is an N-channel Power MOSFET developed using the second generation of MDmesh technology. This revolutionary Power MOSFET associates a vertical structure to the company's strip layout to yield one of the world's lowest on-resistance and gate charge. It is therefore suitable for the most demanding high efficiency converters.
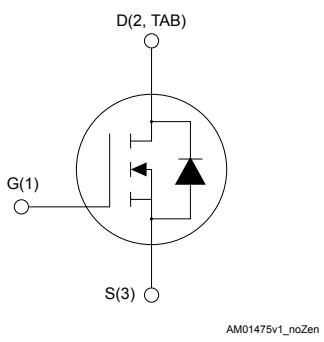
Product status link
STU7NM60N

Product summary	
Order code	STU7NM60N
Marking	7NM60N
Package	IPAK
Packing	Tube

DS6523 - Rev 6 - October 2023
For further information contact your local STMicroelectronics sales office.

www.st.com

1 Electrical ratings

Table 1. Absolute maximum ratings

Symbol	Parameter	Value	Unit
V_{DS}	Drain-source voltage	600	V
V_{GS}	Gate-source voltage	±25	V
I_D	Drain current (continuous) at T_C = 25 °C	5	A
	Drain current (continuous) at T_C = 100 °C	3	
I_{DM}[1]	Drain current pulsed	20	A
P_{TOT}	Total power dissipation at T_C = 25 °C	45	W
dv/dt[2]	Peak diode recovery voltage slope	15	V/ns
T_J	Operating junction temperature range	-55 to 150	°C
T_{stg}	Storage temperature range		

1. *Pulse width limited by safe operating area.*

2. *$I_{SD} \leq 5$ A, di/dt ≤ 100 A/μs, V_{DS} (peak) $\leq V_{(BR)DSS}$, $V_{DD} = 80\% V_{(BR)DSS}$.*

Table 2. Thermal data

Symbol	Parameter	Value	Unit
R_{thJC}	Thermal resistance, junction-to-case	2.78	°C/W
R_{thJA}	Thermal resistance, junction-to-ambient	100	°C/W

Table 3. Avalanche characteristics

Symbol	Parameter	Value	Unit
I_{AR}	Avalanche current, repetitive or not repetitive (pulse width limited by T_J max.)	2	A
E_{AS}	Single-pulse avalanche energy (starting T_J = 25 °C, I_D = I_{AR}, V_{DD} = 50 V)	119	mJ

2 Electrical characteristics

T_C = 25 °C unless otherwise specified.

Table 4. On/off states

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
$V_{(BR)DSS}$	Drain-source breakdown voltage	I_D = 1 mA, V_{GS} = 0 V	600			V
I_{DSS}	Zero gate voltage drain current	V_{GS} = 0 V, V_{DS} = 600 V			1	µA
		V_{GS} = 0 V, V_{DS} = 600 V, T_C = 125 °C[1]			100	
I_{GSS}	Gate body leakage current	V_{DS} = 0 V, V_{GS} = ±20 V			100	nA
$V_{GS(th)}$	Gate threshold voltage	V_{DS} = V_{GS}, I_D = 250 µA	2	3	4	V
$R_{DS(on)}$	Static drain-source on resistance	V_{GS} = 10 V, I_D = 2.5 A		800	900	mΩ

1. *Specified by design, not tested in production.*

Table 5. Dynamic

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
C_{iss}	Input capacitance	V_{DS} = 50 V, f = 1 MHz, V_{GS} = 0 V	-	363	-	pF
C_{oss}	Output capacitance		-	24.6	-	pF
C_{rss}	Reverse transfer capacitance		-	1.1	-	pF
$C_{oss\ eq.}$ [1]	Equivalent capacitance time related	V_{DS} = 0 to 480 V, V_{GS} = 0 V	-	130	-	pF
R_G	Intrinsic gate resistance	f = 1 MHz open drain	-	5.4	-	Ω
Q_g	Total gate charge	V_{DD} = 480 V, I_D = 5 A, V_{GS} = 0 to 10 V (see Figure 12. Test circuit for gate charge behavior)	-	14	-	nC
Q_{gs}	Gate-source charge		-	2.7	-	nC
Q_{gd}	Gate-drain charge		-	7.7	-	nC

1. *$C_{oss\ eq.}$ is defined as a constant equivalent capacitance giving the same charging time as C_{oss} when V_{DS} increases from 0 to 80% V_{DSS}.*

Table 6. Switching times

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
$t_{d(on)}$	Turn-on delay time	V_{DD} = 300 V, I_D = 2.5 A,	-	7	-	ns
t_r	Rise time	R_G = 4.7 Ω, V_{GS} = 10 V	-	10	-	ns
$t_{d(off)}$	Turn-off delay time	(see Figure 11. Test circuit for resistive load switching times and	-	26	-	ns
t_f	Fall time	Figure 16. Switching time waveform)	-	12	-	ns

Table 7. Source drain diode

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
I_{SD}	Source-drain current		-		5	A
I_{SDM}[1]	Source-drain current (pulsed)		-		20	A
V_{SD}[2]	Forward on voltage	I_{SD} = 5 A, V_{GS} = 0 V	-		1.3	V
t_{rr}	Reverse recovery time	I_{SD} = 5 A, di/dt = 100 A/µs,	-	213		ns
Q_{rr}	Reverse recovery charge	V_{DD} = 60 V	-	1.5		µC
I_{RRM}	Reverse recovery current	(see Figure 13. Test circuit for inductive load switching and diode recovery times)	-	14		A
t_{rr}	Reverse recovery time	I_{SD} = 5 A, di/dt = 100 A/µs,	-	265		ns
Q_{rr}	Reverse recovery charge	V_{DD} = 60 V, T_J = 150 °C	-	1.8		µC
I_{RRM}	Reverse recovery current	(see Figure 13. Test circuit for inductive load switching and diode recovery times)	-	14		A

1. *Pulse width limited by safe operating area.*

2. *Pulsed: pulse duration = 300 µs, duty cycle 1.5%.*

2.1 Electrical characteristics (curves)

Figure 1. Safe operating area
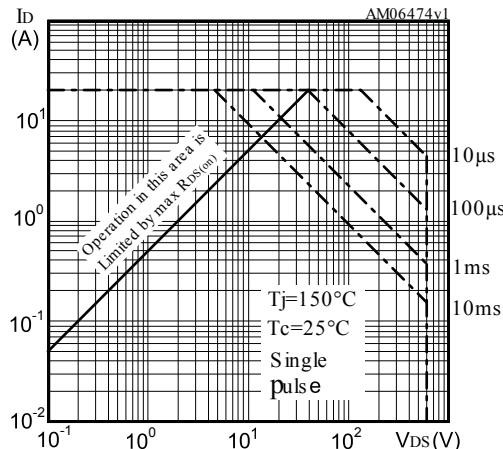
Figure 2. Thermal impedance
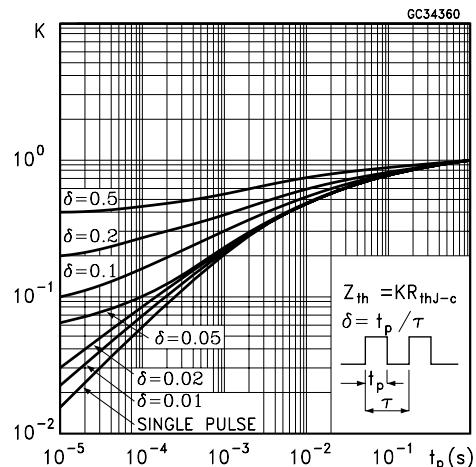
**Figure 3. Output characterisics**
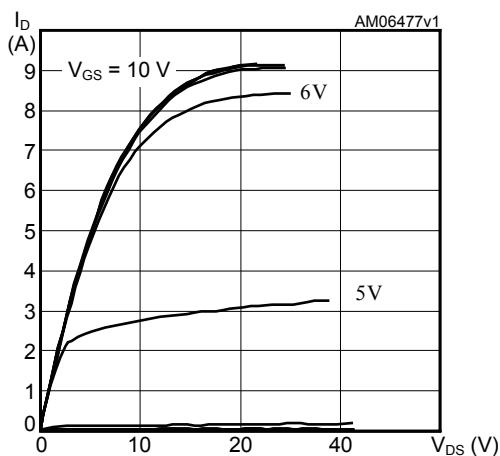

Figure 4. Transfer characteristics
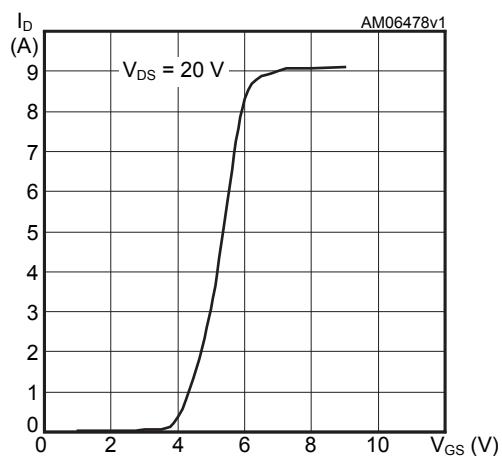
**Figure 5. Gate charge vs gate-source voltage**
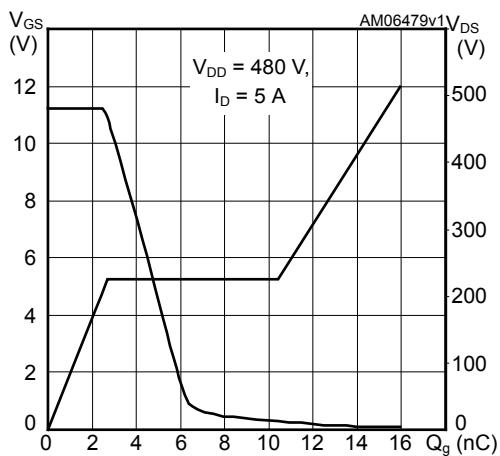

**Figure 6. Static drain-source on-resistance**
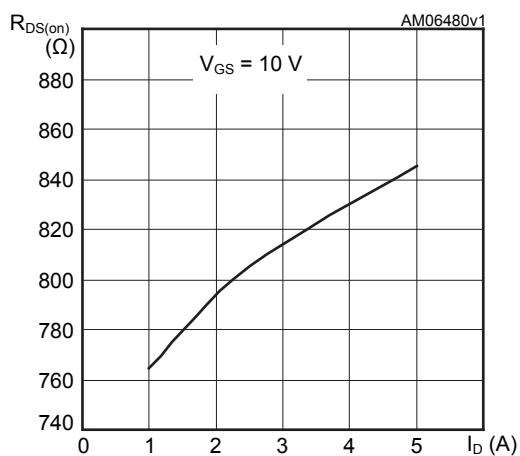
Figure 7. Capacitance variations
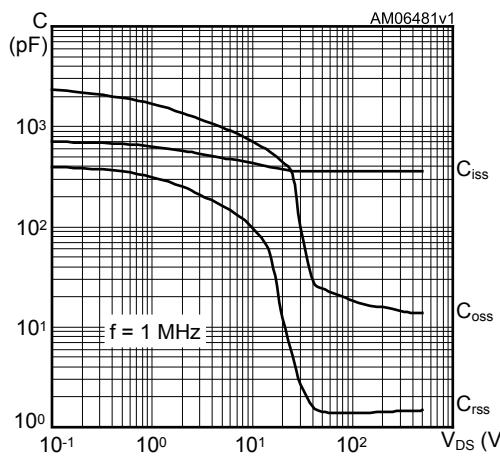
Figure 8. Normalized gate threshold voltage vs temperature
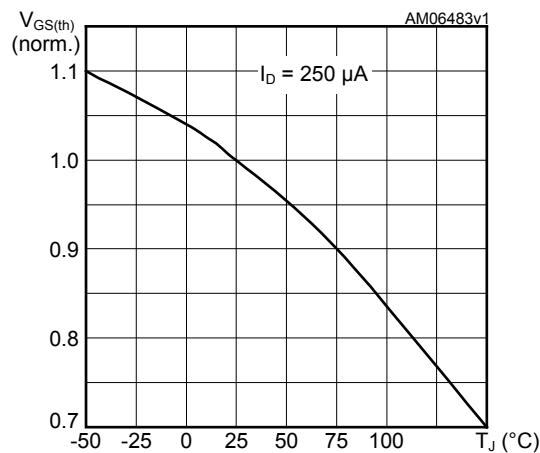

Figure 9. Normalized on-resistance vs temperature
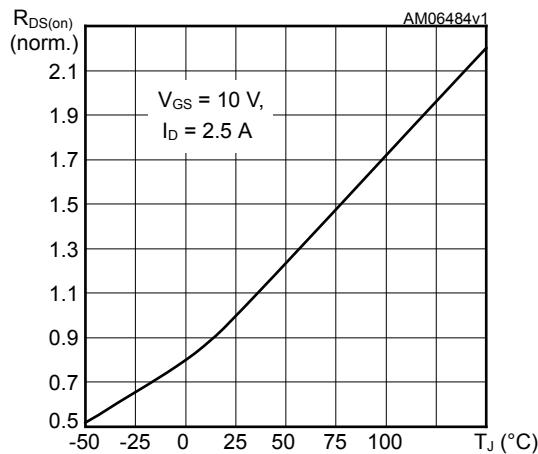
Figure 10. Normalized V$_{(BR)DSS}$ vs temperature
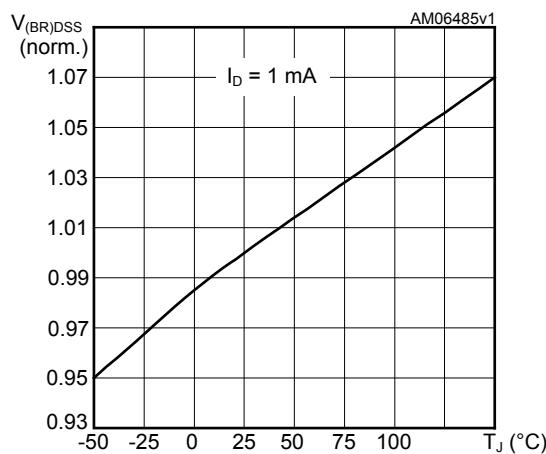
3 Test circuits

Figure 11. Test circuit for resistive load switching times
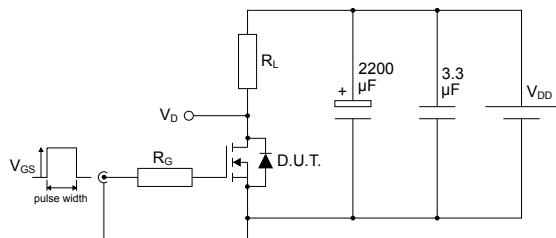
AM01468v1

Figure 12. Test circuit for gate charge behavior
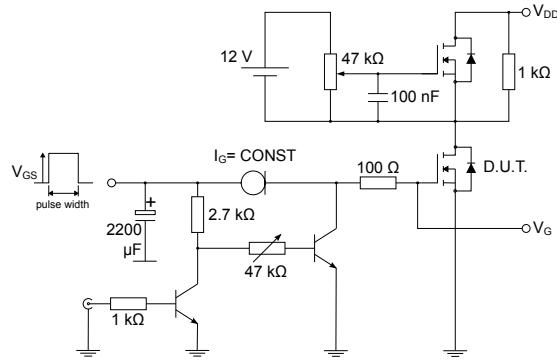
AM01469v1

Figure 13. Test circuit for inductive load switching and diode recovery times
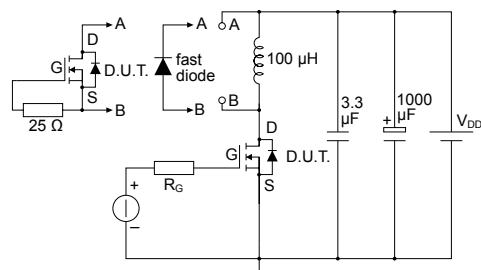
AM01470v1

Figure 14. Unclamped inductive load test circuit

AM01471v1

Figure 15. Unclamped inductive waveform
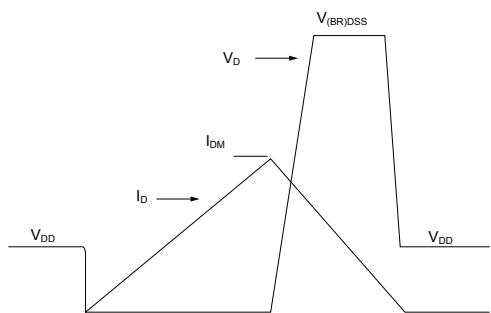

AM01472v1

Figure 16. Switching time waveform
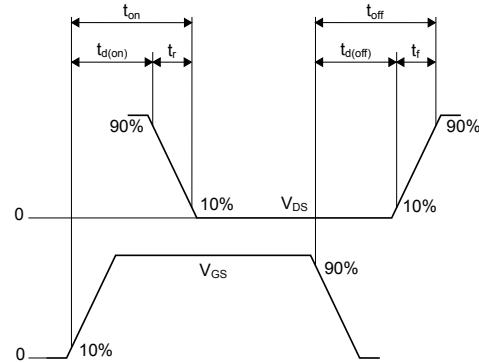
AM01473v1

4 Package information

In order to meet environmental requirements, ST offers these devices in different grades of ECOPACK packages, depending on their level of environmental compliance. ECOPACK specifications, grade definitions and product status are available at: www.st.com. ECOPACK is an ST trademark.

4.1 IPAK (TO-251) type C package information

Figure 17. IPAK (TO-251) type C package outline
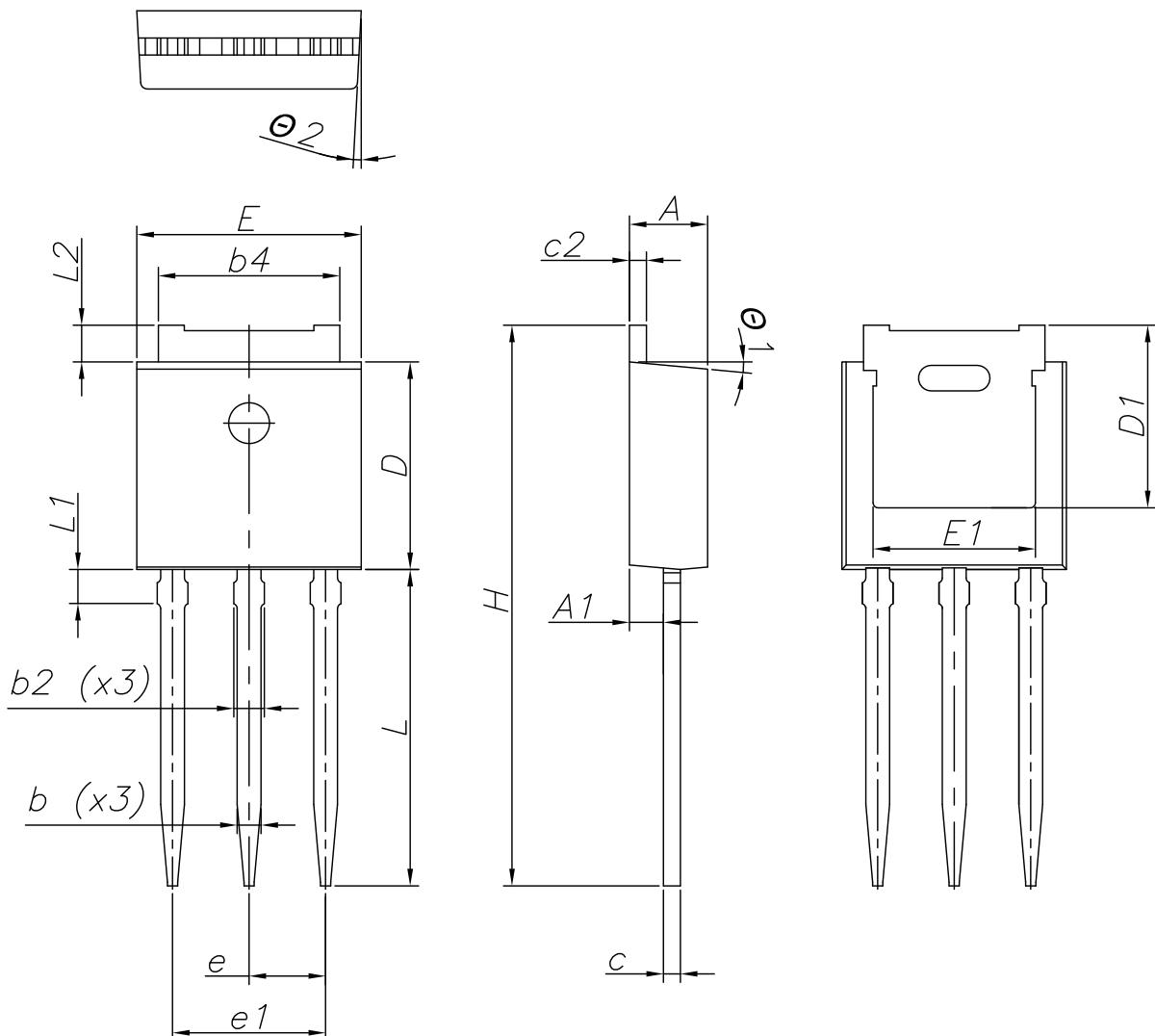
0068771_IK_typeC_rev16

Table 8. **IPAK (TO-251) type C package mechanical data**

Dim.	mm		
	Min.	Typ.	Max.
A	2.20	2.30	2.35
A1	0.90	1.00	1.10
b	0.66		0.79
b2			0.90
b4	5.23	5.33	5.43
c	0.46		0.59
c2	0.46		0.59
D	6.00	6.10	6.20
D1	5.20	5.37	5.55
E	6.50	6.60	6.70
E1	4.60	4.78	4.95
e	2.20	2.25	2.30
e1	4.40	4.50	4.60
H	16.18	16.48	16.78
L	9.00	9.30	9.60
L1	0.80	1.00	1.20
L2	0.90	1.08	1.25
θ1	3°	5°	7°
θ2	1°	3°	5°

Revision history

Table 9. Document revision history

Date	Revision	Changes
29-Oct-2009	1	First release.
19-Jul-2010	2	Corrected values in Table 3: Thermal data.
11-Oct-2010	3	Inserted new value in Table 6: Dynamic
04-Nov-2010	4	Changed $R_{DS(on)}$ typical value.
05-Sep-2018	5	The part number STP7NM60N has been moved to a separate datasheet. Removed maturity status indication from cover page. The document status is production data. Updated title and features in cover page. Updated *Section 1 Electrical ratings*, *Section 2 Electrical characteristics* and *Section 4 Package information*. Minor text changes.
16-Oct-2023	6	The part numbers STD7NM60N and STF7NM60N have been moved to a separate datasheet and the document has been updated accordingly. Removed "*Section 4.6 IPAK (TO-251) type A package information*" and updated Section 4.1 IPAK (TO-251) type C package information. Minor text changes.

Contents

IMPORTANT NOTICE – READ CAREFULLY