

Important notice

Dear Customer,

On 7 February 2017 the former NXP Standard Product business became a new company with the tradename **Nexperia**. Nexperia is an industry leading supplier of Discrete, Logic and PowerMOS semiconductors with its focus on the automotive, industrial, computing, consumer and wearable application markets

In data sheets and application notes which still contain NXP or Philips Semiconductors references, use the references to Nexperia, as shown below.

Instead of http://www.nxp.com, http://www.nxp.com, http://www.nexperia.com, http://www.nexperia.com,

Instead of sales.addresses@www.nxp.com or sales.addresses@www.semiconductors.philips.com, use salesaddresses@nexperia.com (email)

Replace the copyright notice at the bottom of each page or elsewhere in the document, depending on the version, as shown below:

- © NXP N.V. (year). All rights reserved or © Koninklijke Philips Electronics N.V. (year). All rights reserved

Should be replaced with:

- © Nexperia B.V. (year). All rights reserved.

If you have any questions related to the data sheet, please contact our nearest sales office via e-mail or telephone (details via **salesaddresses@nexperia.com**). Thank you for your cooperation and understanding,

Kind regards,

Team Nexperia



40 V, 1 A PNP low V_{CEsat} BISS transistor Rev. 04 — 29 July 2008

Product data sheet

Product profile

1.1 General description

PNP low V_{CEsat} Breakthrough In Small Signal (BISS) transistor in a SOT23 (TO-236AB) small Surface-Mounted Device (SMD) plastic package.

NPN complement: PBSS4140T.

1.2 Features

- Low collector-emitter saturation voltage V_{CEsat}
- High collector current capability I_C and I_{CM}
- High collector current gain (h_{FE}) at high I_C
- High efficiency due to less heat generation

1.3 Applications

- General-purpose switching and muting
- LCD backlighting
- Supply line switching circuits
- Battery-driven equipment (mobile phones, video cameras and handheld devices)

1.4 Quick reference data

Table 1. Quick reference data

Symbol	Parameter	Conditions	Min	Тур	Max	Unit
V_{CEO}	collector-emitter voltage	open base	-	-	-40	V
I_{C}	collector current		-	-	–1	Α
I _{CM}	peak collector current	single pulse; $t_p \le 1 \text{ ms}$	-	-	-2	Α
R _{CEsat}	collector-emitter saturation resistance	$I_C = -500 \text{ mA};$ $I_B = -50 \text{ mA}$	<u>[1]</u> _	300	< 500	mΩ

[1] Pulse test: $t_p \le 300 \ \mu s$; $\delta \le 0.02$.



PBSS5140T NXP Semiconductors

40 V, 1 A PNP low V_{CEsat} BISS transistor

Pinning information 2.

Table 2 Pinning

Table 2.	i iiiiiiig		
Pin	Description	Simplified outline	Graphic symbol
1	base		
2	emitter	<u> 3</u>	3
3	collector	1 2	1—
			006aab259

Ordering information 3.

Table 3. **Ordering information**

Type number	Package	Package			
	Name	Description	Version		
PBSS5140T	-	plastic surface-mounted package; 3 leads	SOT23		

Marking 4.

Table 4. **Marking codes**

Type number	Marking code ^[1]
PBSS5140T	*2H

[1] * = -: made in Hong Kong

* = p: made in Hong Kong

* = t: made in Malaysia

* = W: made in China

Limiting values 5.

Table 5. **Limiting values**

In accordance with the Absolute Maximum Rating System (IEC 60134).

Symbol	Parameter	Conditions	Min	Max	Unit
V_{CBO}	collector-base voltage	open emitter	-	-40	V
V_{CEO}	collector-emitter voltage	open base	-	-40	V
V_{EBO}	emitter-base voltage	open collector	-	-5	V
I_{C}	collector current		-	-1	Α
I _{CM}	peak collector current	single pulse; $t_p \le 1 \text{ ms}$	-	-2	Α
I _{BM}	peak base current	single pulse; $t_p \le 1 \text{ ms}$	-	-1	Α

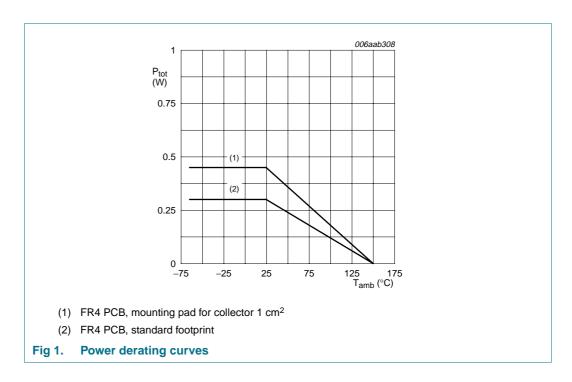
40 V, 1 A PNP low V_{CEsat} BISS transistor

Table 5. Limiting values ...continued
In accordance with the Absolute Maximum Rating System (IEC 60134).

Symbol	Parameter	Conditions	Min	Max	Unit
P_{tot}	total power dissipation	$T_{amb} \le 25 ^{\circ}C$			
			<u>[1]</u> _	300	mW
			[2] _	450	mW
Tj	junction temperature		-	150	°C
T _{amb}	ambient temperature		-65	+150	°C
T _{stg}	storage temperature		-65	+150	°C

^[1] Device mounted on an FR4 Printed-Circuit Board (PCB), single-sided copper, tin-plated and standard footprint.

^[2] Device mounted on an FR4 PCB, single-sided copper, tin-plated, mounting pad for collector 1 cm².



6. Thermal characteristics

Table 6. Thermal characteristics

Symbol	Parameter	Conditions	Min	Тур	Max	Unit
$R_{th(j-a)}$		in free air				
junction to ambient	junction to ambient		<u>[1]</u> _	-	417	K/W
			[2] _	-	278	K/W

^[1] Device mounted on an FR4 PCB, single-sided copper, tin-plated and standard footprint.

^[2] Device mounted on an FR4 PCB, single-sided copper, tin-plated, mounting pad for collector 1 cm².

40 V, 1 A PNP low V_{CEsat} BISS transistor

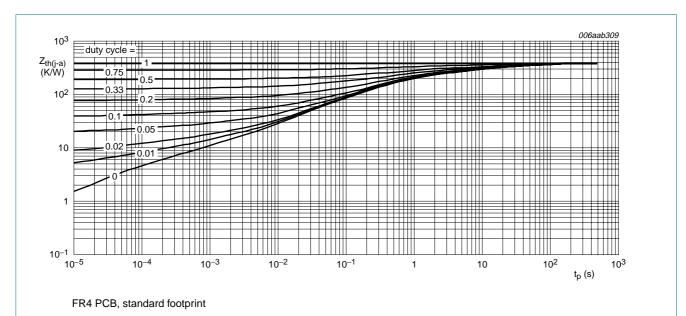


Fig 2. Transient thermal impedance from junction to ambient as a function of pulse duration; typical values

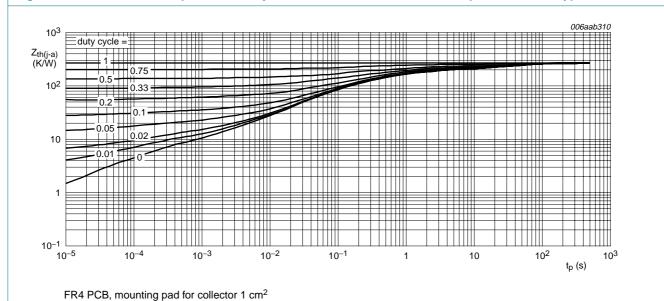


Fig 3. Transient thermal impedance from junction to ambient as a function of pulse duration; typical values

40 V, 1 A PNP low V_{CEsat} BISS transistor

7. Characteristics

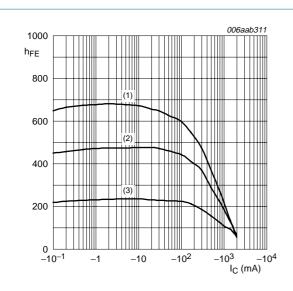
Table 7. Characteristics

 $T_{amb} = 25 \,^{\circ}C$ unless otherwise specified.

•						
Parameter	Conditions		Min	Тур	Max	Unit
collector-base cut-off	$V_{CB} = -40 \text{ V}; I_E = 0 \text{ A}$		-	-	-100	nA
current	$V_{CB} = -40 \text{ V}; I_E = 0 \text{ A};$ $T_j = 150 ^{\circ}\text{C}$		-	-	-50	μΑ
collector-emitter cut-off current	$V_{CE} = -30 \text{ V}; I_{B} = 0 \text{ A}$		-	-	-100	nA
emitter-base cut-off current	$V_{EB} = -5 \text{ V}; I_C = 0 \text{ A}$		-	-	-100	nA
DC current gain	$V_{CE} = -5 \text{ V}; I_{C} = -1 \text{ mA}$		300	-	-	
	$V_{CE} = -5 \text{ V}; I_{C} = -100 \text{ mA}$		300	-	800	
	$V_{CE} = -5 \text{ V}; I_{C} = -500 \text{ mA}$	[1]	250	-	-	
	$V_{CE} = -5 \text{ V}; I_{C} = -1 \text{ A}$	[1]	160	-	-	
collector-emitter	$I_C = -100 \text{ mA}; I_B = -1 \text{ mA}$		-	-	-200	mV
saturation voltage	$I_C = -500 \text{ mA}; I_B = -50 \text{ mA}$	[1]	-	-	-250	mV
	$I_C = -1 A$; $I_B = -100 \text{ mA}$	[1]	-	-	-500	mV
collector-emitter saturation resistance	$I_C = -500 \text{ mA}; I_B = -50 \text{ mA}$	[1]	-	300	< 500	mΩ
base-emitter saturation voltage	$I_C = -1 \text{ A}; I_B = -50 \text{ mA}$	<u>[1]</u>	-	-	-1.1	V
base-emitter turn-on voltage	$V_{CE} = -5 \text{ V}; I_C = -1 \text{ A}$		-	-	-1	V
delay time	$V_{CC} = -10 \text{ V}; I_C = -0.5 \text{ A};$		-	10	-	ns
rise time			-	31	-	ns
turn-on time	180II — 20 IIIA		-	41	-	ns
storage time			-	195	-	ns
fall time			-	65	-	ns
turn-off time			-	260	-	ns
transition frequency	$V_{CE} = -10 \text{ V}; I_{C} = -50 \text{ mA};$		150	-	-	MHz
transition frequency	f = 100 MHz					
	collector-base cut-off current collector-emitter cut-off current emitter-base cut-off current DC current gain collector-emitter saturation voltage collector-emitter saturation resistance base-emitter saturation voltage base-emitter turn-on voltage delay time rise time turn-on time storage time fall time turn-off time	$ \begin{array}{llllllllllllllllllllllllllllllllllll$	$ \begin{array}{llllllllllllllllllllllllllllllllllll$	$ \begin{array}{c} \text{collector-base cut-off} \\ \text{current} \\ \end{array} \begin{array}{c} V_{CB} = -40 \ \text{V}; \ I_E = 0 \ \text{A}; \\ V_{CB} = -40 \ \text{V}; \ I_E = 0 \ \text{A}; \\ T_j = 150 \ ^{\circ}\text{C} \\ \end{array} \begin{array}{c} - \\ \end{array} \\ \begin{array}{c} \text{collector-emitter} \\ \text{cut-off current} \\ \end{array} \begin{array}{c} V_{CE} = -30 \ \text{V}; \ I_B = 0 \ \text{A} \\ \end{array} \begin{array}{c} - \\ \end{array} \\ \end{array} \\ \begin{array}{c} \text{collector-emitter} \\ \text{cut-off current} \\ \end{array} \begin{array}{c} V_{CE} = -30 \ \text{V}; \ I_C = 0 \ \text{A} \\ \end{array} \begin{array}{c} - \\ \end{array} \\ \end{array} \\ \begin{array}{c} \text{collector-emitter} \\ \text{current} \\ \end{array} \begin{array}{c} V_{CE} = -5 \ \text{V}; \ I_C = -1 \ \text{mA} \\ \end{array} \begin{array}{c} 300 \\ \text{300} \\ \end{array} \\ \begin{array}{c} V_{CE} = -5 \ \text{V}; \ I_C = -100 \ \text{mA} \\ \end{array} \begin{array}{c} 300 \\ V_{CE} = -5 \ \text{V}; \ I_C = -100 \ \text{mA} \\ \end{array} \begin{array}{c} 10 \\ \text{250} \\ \end{array} \\ \begin{array}{c} V_{CE} = -5 \ \text{V}; \ I_C = -100 \ \text{mA} \\ \end{array} \begin{array}{c} 11 \\ \text{160} \\ \end{array} \\ \begin{array}{c} I_C = -100 \ \text{mA}; \ I_B = -100 \ \text{mA} \\ \end{array} \begin{array}{c} I_C = -100 \ \text{mA}; \ I_B = -50 \ \text{mA} \\ \end{array} \begin{array}{c} I_C = -100 \ \text{mA}; \ I_B = -50 \ \text{mA} \\ \end{array} \begin{array}{c} I_C = -100 \ \text{mA}; \ I_B = -50 \ \text{mA} \\ \end{array} \begin{array}{c} I_C = -100 \ \text{mA}; \ I_B = -50 \ \text{mA} \\ \end{array} \begin{array}{c} I_C = -100 \ \text{mA}; \ I_B = -50 \ \text{mA} \\ \end{array} \begin{array}{c} I_C = -100 \ \text{mA}; \ I_B = -50 \ \text{mA} \\ \end{array} \begin{array}{c} I_C = -100 \ \text{mA}; \ I_B = -50 \ \text{mA} \\ \end{array} \begin{array}{c} I_C = -100 \ \text{mA}; \ I_B = -50 \ \text{mA} \\ \end{array} \begin{array}{c} I_C = -100 \ \text{mA}; \ I_B = -50 \ \text{mA} \\ \end{array} \begin{array}{c} I_C = -100 \ \text{mA}; \ I_B = -50 \ \text{mA} \\ \end{array} \begin{array}{c} I_C = -100 \ \text{mA}; \ I_B = -50 \ \text{mA} \\ \end{array} \begin{array}{c} I_C = -100 \ \text{mA}; \ I_B = -50 \ \text{mA} \\ \end{array} \begin{array}{c} I_C = -100 \ \text{mA}; \ I_B = -50 \ \text{mA} \\ \end{array} \begin{array}{c} I_C = -100 \ \text{mA}; \ I_B = -50 \ \text{mA} \\ \end{array} \begin{array}{c} I_C = -100 \ \text{mA}; \ I_B = -50 \ \text{mA}; \ I_B = -50 \ \text{mA}; \\ I_B = -50 \ \text{mA}; \ I_B = -50 \ \text{mA}; \\ I_B = -50 \ \text{mA}; \ I_B = -50 \ \text{mA}; \\ I_B = -50 \ \text{mA}; \ I_B = -50 \ \text{mA}; \\ I_B = -50 \ $		

^[1] Pulse test: $t_p \le 300~\mu s;~\delta \le 0.02.$

40 V, 1 A PNP low V_{CEsat} BISS transistor



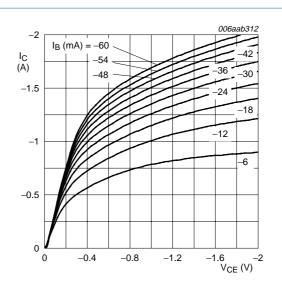
$$V_{CE} = -5 \text{ V}$$

(1)
$$T_{amb} = 100 \, ^{\circ}C$$

(2)
$$T_{amb} = 25 \, ^{\circ}C$$

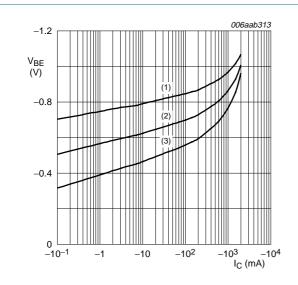
(3) $T_{amb} = -55 \, ^{\circ}C$

Fig 4. DC current gain as a function of collector current; typical values



 $T_{amb} = 25 \, ^{\circ}C$

Fig 5. Collector current as a function of collector-emitter voltage; typical values



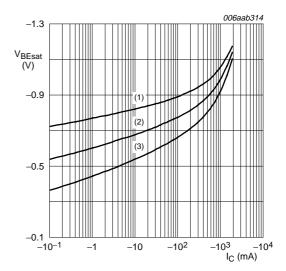


(1) $T_{amb} = -55 \, ^{\circ}C$

(2) $T_{amb} = 25 \, ^{\circ}C$

(3) $T_{amb} = 100 \, ^{\circ}C$

Fig 6. Base-emitter voltage as a function of collector current; typical values



 $I_{\rm C}/I_{\rm B} = 20$

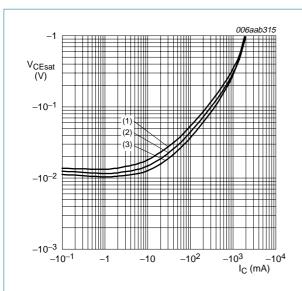
(1) $T_{amb} = -55 \, ^{\circ}C$

(2) $T_{amb} = 25 \, ^{\circ}C$

(3) $T_{amb} = 100 \, ^{\circ}C$

Fig 7. Base-emitter saturation voltage as a function of collector current; typical values

40 V, 1 A PNP low V_{CEsat} BISS transistor



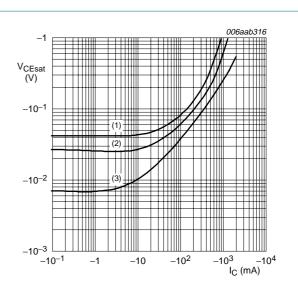
$$I_{\rm C}/I_{\rm B} = 20$$

(1)
$$T_{amb} = 100 \, ^{\circ}C$$

(2)
$$T_{amb} = 25 \, ^{\circ}C$$

(3)
$$T_{amb} = -55 \, ^{\circ}C$$

Fig 8. Collector-emitter saturation voltage as a function of collector current; typical values



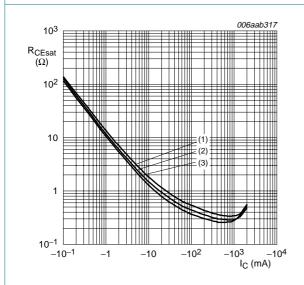
$$T_{amb} = 25 \, ^{\circ}C$$

(1)
$$I_C/I_B = 100$$

(2)
$$I_C/I_B = 50$$

(3)
$$I_C/I_B = 10$$

Fig 9. Collector-emitter saturation voltage as a function of collector current; typical values



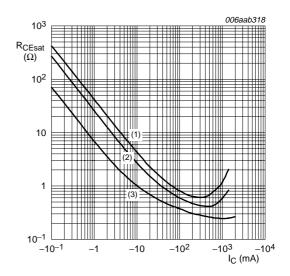


(1)
$$T_{amb} = 100 \, ^{\circ}C$$

(2)
$$T_{amb} = 25 \, ^{\circ}C$$

(3)
$$T_{amb} = -55 \,^{\circ}C$$

Fig 10. Collector-emitter saturation resistance as a function of collector current; typical values



(1)
$$I_C/I_B = 100$$

(2)
$$I_C/I_B = 50$$

(3)
$$I_C/I_B = 10$$

Fig 11. Collector-emitter saturation resistance as a function of collector current; typical values

40 V, 1 A PNP low V_{CEsat} BISS transistor

8. Test information

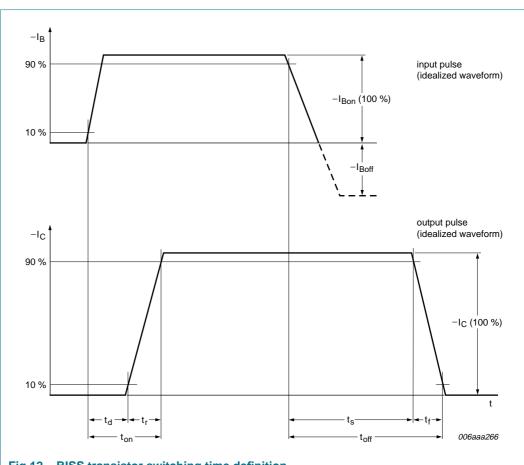
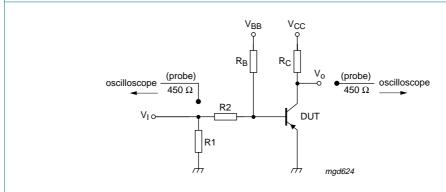


Fig 12. BISS transistor switching time definition

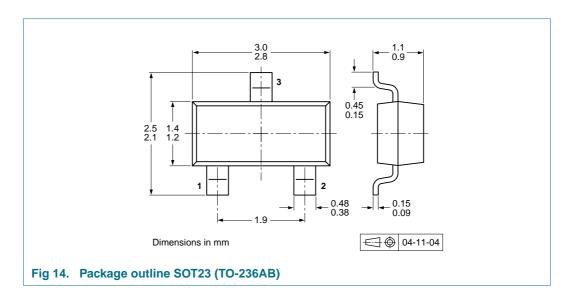


 $V_{CC} = -10 \text{ V}; I_C = -0.5 \text{ A}; I_{Bon} = -25 \text{ mA}; I_{Boff} = 25 \text{ mA}$

Fig 13. Test circuit for switching times

40 V, 1 A PNP low V_{CEsat} BISS transistor

9. Package outline



10. Packing information

Table 8. Packing methods

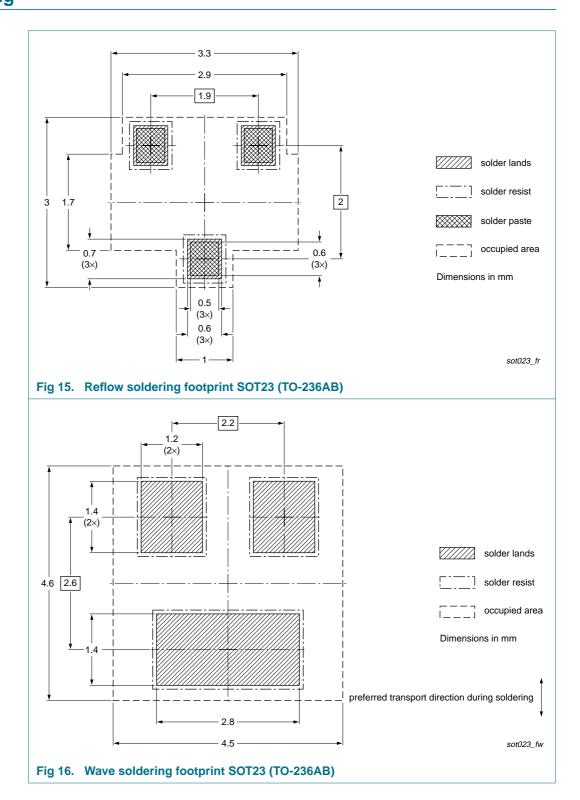
The indicated -xxx are the last three digits of the 12NC ordering code.[1]

Type number	Package	Description	Packing quantity	
			3000	10000
PBSS5140T	SOT23	4 mm pitch, 8 mm tape and reel	-215	-235

^[1] For further information and the availability of packing methods, see Section 14.

40 V, 1 A PNP low V_{CEsat} BISS transistor

11. Soldering



40 V, 1 A PNP low V_{CEsat} BISS transistor

12. Revision history

Table 9. Revision history

	,				
Document ID	Release date	Data sheet status	Change notice	Supersedes	
PBSS5140T_4	20080729	Product data sheet	-	PBSS5140T_3	
Modifications:		f this data sheet has been NXP Semiconductors.	redesigned to comply v	vith the new identity	
	 Legal texts h 	ave been adapted to the n	ew company name whe	re appropriate.	
	 Table 4 "Mar 	king codes": marking code	corrected		
	 Table 5 "Limi 	ting values": conditions ad	ded for I _{CM} and I _{BM}		
	• Figure 1, 2 and 3: added				
	 <u>Table 7</u>: R_{CEsat} redefined to collector-emitter saturation resistance 				
	• Figure 4, 6, 8	and 10: updated			
	• Figure 5, 7, 9	and <u>11</u> : added			
	 Section 8 "Test information": added 				
	• <u>Figure 14</u> : su	uperseded by minimized pa	ackage outline drawing		
	Section 11 "S	Soldering": added			
	 Section 13 "I 	<u>_egal information"</u> : updated	t		
PBSS5140T_3	20040107	Product specification	-	PBSS5140T_2	
PBSS5140T_2	20010720	Product specification	-	PBSS5140T_1	
PBSS5140T_1	20001116	Product specification	-	-	

40 V, 1 A PNP low V_{CEsat} BISS transistor

13. Legal information

13.1 Data sheet status

Document status[1][2]	Product status[3]	Definition
Objective [short] data sheet	Development	This document contains data from the objective specification for product development.
Preliminary [short] data sheet	Qualification	This document contains data from the preliminary specification.
Product [short] data sheet	Production	This document contains the product specification.

- [1] Please consult the most recently issued document before initiating or completing a design.
- [2] The term 'short data sheet' is explained in section "Definitions"
- [3] The product status of device(s) described in this document may have changed since this document was published and may differ in case of multiple devices. The latest product status information is available on the Internet at URL http://www.nxp.com.

13.2 Definitions

Draft — The document is a draft version only. The content is still under internal review and subject to formal approval, which may result in modifications or additions. NXP Semiconductors does not give any representations or warranties as to the accuracy or completeness of information included herein and shall have no liability for the consequences of use of such information.

Short data sheet — A short data sheet is an extract from a full data sheet with the same product type number(s) and title. A short data sheet is intended for quick reference only and should not be relied upon to contain detailed and full information. For detailed and full information see the relevant full data sheet, which is available on request via the local NXP Semiconductors sales office. In case of any inconsistency or conflict with the short data sheet, the full data sheet shall prevail.

13.3 Disclaimers

General — Information in this document is believed to be accurate and reliable. However, NXP Semiconductors does not give any representations or warranties, expressed or implied, as to the accuracy or completeness of such information and shall have no liability for the consequences of use of such information.

Right to make changes — NXP Semiconductors reserves the right to make changes to information published in this document, including without limitation specifications and product descriptions, at any time and without notice. This document supersedes and replaces all information supplied prior to the publication hereof.

Suitability for use — NXP Semiconductors products are not designed, authorized or warranted to be suitable for use in medical, military, aircraft, space or life support equipment, nor in applications where failure or malfunction of an NXP Semiconductors product can reasonably be expected to result in personal injury, death or severe property or environmental

damage. NXP Semiconductors accepts no liability for inclusion and/or use of NXP Semiconductors products in such equipment or applications and therefore such inclusion and/or use is at the customer's own risk.

Applications — Applications that are described herein for any of these products are for illustrative purposes only. NXP Semiconductors makes no representation or warranty that such applications will be suitable for the specified use without further testing or modification.

Limiting values — Stress above one or more limiting values (as defined in the Absolute Maximum Ratings System of IEC 60134) may cause permanent damage to the device. Limiting values are stress ratings only and operation of the device at these or any other conditions above those given in the Characteristics sections of this document is not implied. Exposure to limiting values for extended periods may affect device reliability.

Terms and conditions of sale — NXP Semiconductors products are sold subject to the general terms and conditions of commercial sale, as published at http://www.nxp.com/profile/terms, including those pertaining to warranty, intellectual property rights infringement and limitation of liability, unless explicitly otherwise agreed to in writing by NXP Semiconductors. In case of any inconsistency or conflict between information in this document and such terms and conditions, the latter will prevail.

No offer to sell or license — Nothing in this document may be interpreted or construed as an offer to sell products that is open for acceptance or the grant, conveyance or implication of any license under any copyrights, patents or other industrial or intellectual property rights.

Quick reference data — The Quick reference data is an extract of the product data given in the Limiting values and Characteristics sections of this document, and as such is not complete, exhaustive or legally binding.

13.4 Trademarks

Notice: All referenced brands, product names, service names and trademarks are the property of their respective owners.

14. Contact information

For more information, please visit: http://www.nxp.com

For sales office addresses, please send an email to: salesaddresses@nxp.com

PBSS5140T_4 © NXP B.V. 2008. All rights reserved.

PBSS5140T NXP Semiconductors

40 V, 1 A PNP low V_{CEsat} BISS transistor

15. Contents

1	Product profile
1.1	General description
1.2	Features
1.3	Applications
1.4	Quick reference data
2	Pinning information 2
3	Ordering information 2
4	Marking 2
5	Limiting values 2
6	Thermal characteristics 3
7	Characteristics 5
8	Test information 8
9	Package outline 9
10	Packing information 9
11	Soldering 10
12	Revision history
13	Legal information12
13.1	Data sheet status
13.2	Definitions
13.3	Disclaimers
13.4	Trademarks12
14	Contact information 12
15	Contents 13

Please be aware that important notices concerning this document and the product(s) described herein, have been included in section 'Legal information'.



© NXP B.V. 2008. All rights reserved.