Silicon Carbide (SiC) Schottky Diode – EliteSiC, 20 A, 650 V, D2, Power88

FFSM2065B

Silicon Carbide (SiC) Schottky Diodes use a completely new technology that provides superior switching performance and higher reliability compared to Silicon. No reverse recovery current, temperature independent switching characteristics, and excellent thermal performance sets Silicon Carbide as the next generation of power semiconductor. System benefits include highest efficiency, faster operating frequency, increased power density, reduced EMI, and reduced system size and cost.

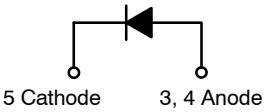
Features

- Max Junction Temperature 175°C
- Avalanche Rated 94 mJ
- High Surge Current Capacity
- Positive Temperature Coefficient
- Ease of Paralleling
- No Reverse Recovery/No Forward Recovery
- These Devices are Pb−Free, Halogen Free/BFR Free and are RoHS Compliant

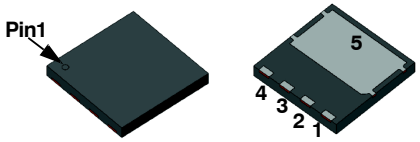
Applications

- General Purpose
- SMPS, Solar Inverter, UPS
- Power Switching Circuit

V_{RRM}	I_F
650 V	20 A



Schottky Diode



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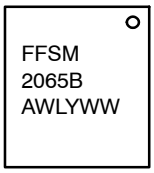
(Power88)
CASE 483AP

MARKING DIAGRAM



FFSM2065B	= Specific Device Code
A	= Assembly Site
WL	= Wafer Lot Number
Y	= Year
WW	= Work Week

ORDERING INFORMATION

See detailed ordering and shipping information in the package dimensions section on page 2 of this data sheet.

ABSOLUTE MAXIMUM RATINGS

(T_C = 25°C, Unless otherwise specified)

Symbol	Parameter		Value	Unit
V_{RRM}	Peak Repetitive Reverse Voltage		650	V
E_{AS}	Single Pulse Avalanche Energy (Note 1)		94	mJ
I_F	Continuous Rectified Forward Current @ T_C < 143°C		20	A
	Continuous Rectified Forward Current @ T_C < 135°C		23.4	
$I_{F, Max}$	Non−Repetitive Peak Forward Surge Current	T_C = 25°C, 10 μs	630	A
		T_C = 150°C, 10 μs	524	
$I_{F, SM}$	Non−Repetitive Forward Surge Current	Half−Sine Pulse, t_p = 8.3 ms T_C = 25°C	77	A
P_{tot}	Power Dissipation	T_C = 25°C	160	W
		T_C = 150°C	27	
T_J, T_{STG}	Operating and Storage Temperature Range		−55 to +175	°C

Stresses exceeding those listed in the Maximum Ratings table may damage the device. If any of these limits are exceeded, device functionality should not be assumed, damage may occur and reliability may be affected.

1. E_{AS} of 94 mJ is based on starting T_J = 25°C, L = 0.5 mH, I_{AS} = 19.4 A, V = 50 V.

THERMAL CHARACTERISTICS

Symbol	Parameter	Ratings	Unit
$R_{\theta JC}$	Thermal Resistance, Junction to Case, Max.	0.94	°C/W

PACKAGE MARKING AND ORDERING INFORMATION

Part Number	Top Marking	Package	Shipping†
FFSM2065B	FFSM2065B	PQFN4 8X8, 2P (Power88) (Halogen Free)	3000 Units / Tape & Reel

†For information on tape and reel specifications, including part orientation and tape sizes, please refer to our Tape and Reel Packaging Specifications Brochure, BRD8011/D

ELECTRICAL CHARACTERISTICS T_J = 25°C unless otherwise noted

Symbol	Parameter	Test Conditions	Min.	Typ.	Max.	Unit
V_F	Forward Voltage	I_F = 20 A, T_J = 25°C		1.38	1.7	V
		I_F = 20 A, T_J = 125°C		1.6		
		I_F = 20 A, T_J = 150°C		1.67		
I_R	Reverse Current	V_R = 650 V, T_J = 25°C		0.5	40	μA
		V_R = 650 V, T_J = 125°C		1	80	
		V_R = 650 V, T_J = 175°C		2	160	
Q_C	Total Capacitive Charge	V = 400 V		51		nC
C	Total Capacitance	V_R = 1 V, f = 100 kHz		866		pF
		V_R = 200 V, f = 100 kHz		80		
		V_R = 400 V, f = 100 kHz		70		

Product parametric performance is indicated in the Electrical Characteristics for the listed test conditions, unless otherwise noted. Product performance may not be indicated by the Electrical Characteristics if operated under different conditions.

TYPICAL CHARACTERISTICS

(T_J = 25°C UNLESS OTHERWISE NOTED)

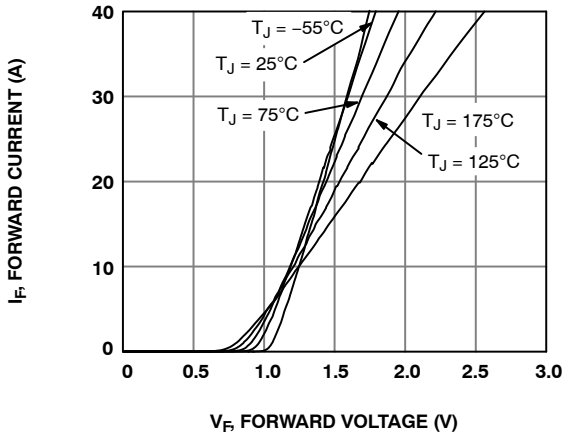


Figure 1. Forward Characteristics

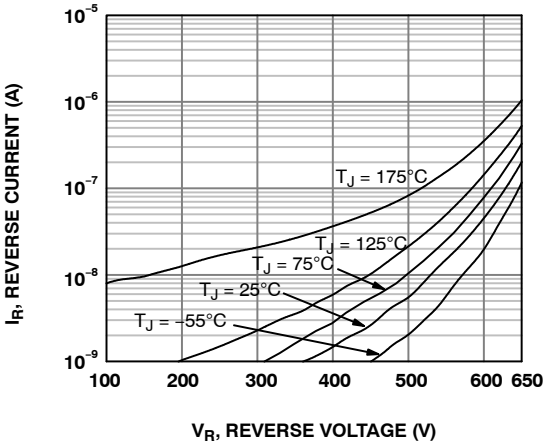


Figure 2. Reverse Characteristics

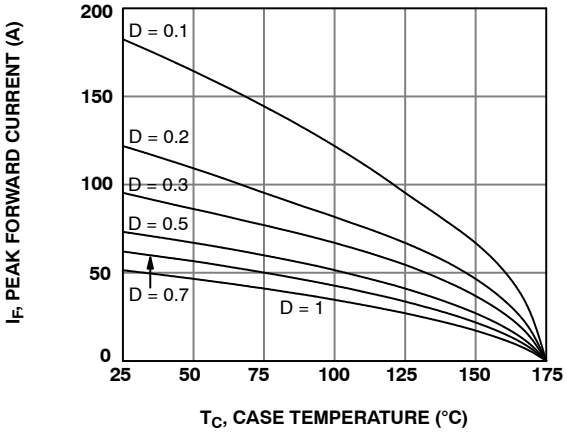


Figure 3. Current Derating

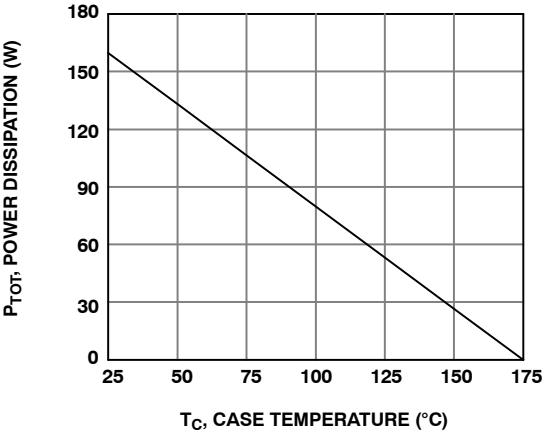


Figure 4. Power Dissipation

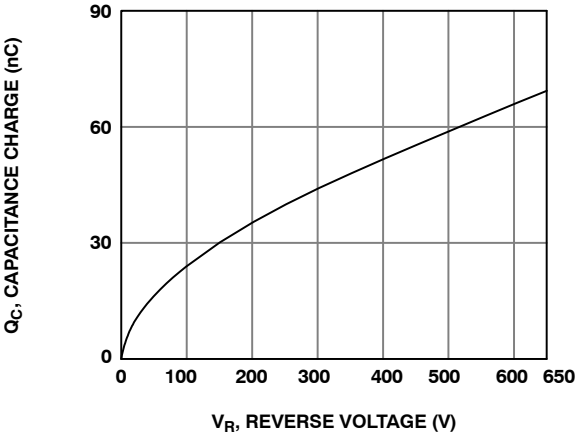


Figure 5. Capacitance Charge vs. Reverse Voltage

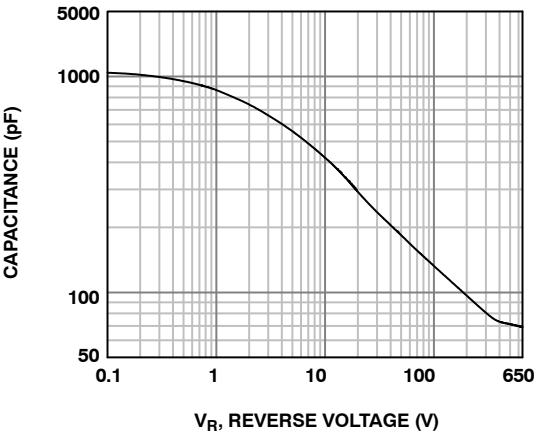


Figure 6. Capacitance vs. Reverse Voltage

TYPICAL CHARACTERISTICS (CONTINUED)

(T_J = 25°C UNLESS OTHERWISE NOTED)

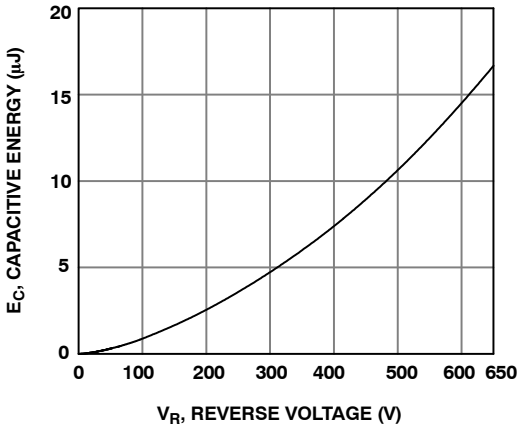


Figure 7. Capacitance Stored Energy

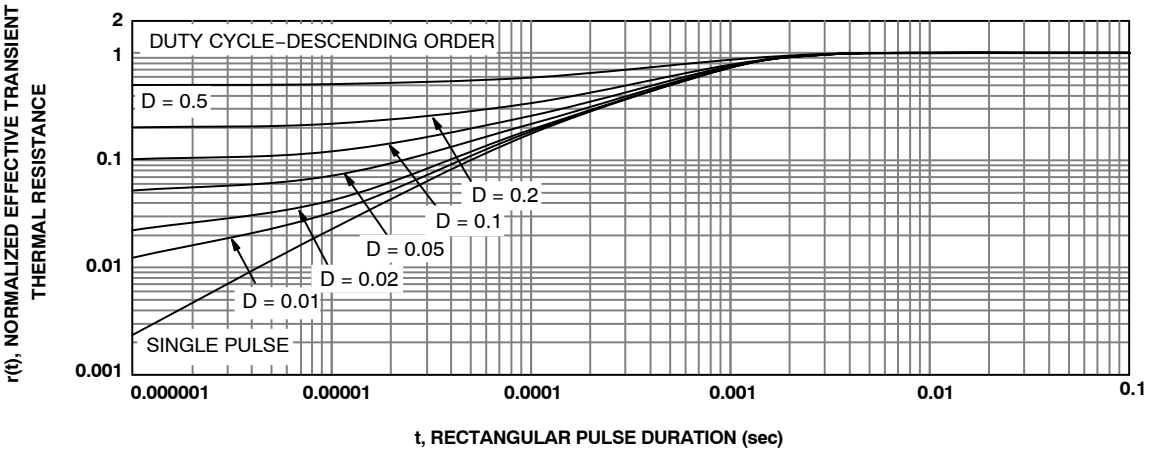
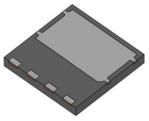


Figure 8. Junction−to−Case Transient Thermal Response Curve



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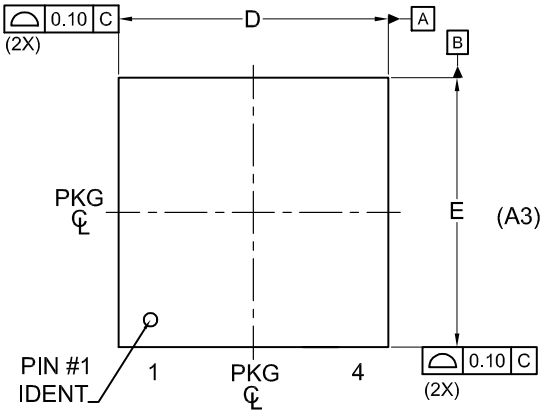
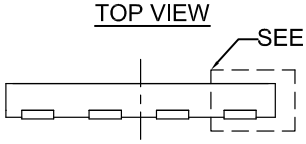
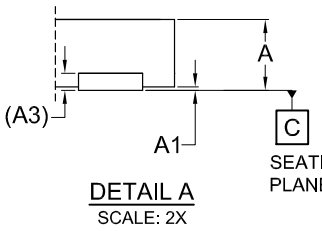
DATE 06 JUL 2021



TOP VIEW



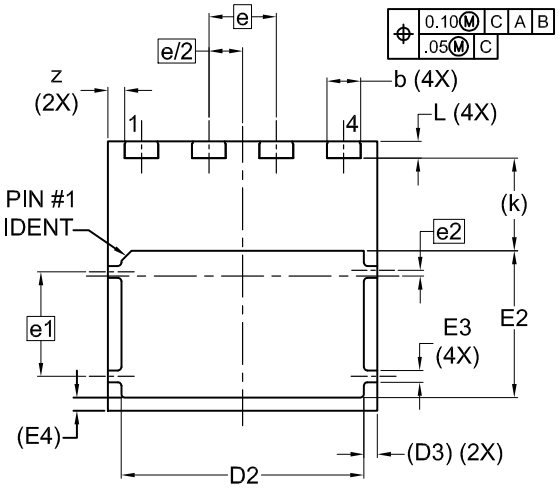
FRONT VIEW



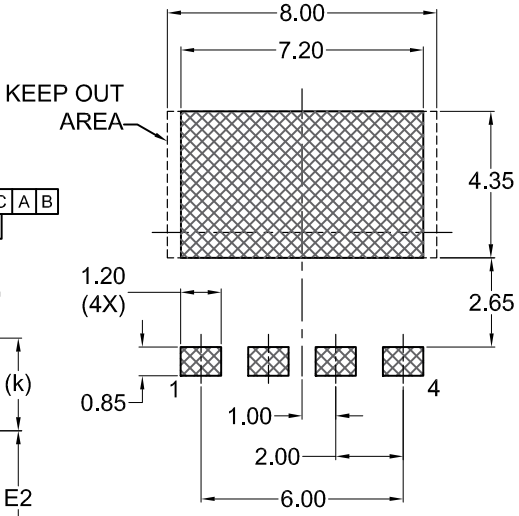
DETAIL A
SCALE: 2X

NOTES:

1. DIMENSIONING AND TOLERANCING PER ASME Y14.5M, 2009.
2. CONTROLLING DIMENSION: MILLIMETERS
3. COPLANARITY APPLIES TO THE EXPOSED PADS AS WELL AS THE TERMINALS.
4. DIMENSIONS D1 AND E1 DO NOT INCLUDE MOLD FLASH, PROTRUSIONS, OR GATE BURRS.
5. SEATING PLANE IS DEFINED BY THE TERMINALS. "A1" IS DEFINED AS THE DISTANCE FROM THE SEATING PLANE TO THE LOWEST POINT ON THE PACKAGE BODY.
6. IT IS RECOMMENDED TO HAVE NO TRACES OR VIAS WITHIN THE KEEP OUT AREA.



BOTTOM VIEW



LAND PATTERN
RECOMMENDATION

*FOR ADDITIONAL INFORMATION ON OUR PB-FREE STRATEGY AND SOLDERING DETAILS, PLEASE DOWNLOAD THE ON SEMICONDUCTOR SOLDERING AND MOUNTING TECHNIQUES REFERENCE MANUAL, SOLDERRM/D.

DIM	MILLIMETERS		
	MIN.	NOM.	MAX.
A	0.90	1.00	1.10
A1	0.00	-	0.05
A3		0.20 REF	
b	0.90	1.00	1.10
D	7.90	8.00	8.10
D2	7.10	7.20	7.30
D3		0.40 REF	
E	7.90	8.00	8.10
E2	4.25	4.35	4.45
E3	0.25	0.35	0.45
E4		0.40 REF	
e		2.00 BSC	
e/2		1.00 BSC	
e1		3.10 BSC	
e2		0.17 BSC	
k		2.75 REF	
L	0.40	0.50	0.60

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