High Voltage PNP Silicon Power Transistors

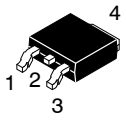
MJD5731

Designed for line operated audio output amplifier, SWITCHMODE power supply drivers and other switching applications.

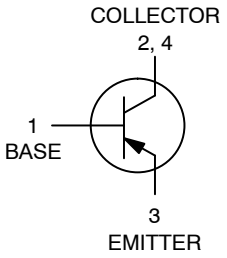
Features

- PNP Complements to the MJD47 thru MJD50 Series
- Epoxy Meets UL 94 V−0 @ 0.125 in
- These Devices are Pb−Free and are RoHS Compliant

SILICON
POWER TRANSISTORS
1.0 AMPERE
350 VOLTS, 15 WATTS



DPAK
CASE 369C
STYLE 1



MAXIMUM RATINGS

Symbol	Rating	Max	Unit
V_{CEO}	Collector−Emitter Voltage	350	Vdc
V_{EB}	Emitter−Base Voltage	5	Vdc
I_C	Collector Current − Continuous	1.0	Adc
I_{CM}	Collector Current − Peak	3.0	Adc
P_D	Total Power Dissipation @ T_C = 25°C Derate above 25°C	 15 0.12	 W W/°C
P_D	Total Power Dissipation (Note 1) @ T_A = 25°C Derate above 25°C	 1.56 0.0125	 W W/°C
E	Unclamped Inductive Load Energy (See Figure 10)	20	mJ
T_J, T_{stg}	Operating and Storage Junction Temperature Range	−55 to +150	°C
HBM	ESD − Human Body Model	3B	V
MM	ESD − Machine Model	C	V

Stresses exceeding those listed in the Maximum Ratings table may damage the device. If any of these limits are exceeded, device functionality should not be assumed, damage may occur and reliability may be affected.

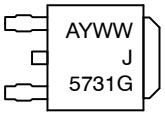
1. These ratings are applicable when surface mounted on the minimum pad sizes recommended.

THERMAL CHARACTERISTICS

Symbol	Characteristic	Max	Unit
$R_{\theta JC}$	Thermal Resistance, Junction−to−Case	8.33	°C/W
$R_{\theta JA}$	Thermal Resistance, Junction−to−Ambient (Note 2)	80	°C/W
T_L	Lead Temperature for Soldering	260	°C

2. These ratings are applicable when surface mounted on the minimum pad sizes recommended.

MARKING DIAGRAM



A	= Assembly Location
Y	= Year
WW	= Work Week
J5731	= Device Code
G	= Pb−Free Package

ORDERING INFORMATION

Device	Package	Shipping†
MJD5731T4G	DPAK (Pb−Free)	2500/Tape & Reel

†For information on tape and reel specifications, including part orientation and tape sizes, please refer to our Tape and Reel Packaging Specification Brochure, BRD8011/D.

ELECTRICAL CHARACTERISTICS (T_C = 25°C unless otherwise noted)

Symbol	Characteristic	Min	Max	Unit
OFF CHARACTERISTICS				
$V_{CEO(sus)}$	Collector−Emitter Sustaining Voltage (Note 3) (I_C = 30 mAdc, I_B = 0)	350	–	Vdc
I_{CEO}	Collector Cutoff Current (V_{CE} = 250 Vdc, I_B = 0)	–	0.1	mAdc
I_{CES}	Collector Cutoff Current (V_{CE} = 350 Vdc, V_{BE} = 0)	–	0.01	mAdc
I_{EBO}	Emitter Cutoff Current (V_{BE} = 5.0 Vdc, I_C = 0)	–	0.5	mAdc
ON CHARACTERISTICS (Note 3)				
h_{FE}	DC Current Gain (I_C = 0.3 Adc, V_{CE} = 10 Vdc) (I_C = 1.0 Adc, V_{CE} = 10 Vdc)	30 10	175 –	–
$V_{CE(sat)}$	Collector−Emitter Saturation Voltage (I_C = 1.0 Adc, I_B = 0.2 Adc)	–	1.0	Vdc
$V_{BE(on)}$	Base−Emitter On Voltage (I_C = 1.0 Adc, V_{CE} = 10 Vdc)	–	1.5	Vdc
DYNAMIC CHARACTERISTICS				
f_T	Current Gain − Bandwidth Product (I_C = 0.2 Adc, V_{CE} = 10 Vdc, f = 2.0 MHz)	10	–	MHz
h_{fe}	Small−Signal Current Gain (I_C = 0.2 Adc, V_{CE} = 10 Vdc, f = 1.0 kHz)	25	–	–

3. Pulse Test: Pulse Width ≤ 300 μs, Duty Cycle ≤ 2.0%.

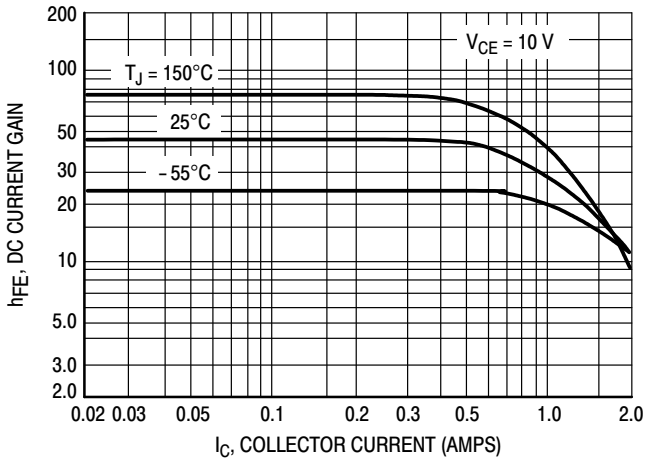


Figure 1. DC Current Gain

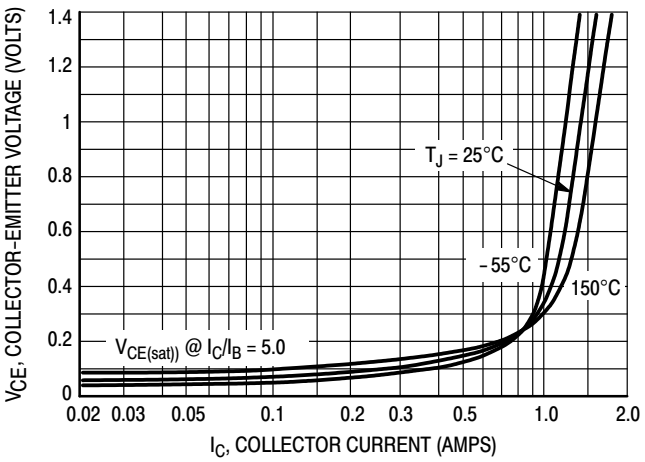


Figure 2. Collector−Emitter Saturation Voltage

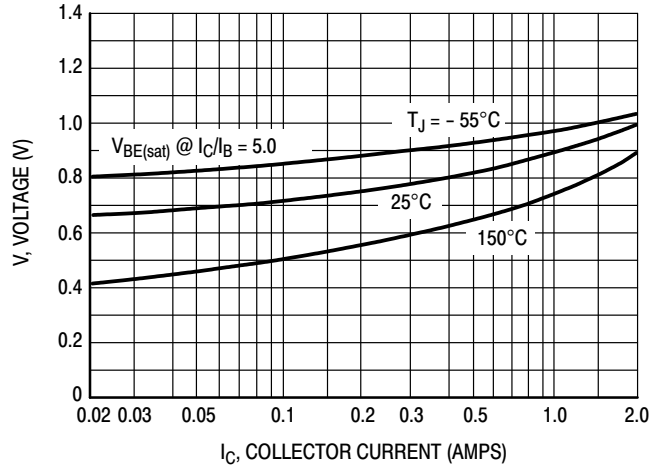


Figure 3. Base−Emitter Voltage

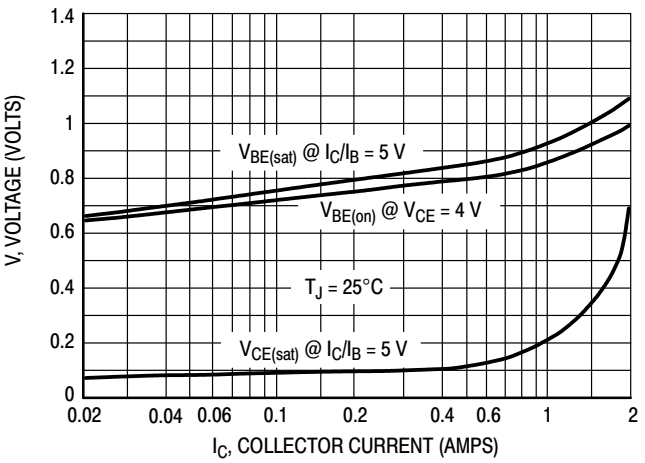


Figure 4. “On” Voltages

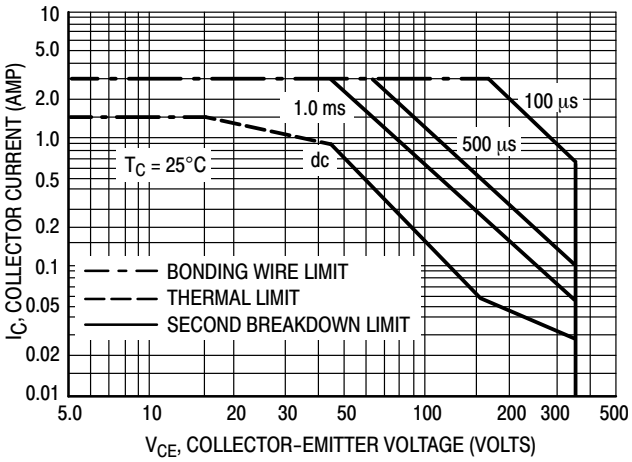


Figure 5. Forward Bias Safe Operating Area

There are two limitations on the power handling ability of a transistor: average junction temperature and second breakdown. Safe operating area curves indicate $I_C - V_{CE}$ limits of the transistor that must be observed for reliable operation; i.e., the transistor must not be subjected to greater dissipation than the curves indicate.

The data of Figure 5 is based on $T_{J(pk)}$ = 150°C; T_C is variable depending on conditions. Second breakdown pulse limits are valid for duty cycles to 10% provided $T_{J(pk)} \le 150°C$. $T_{J(pk)}$ may be calculated from the data in Figure 6. At high case temperatures, thermal limitations will reduce the power that can be handled to values less than the limitations imposed by second breakdown.

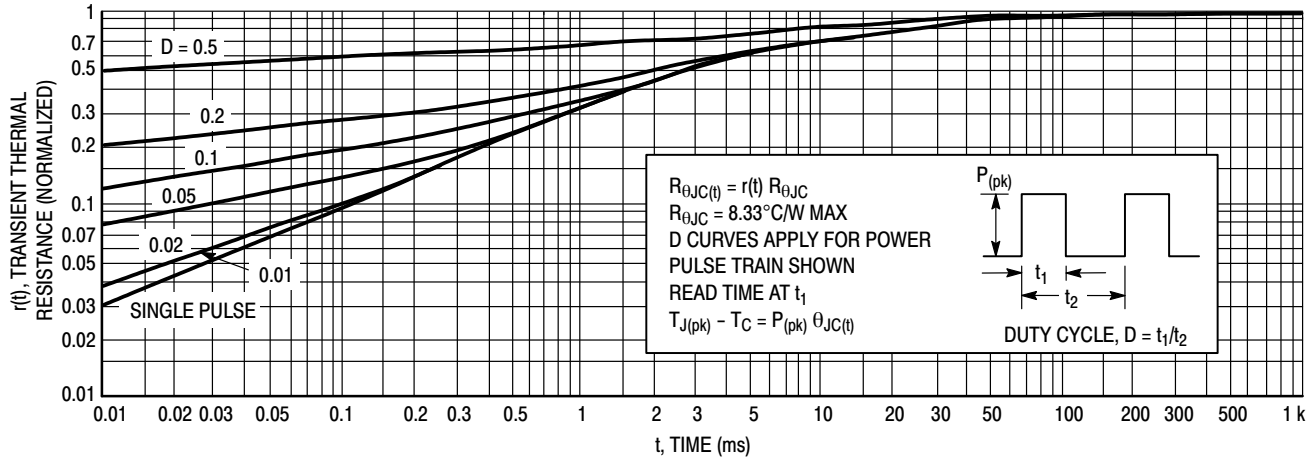


Figure 6. Thermal Response

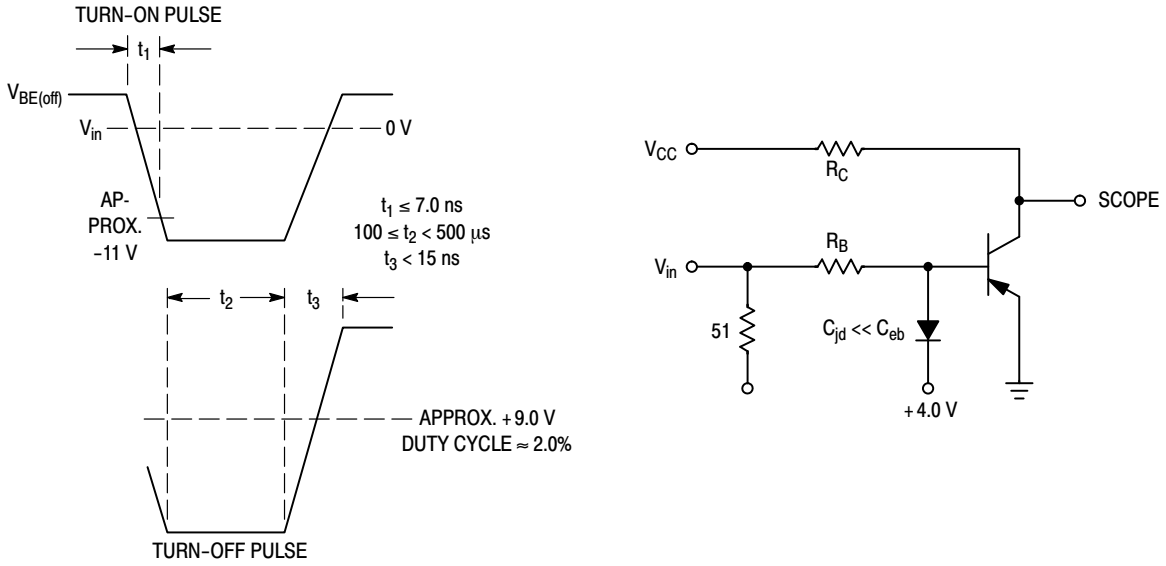


Figure 7. Switching Time Equivalent Circuit

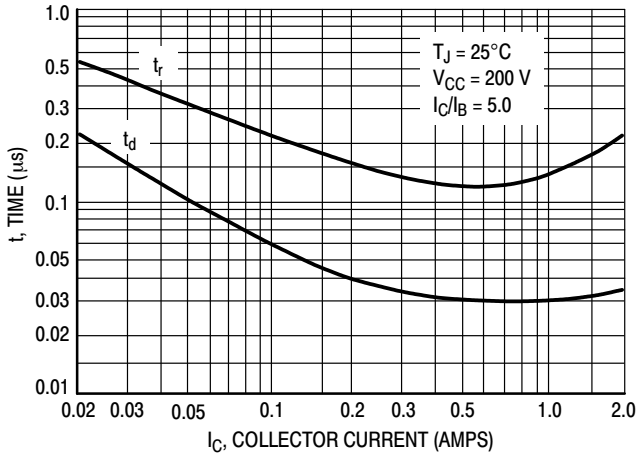


Figure 8. Turn−On Resistive Switching Times

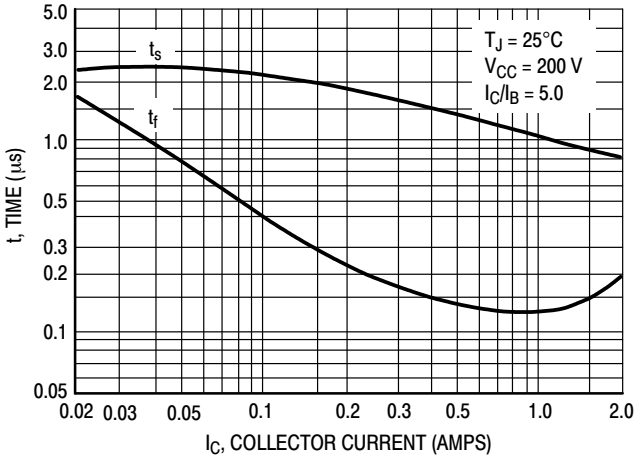
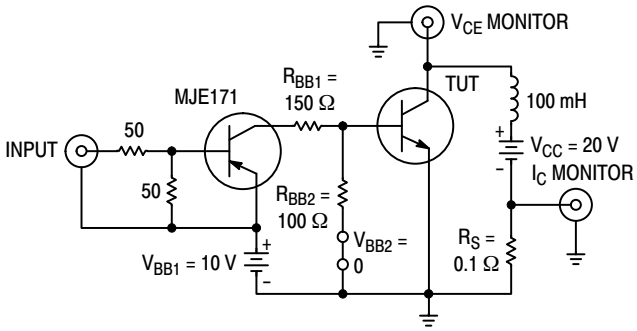


Figure 9. Resistive Turn−Off Switching Times

Test Circuit



Voltage and Current Waveforms

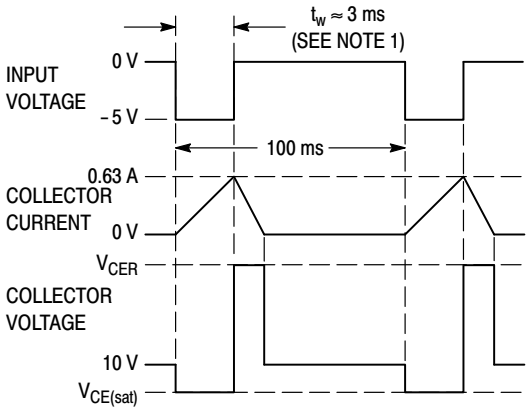
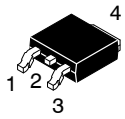


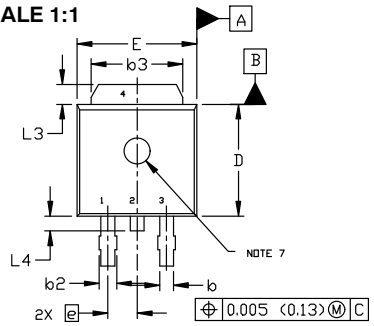
Figure 10. Inductive Load Switching



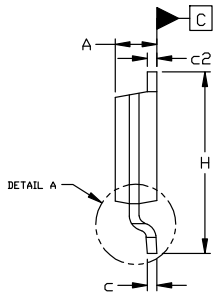
DPAK (SINGLE GAUGE)
CASE 369C
ISSUE G

DATE 31 MAY 2023

SCALE 1:1



TOP VIEW

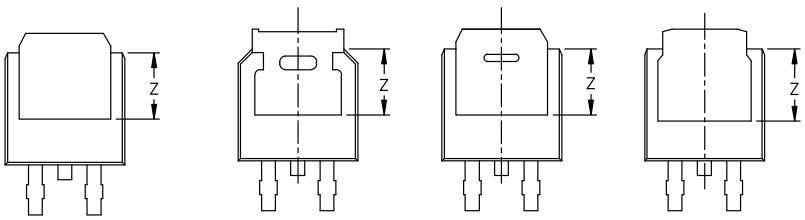


SIDE VIEW

NOTES:

1. DIMENSIONING AND TOLERANCING ASME Y14.5M, 1994.
2. CONTROLLING DIMENSION: INCHES
3. THERMAL PAD CONTOUR OPTIONAL WITHIN DIMENSIONS b3, L3, AND Z.
4. DIMENSIONS D AND E DO NOT INCLUDE MOLD FLASH, PROTRUSIONS, OR BURRS. MOLD FLASH, PROTRUSIONS, OR GATE BURRS SHALL NOT EXCEED 0.006 INCHES PER SIDE.
5. DIMENSIONS D AND E ARE DETERMINED AT THE OUTERMOST EXTREMES OF THE PLASTIC BODY.
6. DATUMS A AND B ARE DETERMINED AT DATUM PLANE H.
7. OPTIONAL MOLD FEATURE.

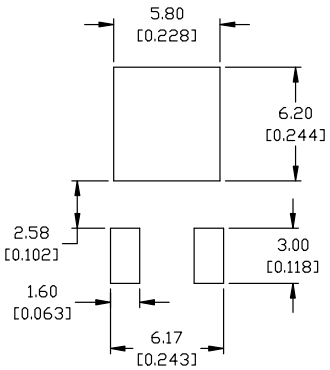
DIM	INCHES		MILLIMETERS	
	MIN.	MAX.	MIN.	MAX.
A	0.086	0.094	2.18	2.38
A1	0.000	0.005	0.00	0.13
b	0.025	0.035	0.63	0.89
b2	0.028	0.045	0.72	1.14
b3	0.180	0.215	4.57	5.46
c	0.018	0.024	0.46	0.61
c2	0.018	0.024	0.46	0.61
D	0.235	0.245	5.97	6.22
E	0.250	0.265	6.35	6.73
e	0.090 BSC		2.29 BSC	
H	0.370	0.410	9.40	10.41
L	0.055	0.070	1.40	1.78
L1	0.114 REF		2.90 REF	
L2	0.020 BSC		0.51 BSC	
L3	0.035	0.050	0.89	1.27
L4	----	0.040	---	1.01
Z	0.155	----	3.93	---



BOTTOM VIEW

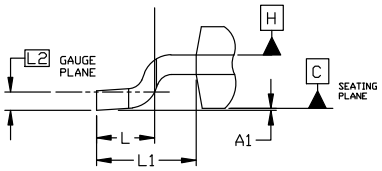
BOTTOM VIEW

ALTERNATE CONSTRUCTIONS



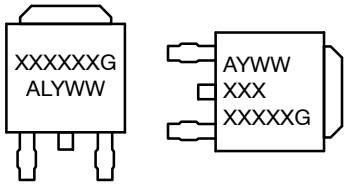
RECOMMENDED MOUNTING FOOTPRINT*

*FOR ADDITIONAL INFORMATION ON OUR PB-FREE STRATEGY AND SOLDERING DETAILS, PLEASE DOWNLOAD THE ON SEMICONDUCTOR SOLDERING AND MOUNTING TECHNIQUES REFERENCE MANUAL, SOLDERRM/D.



DETAIL A
ROTATED 90° CW

GENERIC MARKING DIAGRAM*



IC **Discrete**

XXXXXX = Device Code
A = Assembly Location
L = Wafer Lot
Y = Year
WW = Work Week
G = Pb−Free Package

*This information is generic. Please refer to device data sheet for actual part marking. Pb−Free indicator, "G" or microdot "▪", may or may not be present. Some products may not follow the Generic Marking.

STYLE 1:
PIN 1. BASE
2. COLLECTOR
3. EMITTER
4. COLLECTOR

STYLE 2:
PIN 1. GATE
2. DRAIN
3. SOURCE
4. DRAIN

STYLE 3:
PIN 1. ANODE
2. CATHODE
3. ANODE
4. CATHODE

STYLE 4:
PIN 1. CATHODE
2. ANODE
3. GATE
4. ANODE

STYLE 5:
PIN 1. GATE
2. ANODE
3. CATHODE
4. ANODE

STYLE 6:
PIN 1. MT1
2. MT2
3. GATE
4. MT2

STYLE 7:
PIN 1. GATE
2. COLLECTOR
3. EMITTER
4. COLLECTOR

STYLE 8:
PIN 1. N/C
2. CATHODE
3. ANODE
4. CATHODE

STYLE 9:
PIN 1. ANODE
2. CATHODE
3. RESISTOR ADJUST
4. CATHODE

STYLE 10:
PIN 1. CATHODE
2. ANODE
3. CATHODE
4. ANODE

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DESCRIPTION:	**DPAK (SINGLE GAUGE)**	**PAGE 1 OF 1**

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