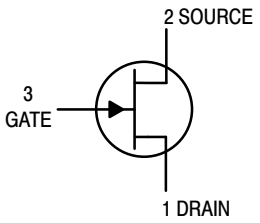
JFET Transistor

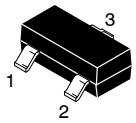
N-Channel

MMBFU310LT1G



Features

- These Devices are Pb−Free, Halogen Free/BFR Free and are RoHS Compliant



SOT−23 (TO−236AB)
CASE 318−08
STYLE 10

MAXIMUM RATINGS

Rating	Symbol	Value	Unit
Drain−Source Voltage	V_{DS}	25	Vdc
Gate−Source Voltage	V_{GS}	25	Vdc
Gate Current	I_G	10	mAdc

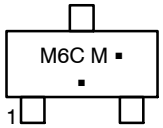
Stresses exceeding those listed in the Maximum Ratings table may damage the device. If any of these limits are exceeded, device functionality should not be assumed, damage may occur and reliability may be affected.

THERMAL CHARACTERISTICS

Total Device Dissipation FR−5 Board (Note 1) T_A = 25°C Derate above 25°C	P_D	225 1.8	mW mW/°C
Thermal Resistance, Junction−to−Ambient	$R_{\theta JA}$	556	°C/W
Junction and Storage Temperature	T_J, T_{stg}	−55 to +150	°C

1. FR−5 = 1.0 × 0.75 × 0.062 in.

MARKING DIAGRAM



M6C = Device Code
M = Date Code*
▪ = Pb−Free Package
(Note: Microdot may be in either location)
*Date Code orientation and/or overbar may vary depending upon manufacturing location.

ORDERING INFORMATION

Device	Package	Shipping†
MMBFU310LT1G	SOT−23 (Pb−Free)	3000 Tape & Reel

†For information on tape and reel specifications, including part orientation and tape sizes, please refer to our Tape and Reel Packaging Specifications Brochure, BRD8011/D.

ELECTRICAL CHARACTERISTICS (T_A = 25°C unless otherwise noted)

Characteristic	Symbol	Min	Max	Unit
OFF CHARACTERISTICS				
Gate−Source Breakdown Voltage − (I_G = −1.0 μAdc, V_{DS} = 0)	$V_{(BR)GSS}$	−25	−	Vdc
Gate 1 Leakage Current − (V_{GS} = −15 Vdc, V_{DS} = 0)	I_{G1SS}	−	−150	pA
Gate 2 Leakage Current − (V_{GS} = −15 Vdc, V_{DS} = 0, T_A = 125°C)	I_{G2SS}	−	−150	nAdc
Gate Source Cutoff Voltage − (V_{DS} = 10 Vdc, I_D = 1.0 nAdc)	$V_{GS(off)}$	−2.5	−6.0	Vdc
ON CHARACTERISTICS				
Zero−Gate−Voltage Drain Current − (V_{DS} = 10 Vdc, V_{GS} = 0)	I_{DSS}	24	60	mAdc
Gate−Source Forward Voltage − (I_G = 10 mAdc, V_{DS} = 0)	$V_{GS(f)}$	−	1.0	Vdc
SMALL−SIGNAL CHARACTERISTICS				
Forward Transfer Admittance − (V_{DS} = 10 Vdc, I_D = 10 mAdc, f = 1.0 kHz)	$\|Y_{fs}\|$	10	18	mmhos
Output Admittance − (V_{DS} = 10 Vdc, I_D = 10 mAdc, f = 1.0 kHz)	$\|y_{os}\|$	−	250	μmhos
Input Capacitance − (V_{GS} = −10 Vdc, V_{DS} = 0 Vdc, f = 1.0 MHz)	C_{iss}	−	5.0	pF
Reverse Transfer Capacitance − (V_{GS} = −10 Vdc, V_{DS} = 0 Vdc, f = 1.0 MHz)	C_{rss}	−	2.5	pF

Product parametric performance is indicated in the Electrical Characteristics for the listed test conditions, unless otherwise noted. Product performance may not be indicated by the Electrical Characteristics if operated under different conditions.

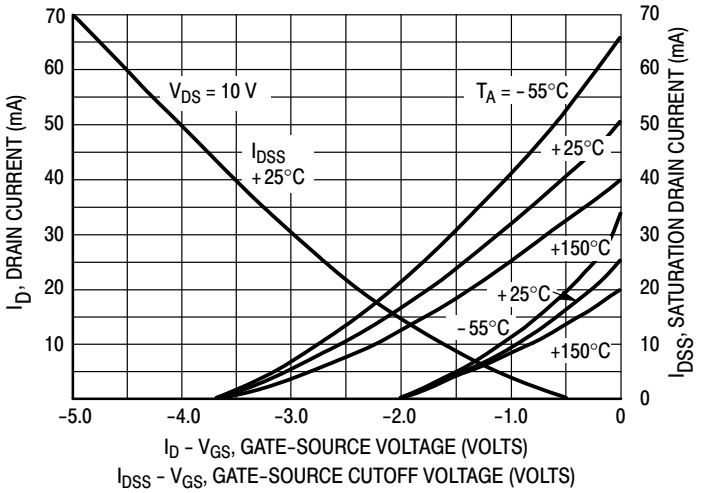


Figure 1. Drain Current and Transfer Characteristics vs Gate−Source Voltage

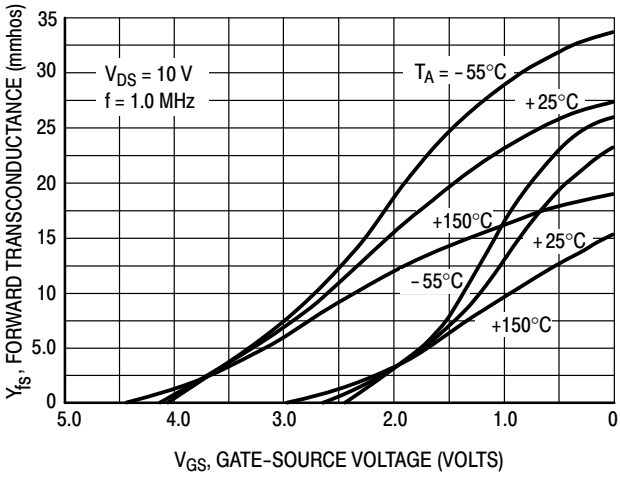


Figure 2. Forward Transconductance vs Gate−Source Voltage

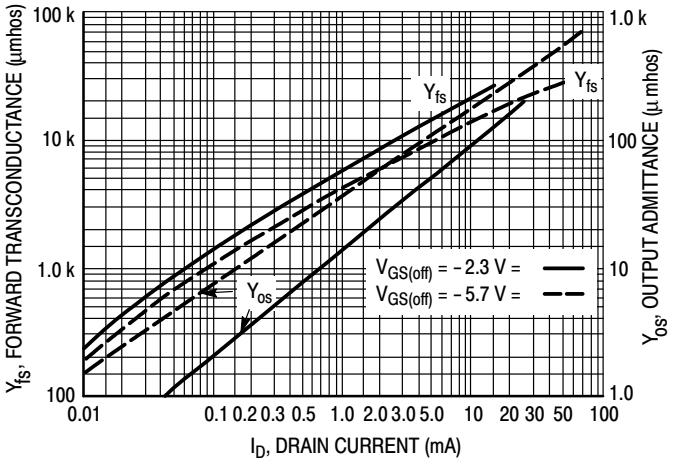


Figure 3. Common−Source Output Admittance and Forward Transconductance vs Drain Current

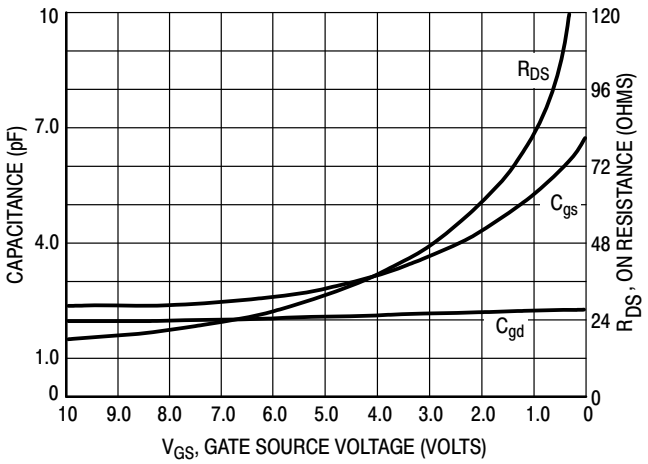


Figure 4. On Resistance and Junction Capacitance vs Gate−Source Voltage

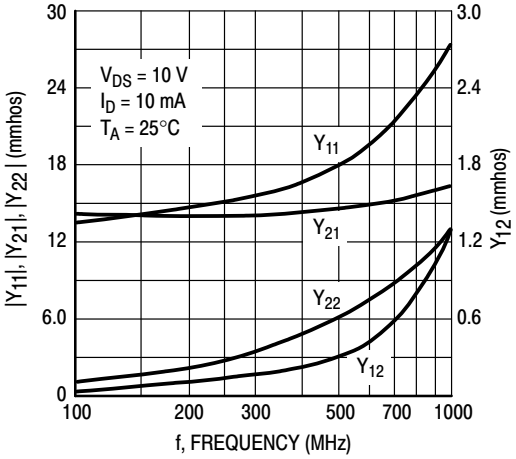


Figure 5. Common−Gate Y Parameter Magnitude vs Frequency

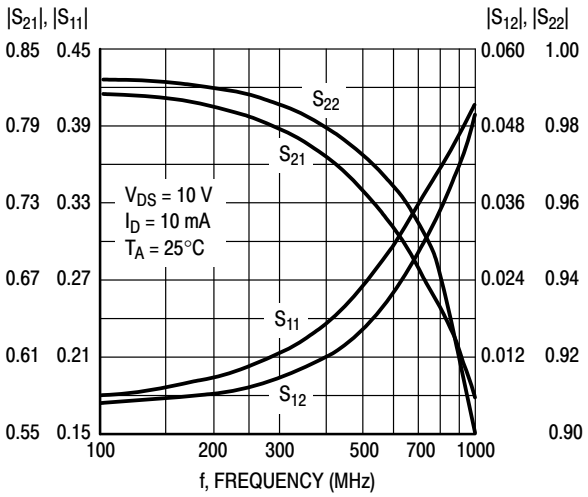


Figure 6. Common−Gate S Parameter Magnitude vs Frequency

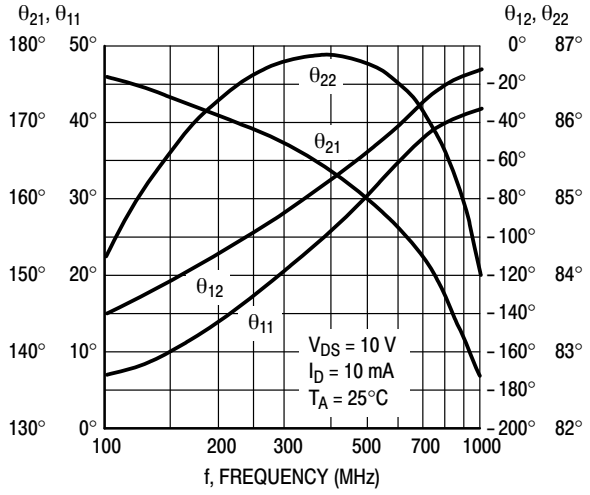


Figure 7. Common−Gate Y Parameter Phase−Angle vs Frequency

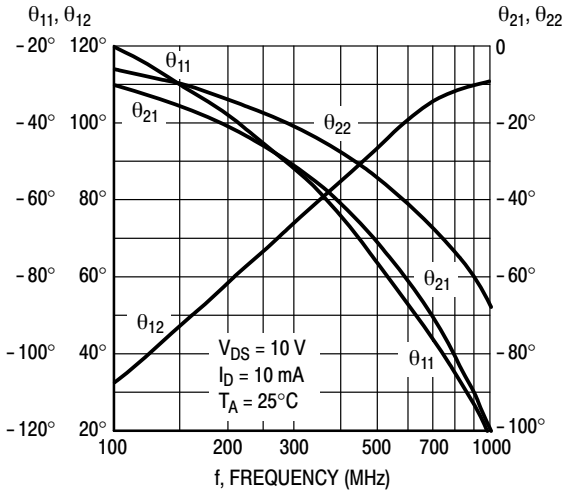
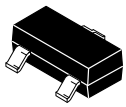


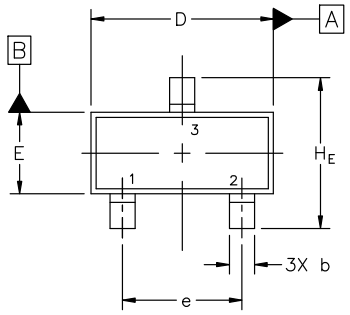
Figure 8. S Parameter Phase−Angle vs Frequency



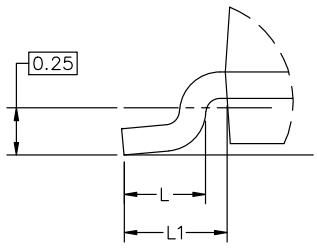
SCALE 4:1

SOT−23 (TO−236) 2.90x1.30x1.00 1.90P
CASE 318
ISSUE AU

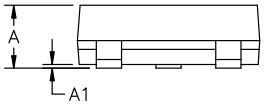
DATE 14 AUG 2024



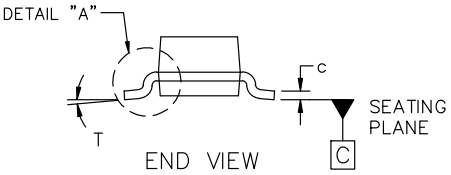
TOP VIEW



DETAIL "A"
Scale 3:1



SIDE VIEW

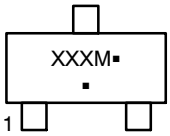


END VIEW

MILLIMETERS			
DIM	MIN	NOM	MAX
A	0.89	1.00	1.11
A1	0.01	0.06	0.10
b	0.37	0.44	0.50
c	0.08	0.14	0.20
D	2.80	2.90	3.04
E	1.20	1.30	1.40
e	1.78	1.90	2.04
L	0.30	0.43	0.55
L1	0.35	0.54	0.69
H_E	2.10	2.40	2.64
T	0°	−−−	10°

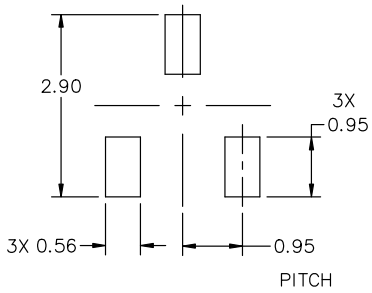
NOTES:
1. DIMENSIONING AND TOLERANCING PER ASME Y14.5M, 2018.
2. CONTROLLING DIMENSIONS: MILLIMETERS.
3. MAXIMUM LEAD THICKNESS INCLUDES LEAD FINISH. MINIMUM LEAD THICKNESS IS THE MINIMUM THICKNESS OF THE BASE MATERIAL.
4. DIMENSIONS D AND E DO NOT INCLUDE MOLD FLASH, PROTRUSIONS, OR GATE BURRS.

GENERIC
MARKING DIAGRAM*



XXX = Specific Device Code
M = Date Code
▪ = Pb−Free Package

*This information is generic. Please refer to device data sheet for actual part marking. Pb−Free indicator, "G" or microdot "▪", may or may not be present. Some products may not follow the Generic Marking.



RECOMMENDED
MOUNTING FOOTPRINT

* For additional information on our Pb−Free strategy and soldering details, please download the onsemi Soldering and Mounting Techniques Reference Manual, SOLDERRM/D.

STYLES ON PAGE 2

DOCUMENT NUMBER:	**98ASB42226B**	Electronic versions are uncontrolled except when accessed directly from the Document Repository. Printed versions are uncontrolled except when stamped "CONTROLLED COPY" in red.	
DESCRIPTION:	**SOT−23 (TO−236) 2.90x1.30x1.00 1.90P**		**PAGE 1 OF 2**

SOT−23 (TO−236) 2.90x1.30x1.00 1.90P
CASE 318
ISSUE AU

DATE 14 AUG 2024

STYLE 1 THRU 5:
CANCELLED

STYLE 6:
PIN 1. BASE
2. EMITTER
3. COLLECTOR

STYLE 7:
PIN 1. EMITTER
2. BASE
3. COLLECTOR

STYLE 8:
PIN 1. ANODE
2. NO CONNECTION
3. CATHODE

STYLE 9:
PIN 1. ANODE
2. ANODE
3. CATHODE

STYLE 10:
PIN 1. DRAIN
2. SOURCE
3. GATE

STYLE 11:
PIN 1. ANODE
2. CATHODE
3. CATHODE−ANODE

STYLE 12:
PIN 1. CATHODE
2. CATHODE
3. ANODE

STYLE 13:
PIN 1. SOURCE
2. DRAIN
3. GATE

STYLE 14:
PIN 1. CATHODE
2. GATE
3. ANODE

STYLE 15:
PIN 1. GATE
2. CATHODE
3. ANODE

STYLE 16:
PIN 1. ANODE
2. CATHODE
3. CATHODE

STYLE 17:
PIN 1. NO CONNECTION
2. ANODE
3. CATHODE

STYLE 18:
PIN 1. NO CONNECTION
2. CATHODE
3. ANODE

STYLE 19:
PIN 1. CATHODE
2. ANODE
3. CATHODE−ANODE

STYLE 20:
PIN 1. CATHODE
2. ANODE
3. GATE

STYLE 21:
PIN 1. GATE
2. SOURCE
3. DRAIN

STYLE 22:
PIN 1. RETURN
2. OUTPUT
3. INPUT

STYLE 23:
PIN 1. ANODE
2. ANODE
3. CATHODE

STYLE 24:
PIN 1. GATE
2. DRAIN
3. SOURCE

STYLE 25:
PIN 1. ANODE
2. CATHODE
3. GATE

STYLE 26:
PIN 1. CATHODE
2. ANODE
3. NO CONNECTION

STYLE 27:
PIN 1. CATHODE
2. CATHODE
3. CATHODE

STYLE 28:
PIN 1. ANODE
2. ANODE
3. ANODE

ADDITIONAL INFORMATION

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