# NSS20200W6

## 20 V, 3.0 A, Low $V_{CE(sat)}$ PNP Transistor

ON Semiconductor’s e$^2$PowerEdge family of low $V_{CE(sat)}$ transistors are miniature surface mount devices featuring ultra low saturation voltage ($V_{CE(sat)}$) and high current gain capability. These are designed for use in low voltage, high speed switching applications where affordable efficient energy control is important.

Typical applications are DC−DC converters and power management in portable and battery powered products such as cellular and cordless phones, PDAs, computers, printers, digital cameras and MP3 players. Other applications are low voltage motor controls in mass storage products such as disc drives and tape drives. In the automotive industry they can be used in air bag deployment and in the instrument cluster. The high current gain allows e$^2$PowerEdge devices to be driven directly from PMU’s control outputs, and the Linear Gain (Beta) makes them ideal components in analog amplifiers.

- This is a Pb−Free Device

**MAXIMUM RATINGS** ($T_A$ = 25°C)

| Rating | Symbol | Max | Unit |
|---|---|---|---|
| Collector-Emitter Voltage | $V_{CEO}$ | −20 | Vdc |
| Collector-Base Voltage | $V_{CBO}$ | −20 | Vdc |
| Emitter-Base Voltage | $V_{EBO}$ | −7.0 | Vdc |
| Collector Current − Continuous | $I_C$ | −2.0 | A |
| Collector Current − Peak | $I_{CM}$ | −3.0 | A |

**THERMAL CHARACTERISTICS**

| Characteristic | Symbol | Max | Unit |
|---|---|---|---|
| Total Device Dissipation<br>$T_A$ = 25°C<br>Derate above 25°C | $P_D$ (Note 1) | 426<br><br>3.4 | mW<br><br>mW/°C |
| Thermal Resistance, Junction−to−Ambient | $R_{\theta JA}$ (Note 1) | 293 | °C/W |
| Total Device Dissipation<br>$T_A$ = 25°C<br>Derate above 25°C | $P_D$ (Note 2) | 555<br><br>4.4 | mW<br><br>mW/°C |
| Thermal Resistance, Junction−to−Ambient | $R_{\theta JA}$ (Note 2) | 225 | °C/W |
| Junction and Storage Temperature Range | $T_J$, $T_{stg}$ | −55 to +150 | °C |

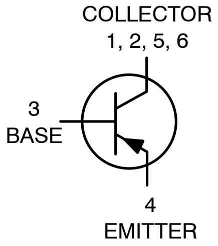
Stresses exceeding Maximum Ratings may damage the device. Maximum Ratings are stress ratings only. Functional operation above the Recommended Operating Conditions is not implied. Extended exposure to stresses above the Recommended Operating Conditions may affect device reliability.

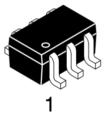
1. FR−4 @ 100 mm$^2$, 1 oz. copper traces.
2. FR−4 @ 500 mm$^2$, 1 oz. copper traces.

**ON Semiconductor®**

**http://onsemi.com**

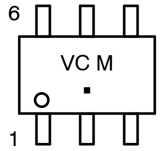
### −20 VOLTS, 3.0 AMPS PNP LOW $V_{CE(sat)}$ TRANSISTOR EQUIVALENT $R_{DS(on)}$ 65 mΩ





**SC−88/SOT−363**
**CASE 419B**
**STYLE 20**

### DEVICE MARKING



VC = Specific Device Code
M = Date Code
▪ = Pb−Free Package

### ORDERING INFORMATION

| Device | Package | Shipping† |
|---|---|---|
| NSS20200W6T1G | SC−88<br>(Pb−Free) | 3000/<br>Tape & Reel |

†For information on tape and reel specifications, including part orientation and tape sizes, please refer to our Tape and Reel Packaging Specification Brochure, BRD8011/D.

August, 2008 − Rev. 2

**ELECTRICAL CHARACTERISTICS** ($T_A$ = 25°C unless otherwise noted)

| Characteristic | Symbol | Min | Typ | Max | Unit |
|---|---|---|---|---|---|
| **OFF CHARACTERISTICS** | | | | | |
| Collector − Emitter Breakdown Voltage<br>($I_C$ = −10 mAdc, $I_B$ = 0) | $V_{(BR)CEO}$ | −20 | − | − | Vdc |
| Collector − Base Breakdown Voltage<br>($I_C$ = −0.1 mAdc, $I_E$ = 0) | $V_{(BR)CBO}$ | −20 | − | − | Vdc |
| Emitter − Base Breakdown Voltage<br>($I_E$ = −0.1 mAdc, $I_C$ = 0) | $V_{(BR)EBO}$ | −7.0 | − | − | Vdc |
| Collector Cutoff Current<br>($V_{CB}$ = −20 Vdc, $I_E$ = 0) | $I_{CBO}$ | − | − | −0.1 | μAdc |
| Emitter Cutoff Current<br>($V_{EB}$ = −7.0 Vdc) | $I_{EBO}$ | − | − | −0.1 | μAdc |
| **ON CHARACTERISTICS** | | | | | |
| DC Current Gain (Note 3)<br>($I_C$ = −10 mA, $V_{CE}$ = −2.0 V)<br>($I_C$ = −500 mA, $V_{CE}$ = −2.0 V)<br>($I_C$ = −1.0 A, $V_{CE}$ = −2.0 V)<br>($I_C$ = −2.0 A, $V_{CE}$ = −2.0 V) | $h_{FE}$ | <br>250<br>220<br>200<br>160 | <br>370<br>325<br>290<br>245 | <br>−<br>−<br>−<br>− | |
| Collector − Emitter Saturation Voltage (Note 3)<br>($I_C$ = −0.1 A, $I_B$ = −0.010 A) (Note 4)<br>($I_C$ = −1.0 A, $I_B$ = −0.100 A)<br>($I_C$ = −1.0 A, $I_B$ = −0.010 A)<br>($I_C$ = −2.0 A, $I_B$ = −0.200 A)<br>($I_C$ = −2.0 A, $I_B$ = −0.020 A) | $V_{CE(sat)}$ | <br>−<br>−<br>−<br>−<br>− | <br>−0.010<br>−0.067<br>−0.102<br>−0.128<br>−0.177 | <br>−0.014<br>−0.092<br>−0.126<br>−0.165<br>−0.215 | V |
| Base − Emitter Saturation Voltage (Note 3)<br>($I_C$ = −1.0 A, $I_B$ = −0.01 A) | $V_{BE(sat)}$ | − | − | −0.900 | V |
| Base − Emitter Turn−on Voltage (Note 3)<br>($I_C$ = −1.0 A, $V_{CE}$ = −2.0 V) | $V_{BE(on)}$ | − | − | −0.900 | V |
| Cutoff Frequency<br>($I_C$ = −100 mA, $V_{CE}$ = −5.0 V, f = 100 MHz) | $f_T$ | 100 | − | − | MHz |
| Input Capacitance ($V_{EB}$ = −0.5 V, f = 1.0 MHz) | Cibo | − | − | 330 | pF |
| Output Capacitance ($V_{CB}$ = −3.0 V, f = 1.0 MHz) | Cobo | − | − | 90 | pF |
| **SWITCHING CHARACTERISTICS** | | | | | |
| Delay ($V_{CC}$ = −10 V, $I_C$ = 750 mA, $I_{B1}$ = 15 mA) | $t_d$ | − | − | 65 | ns |
| Rise ($V_{CC}$ = −10 V, $I_C$ = 750 mA, $I_{B1}$ = 15 mA) | $t_r$ | − | − | 100 | ns |
| Storage ($V_{CC}$ = −10 V, $I_C$ = 750 mA, $I_{B1}$ = 15 mA) | $t_s$ | − | − | 320 | ns |
| Fall ($V_{CC}$ = −10 V, $I_C$ = 750 mA, $I_{B1}$ = 15 mA) | $t_f$ | − | − | 125 | ns |

3. Pulsed Condition: Pulse Width = 300 msec, Duty Cycle ≤ 2%.
4. Guaranteed by design but not tested.

## TYPICAL CHARACTERISTICS

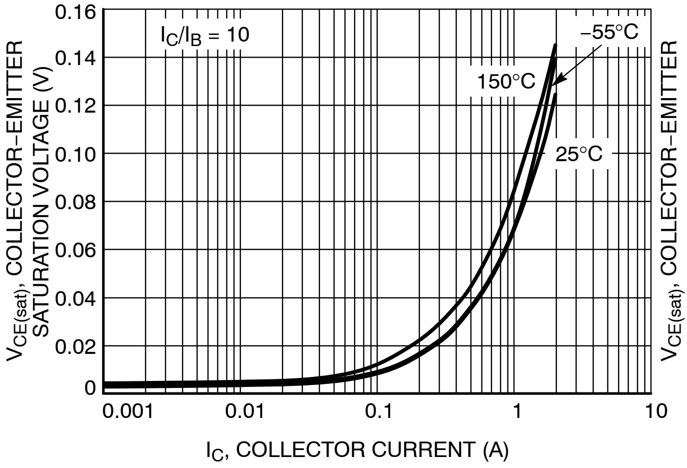


**Figure 1. Collector Emitter Saturation Voltage vs. Collector Current**

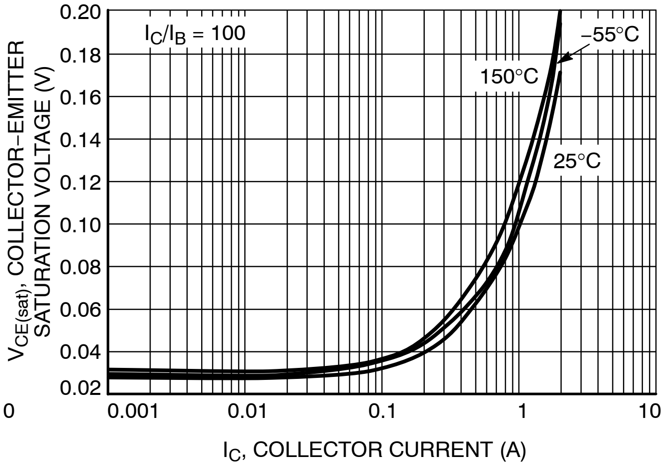


**Figure 2. Collector Emitter Saturation Voltage vs. Collector Current**

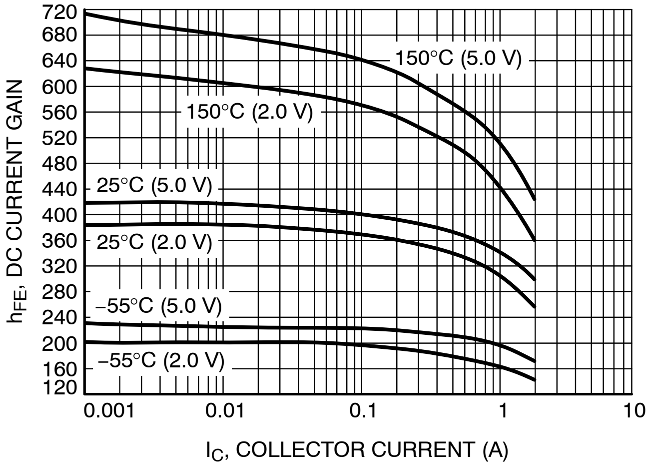


**Figure 3. DC Current Gain vs. Collector Current**

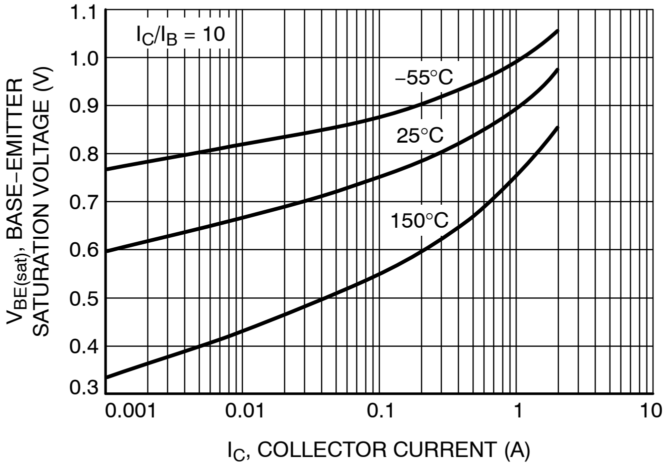


**Figure 4. Base Emitter Saturation Voltage vs. Collector Current**

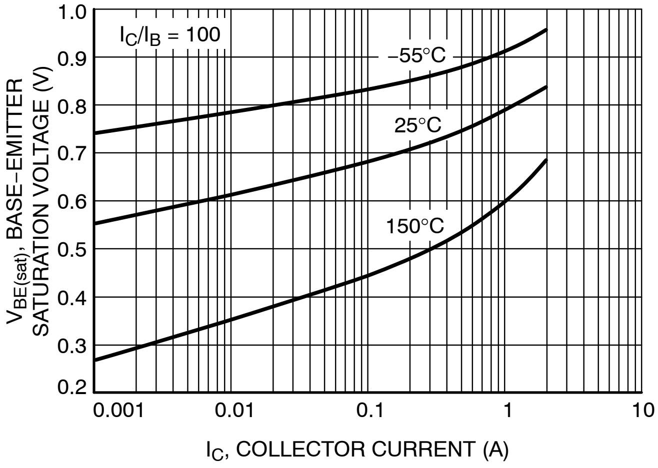


**Figure 5. Base Emitter Saturation Voltage vs. Collector Current**

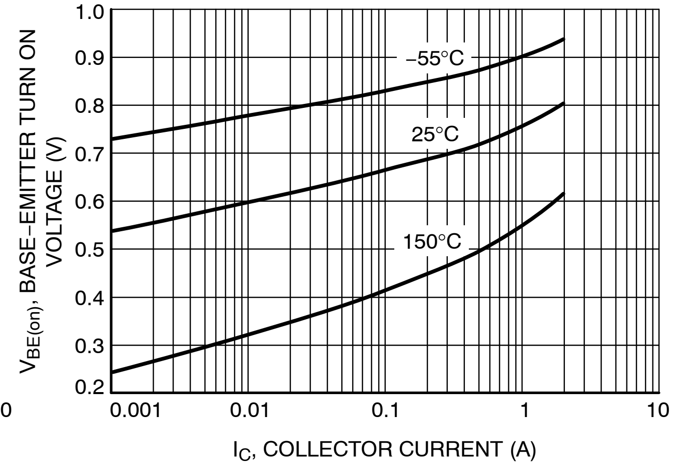


**Figure 6. Base Emitter Turn−On Voltage vs. Collector Current**

## TYPICAL CHARACTERISTICS

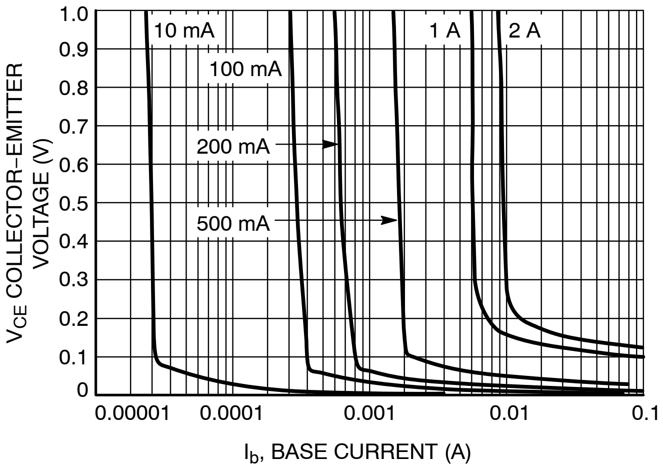


**Figure 7. Saturation Region**

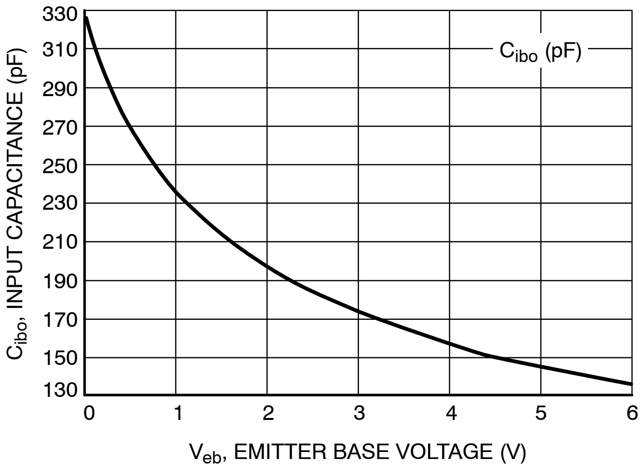


**Figure 8. Input Capacitance**

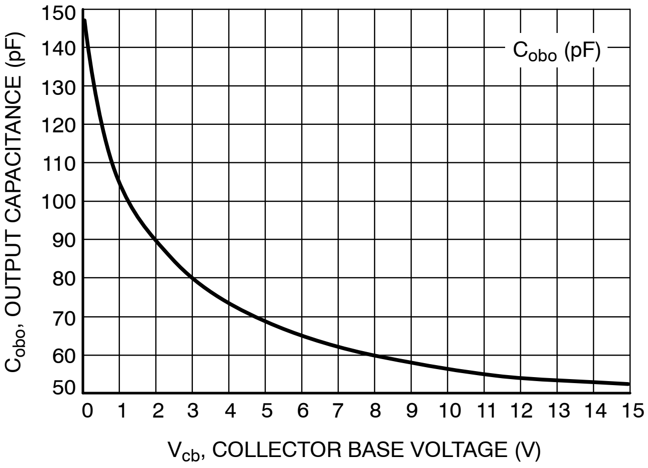


**Figure 9. Output Capacitance**

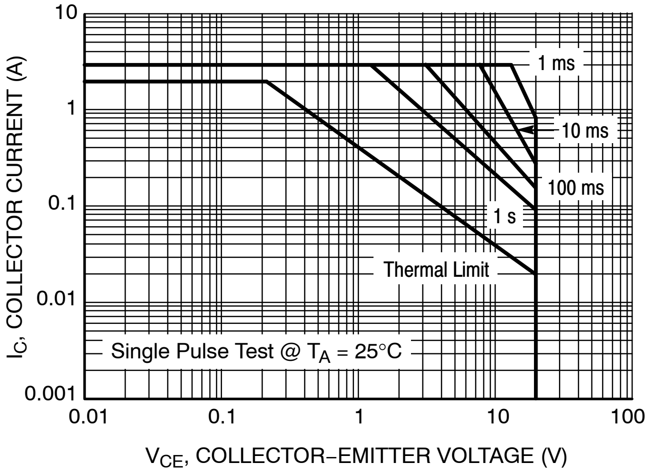
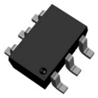
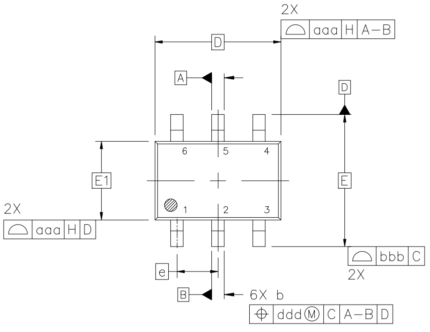


**Figure 10. Safe Operating Area**



### SC−88 2.00x1.25x0.90, 0.65P
CASE 419B−02
ISSUE Z

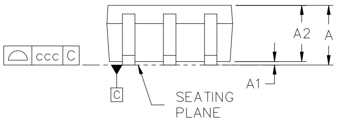
DATE 18 APR 2024



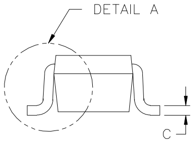
TOP VIEW

NOTES:

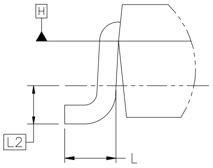
1. DIMENSIONING AND TOLERANCING CONFORM TO ASME Y14.5−2018.
2. ALL DIMENSION ARE IN MILLIMETERS.
3. DIMENSIONS D AND E1 DO NOT INCLUDE MOLD FLASH, PROTRUSIONS, OR GATE BURRS. MOLD FLASH, PROTRUSIONS, OR GATE BURRS SHALL NOT EXCEED 0.20 PER END.
4. DIMENSIONS D AND E1 AT THE OUTERMOST EXTREMES OF THE PLASTIC BODY AND DATUM H.
5. DATUMS A AND B ARE DETERMINED AT DATUM H.
6. DIMENSIONS b AND c APPLY TO THE FLAT SECTION OF THE LEAD BETWEEN 0.08 AND 0.15 FROM THE TIP.
7. DIMENSION b DOES NOT INCLUDE DAMBAR PROTRUSION. ALLOWABLE DAMBAR PROTRUSION SHALL BE 0.08 TOTAL IN EXCESS OF DIMENSION b AT MAXIMUM MATERIAL CONDITION. THE DAMBAR CANNOT BE LOCATED ON THE LOWER RADIUS OF THE FOOT.



SIDE VIEW

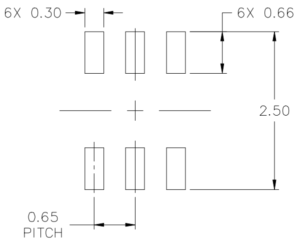


END VIEW



DETAIL A
SCALE 2:1

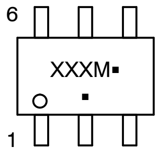
| DIM | MILLIMETERS | | |
|---|---|---|---|
| | MIN. | NOM. | MAX. |
| A | −−− | −−− | 1.10 |
| A1 | 0.00 | −−− | 0.10 |
| A2 | 0.70 | 0.90 | 1.00 |
| b | 0.15 | 0.20 | 0.25 |
| c | 0.08 | 0.15 | 0.22 |
| D | 2.00 BSC | | |
| E | 2.10 BSC | | |
| E1 | 1.25 BSC | | |
| e | 0.65 BSC | | |
| L | 0.26 | 0.36 | 0.46 |
| L2 | 0.15 BSC | | |
| aaa | 0.15 | | |
| bbb | 0.30 | | |
| ccc | 0.10 | | |
| ddd | 0.10 | | |



RECOMMENDED MOUNTING FOOTPRINT*

* FOR ADDITIONAL INFORMATION ON OUR Pb−FREE STRATEGY AND SOLDERING DETAILS, PLEASE DOWNLOAD THE ONSEMI SOLDERING AND MOUNTING TECHNIQUES REFERENCE MANUAL, SOLDERRM/D.

### GENERIC MARKING DIAGRAM*



XXX = Specific Device Code
M = Date Code*
▪ = Pb−Free Package

(Note: Microdot may be in either location)

*Date Code orientation and/or position may vary depending upon manufacturing location.

*This information is generic. Please refer to device data sheet for actual part marking. Pb−Free indicator, “G” or microdot “▪”, may or may not be present. Some products may not follow the Generic Marking.

### STYLES ON PAGE 2

| | | |
|---|---|---|
| **DOCUMENT NUMBER:** | **98ASB42985B** | Electronic versions are uncontrolled except when accessed directly from the Document Repository. Printed versions are uncontrolled except when stamped “CONTROLLED COPY” in red. |
| **DESCRIPTION:** | **SC−88 2.00x1.25x0.90, 0.65P** | **PAGE 1 OF 2** |

**SC−88 2.00x1.25x0.90, 0.65P**
CASE 419B−02
ISSUE Z

DATE 18 APR 2024

STYLE 1:
PIN 1. EMITTER 2
2. BASE 2
3. COLLECTOR 1
4. EMITTER 1
5. BASE 1
6. COLLECTOR 2

STYLE 2:
CANCELLED

STYLE 3:
CANCELLED

STYLE 4:
PIN 1. CATHODE
2. CATHODE
3. COLLECTOR
4. EMITTER
5. BASE
6. ANODE

STYLE 5:
PIN 1. ANODE
2. ANODE
3. COLLECTOR
4. EMITTER
5. BASE
6. CATHODE

STYLE 6:
PIN 1. ANODE 2
2. N/C
3. CATHODE 1
4. ANODE 1
5. N/C
6. CATHODE 2

STYLE 7:
PIN 1. SOURCE 2
2. DRAIN 2
3. GATE 1
4. SOURCE 1
5. DRAIN 1
6. GATE 2

STYLE 8:
CANCELLED

STYLE 9:
PIN 1. EMITTER 2
2. EMITTER 1
3. COLLECTOR 1
4. BASE 1
5. BASE 2
6. COLLECTOR 2

STYLE 10:
PIN 1. SOURCE 2
2. SOURCE 1
3. GATE 1
4. DRAIN 1
5. DRAIN 2
6. GATE 2

STYLE 11:
PIN 1. CATHODE 2
2. CATHODE 2
3. ANODE 1
4. CATHODE 1
5. CATHODE 1
6. ANODE 2

STYLE 12:
PIN 1. ANODE 2
2. ANODE 2
3. CATHODE 1
4. ANODE 1
5. ANODE 1
6. CATHODE 2

STYLE 13:
PIN 1. ANODE
2. N/C
3. COLLECTOR
4. EMITTER
5. BASE
6. CATHODE

STYLE 14:
PIN 1. VREF
2. GND
3. GND
4. IOUT
5. VEN
6. VCC

STYLE 15:
PIN 1. ANODE 1
2. ANODE 2
3. ANODE 3
4. CATHODE 3
5. CATHODE 2
6. CATHODE 1

STYLE 16:
PIN 1. BASE 1
2. EMITTER 2
3. COLLECTOR 2
4. BASE 2
5. EMITTER 1
6. COLLECTOR 1

STYLE 17:
PIN 1. BASE 1
2. EMITTER 1
3. COLLECTOR 2
4. BASE 2
5. EMITTER 2
6. COLLECTOR 1

STYLE 18:
PIN 1. VIN1
2. VCC
3. VOUT2
4. VIN2
5. GND
6. VOUT1

STYLE 19:
PIN 1. I OUT
2. GND
3. GND
4. V CC
5. V EN
6. V REF

STYLE 20:
PIN 1. COLLECTOR
2. COLLECTOR
3. BASE
4. EMITTER
5. COLLECTOR
6. COLLECTOR

STYLE 21:
PIN 1. ANODE 1
2. N/C
3. ANODE 2
4. CATHODE 2
5. N/C
6. CATHODE 1

STYLE 22:
PIN 1. D1 (i)
2. GND
3. D2 (i)
4. D2 (c)
5. VBUS
6. D1 (c)

STYLE 23:
PIN 1. Vn
2. CH1
3. Vp
4. N/C
5. CH2
6. N/C

STYLE 24:
PIN 1. CATHODE
2. ANODE
3. CATHODE
4. CATHODE
5. CATHODE
6. CATHODE

STYLE 25:
PIN 1. BASE 1
2. CATHODE
3. COLLECTOR 2
4. BASE 2
5. EMITTER
6. COLLECTOR 1

STYLE 26:
PIN 1. SOURCE 1
2. GATE 1
3. DRAIN 2
4. SOURCE 2
5. GATE 2
6. DRAIN 1

STYLE 27:
PIN 1. BASE 2
2. BASE 1
3. COLLECTOR 1
4. EMITTER 1
5. EMITTER 2
6. COLLECTOR 2

STYLE 28:
PIN 1. DRAIN
2. DRAIN
3. GATE
4. SOURCE
5. DRAIN
6. DRAIN

STYLE 29:
PIN 1. ANODE
2. ANODE
3. COLLECTOR
4. EMITTER
5. BASE/ANODE
6. CATHODE

STYLE 30:
PIN 1. SOURCE 1
2. DRAIN 2
3. DRAIN 2
4. SOURCE 2
5. GATE 1
6. DRAIN 1

Note: Please refer to datasheet for style callout. If style type is not called out in the datasheet refer to the device datasheet pinout or pin assignment.

| | | |
|---|---|---|
| **DOCUMENT NUMBER:** | **98ASB42985B** | Electronic versions are uncontrolled except when accessed directly from the Document Repository. Printed versions are uncontrolled except when stamped "CONTROLLED COPY" in red. |
| **DESCRIPTION:** | **SC−88 2.00x1.25x0.90, 0.65P** | **PAGE 2 OF 2** |

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