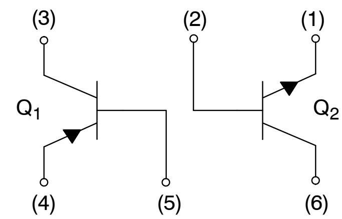
DATA SHEET
www.onsemi.com

Dual Complementary General Purpose Transistor

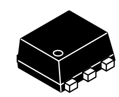
NST3946DP6T5G

The NST3946DP6T5G device is a spin−off of our popular SOT−23/SOT−323/SOT−563 three−leaded device. It is designed for general purpose amplifier applications and is housed in the SOT−963 six−leaded surface mount package. By putting two discrete devices in one package, this device is ideal for low−power surface mount applications where board space is at a premium.



NST3946DP6T5G*

*Q1 PNP
Q2 NPN



SOT−963
CASE 527AD

Features

- h_{FE}, 100−300
- Low $V_{CE(sat)}$, ≤ 0.4 V
- Reduces Board Space and Component Count
- NSV Prefix for Automotive and Other Applications Requiring Unique Site and Control Change Requirements; AEC−Q101 Qualified and PPAP Capable
- These Devices are Pb−Free, Halogen Free and are RoHS Compliant

MAXIMUM RATINGS

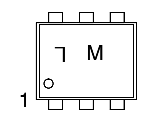
Rating	Symbol	Value	Unit
Collector − Emitter Voltage	V_{CEO}	40	Vdc
Collector − Base Voltage	V_{CBO}	60	Vdc
Emitter − Base Voltage	V_{EBO}	6.0	Vdc
Collector Current − Continuous	I_C	200	mAdc
Electrostatic Discharge HBM MM	ESD Class	2 B	

THERMAL CHARACTERISTICS

Characteristic (Single Heated)	Symbol	Max	Unit
Total Device Dissipation T_A = 25°C Derate above 25°C (Note 2)	P_D	240 1.9	mW mW/°C
Thermal Resistance, Junction-to-Ambient (Note 2)	$R_{\theta JA}$	520	°C/W
Total Device Dissipation T_A = 25°C Derate above 25°C (Note 3)	P_D	280 2.2	mW mW/°C
Thermal Resistance, Junction-to-Ambient (Note 3)	$R_{\theta JA}$	446	°C/W
Characteristic (Dual Heated) (Note 4)	**Symbol**	**Max**	**Unit**
Total Device Dissipation T_A = 25°C Derate above 25°C (Note 2)	P_D	350 2.8	mW mW/°C
Thermal Resistance, Junction-to-Ambient (Note 2)	$R_{\theta JA}$	357	°C/W
Total Device Dissipation T_A = 25°C Derate above 25°C (Note 3)	P_D	420 3.4	mW mW/°C
Thermal Resistance, Junction-to-Ambient (Note 3)	$R_{\theta JA}$	297	°C/W
Junction and Storage Temperature Range	T_J, T_{stg}	−55 to +150	°C

Stresses exceeding those listed in the Maximum Ratings table may damage the device. If any of these limits are exceeded, device functionality should not be assumed, damage may occur and reliability may be affected.
2. FR−4 @ 100 mm², 1 oz. copper traces, still air
3. FR−4 @ 500 mm², 1 oz. copper traces, still air.
4. Dual heated values assume total power is sum of two equally powered channels

MARKING DIAGRAM



L = Device Code
(180° Clockwise Rotation)
M = Date Code

ORDERING INFORMATION

Device	Package	Shipping†
NST3946DP6T5G	SOT−963 (Pb−Free)	8000 / Tape & Reel

DISCONTINUED (Note 1)

Device	Package	Shipping†
NSVT3946DP6T5G	SOT−963 (Pb−Free)	8000 / Tape & Reel

†For information on tape and reel specifications, including part orientation and tape sizes, please refer to our Tape and Reel Packaging Specifications Brochure, BRD8011/D.

1. **DISCONTINUED:** This device is not recommended for new design. Please contact your **onsemi** representative for information. The most current information on this device may be available on www.onsemi.com.

July, 2024 − Rev. 4
Publication Order Number:
NST3946DP6/D

ELECTRICAL CHARACTERISTICS (T_A = 25°C unless otherwise noted)

Characteristic		Symbol	Min	Max	Unit
OFF CHARACTERISTICS					
Collector − Emitter Breakdown Voltage (Note 5)		$V_{(BR)CEO}$			Vdc
(I_C = 1.0 mAdc, I_B = 0)	(NPN)		40	–	
(I_C = −1.0 mAdc, I_B = 0)	(PNP)		−40	–	
Collector − Base Breakdown Voltage		$V_{(BR)CBO}$			Vdc
(I_C = 10 μAdc, I_E = 0)	(NPN)		60	–	
(I_C = −10 μAdc, I_E = 0)	(PNP)		−40	–	
Emitter − Base Breakdown Voltage		$V_{(BR)EBO}$			Vdc
(I_E = 10 μAdc, I_C = 0)	(NPN)		6.0	–	
(I_E = −10 μAdc, I_C = 0)	(PNP)		−5.0	–	
Collector Cutoff Current		I_{CEX}			nAdc
(V_{CE} = 30 Vdc, V_{EB} = 3.0 Vdc)	(NPN)		–	50	
(V_{CE} = −30 Vdc, V_{EB} = −3.0 Vdc)	(PNP)		–	−50	
ON CHARACTERISTICS (Note 5)					
DC Current Gain		h_{FE}			–
(I_C = 0.1 mAdc, V_{CE} = 1.0 Vdc)	(NPN)		40	–	
(I_C = 1.0 mAdc, V_{CE} = 1.0 Vdc)			70	–	
(I_C = 10 mAdc, V_{CE} = 1.0 Vdc)			100	300	
(I_C = 50 mAdc, V_{CE} = 1.0 Vdc)			60	–	
(I_C = 100 mAdc, V_{CE} = 1.0 Vdc)			30	–	
(I_C = −0.1 mAdc, V_{CE} = −1.0 Vdc)	(PNP)		60	–	
(I_C = −1.0 mAdc, V_{CE} = −1.0 Vdc)			80	–	
(I_C = −10 mAdc, V_{CE} = −1.0 Vdc)			100	300	
(I_C = −50 mAdc, V_{CE} = −1.0 Vdc)			60	–	
(I_C = −100 mAdc, V_{CE} = −1.0 Vdc)			30	–	
Collector − Emitter Saturation Voltage		$V_{CE(sat)}$			Vdc
(I_C = 10 mAdc, I_B = 1.0 mAdc)	(NPN)		–	0.2	
(I_C = 50 mAdc, I_B = 5.0 mAdc)			–	0.3	
(I_C = −10 mAdc, I_B = −1.0 mAdc)	(PNP)		–	−0.25	
(I_C = −50 mAdc, I_B = −5.0 mAdc)			–	−0.4	
Base − Emitter Saturation Voltage		$V_{BE(sat)}$			Vdc
(I_C = 10 mAdc, I_B = 1.0 mAdc)	(NPN)		0.65	0.85	
(I_C = 50 mAdc, I_B = 5.0 mAdc)			–	0.95	
(I_C = −10 mAdc, I_B = −1.0 mAdc)	(PNP)		−0.65	−0.85	
(I_C = −50 mAdc, I_B = −5.0 mAdc)			–	−0.95	

5. Pulse Test: Pulse Width ≤ 300 μs; Duty Cycle ≤ 2.0%.

ELECTRICAL CHARACTERISTICS (T_A = 25°C unless otherwise noted) (Continued)

Characteristic		Symbol	Min	Max	Unit
SMALL−SIGNAL CHARACTERISTICS					
Current−Gain − Bandwidth Product (I_C = 10 mAdc, V_{CE} = 20 Vdc, f = 100 MHz) (I_C = −10 mAdc, V_{CE} = −20 Vdc, f = 100 MHz)	 (NPN) (PNP)	f_T	 200 250	 − −	MHz
Output Capacitance (V_{CB} = 5.0 Vdc, I_E = 0, f = 1.0 MHz) (V_{CB} = −5.0 Vdc, I_E = 0, f = 1.0 MHz)	 (NPN) (PNP)	C_{obo}	 − −	 4.0 4.5	pF
Input Capacitance (V_{EB} = 0.5 Vdc, I_C = 0, f = 1.0 MHz) (V_{EB} = −0.5 Vdc, I_C = 0, f = 1.0 MHz)	 (NPN) (PNP)	C_{ibo}	 − −	 8.0 10.0	pF
Noise Figure (V_{CE} = 5.0 Vdc, I_C = 100 μAdc, R_S = 1.0 k Ω, f = 1.0 kHz) (V_{CE} = −5.0 Vdc, I_C = −100 μAdc, R_S = 1.0 k Ω, f = 1.0 kHz)	 (NPN) (PNP)	NF	 − −	 5.0 4.0	dB
SWITCHING CHARACTERISTICS					
Delay Time (V_{CC} = 3.0 Vdc, V_{BE} = −0.5 Vdc) (V_{CC} = −3.0 Vdc, V_{BE} = 0.5 Vdc)	(NPN) (PNP)	t_d	− −	35 35	ns
Rise Time (I_C = 10 mAdc, I_{B1} = 1.0 mAdc) (I_C = −10 mAdc, I_{B1} = −1.0 mAdc)	(NPN) (PNP)	t_r	− −	35 35	
Storage Time (V_{CC} = 3.0 Vdc, I_C = 10 mAdc) (V_{CC} = −3.0 Vdc, I_C = −10 mAdc)	(NPN) (PNP)	t_s	− −	275 250	ns
Fall Time (I_{B1} = I_{B2} = 1.0 mAdc) (I_{B1} = I_{B2} = −1.0 mAdc)	(NPN) (PNP)	t_f	− −	50 50	

NPN TRANSISTOR

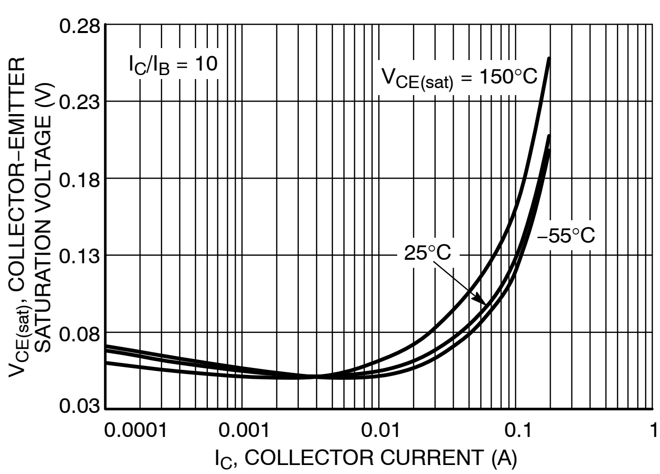


Figure 1. Collector Emitter Saturation Voltage vs. Collector Current

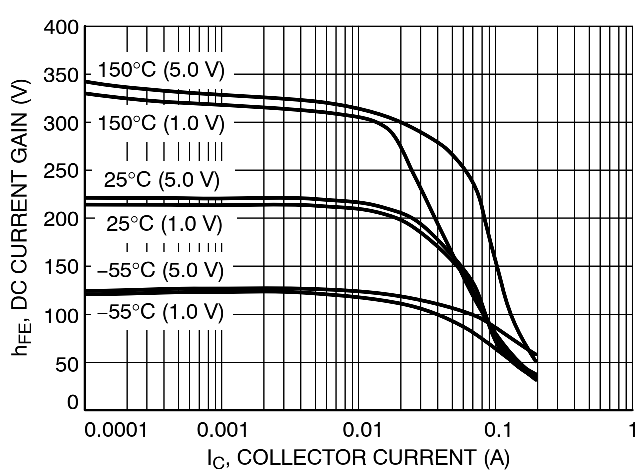


Figure 2. DC Current Gain vs. Collector Current

NPN TRANSISTOR

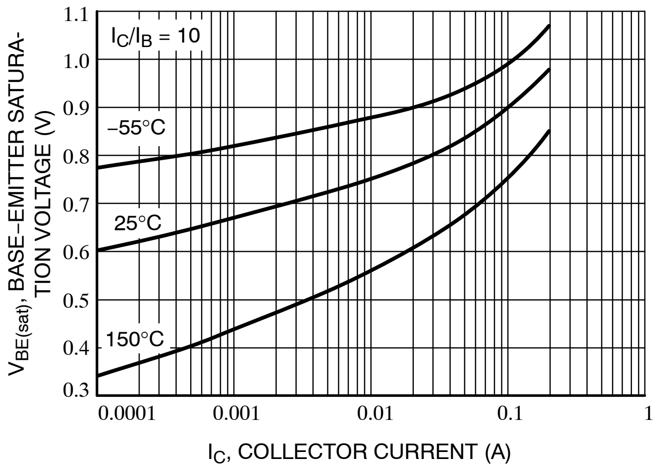


Figure 3. Base Emitter Saturation Voltage vs. Collector Current

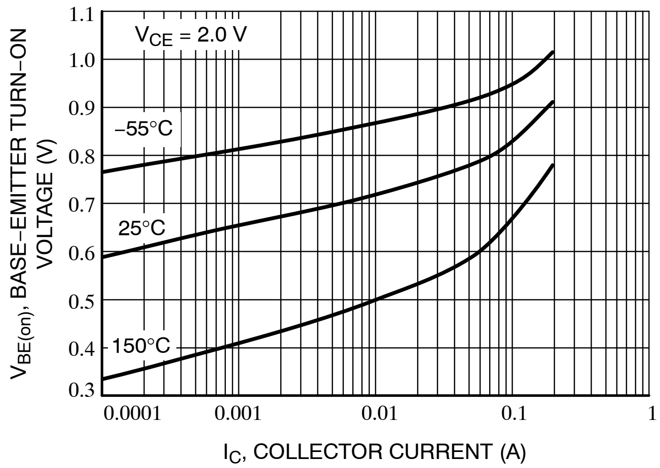


Figure 4. Base Emitter Turn−On Voltage vs. Collector Current

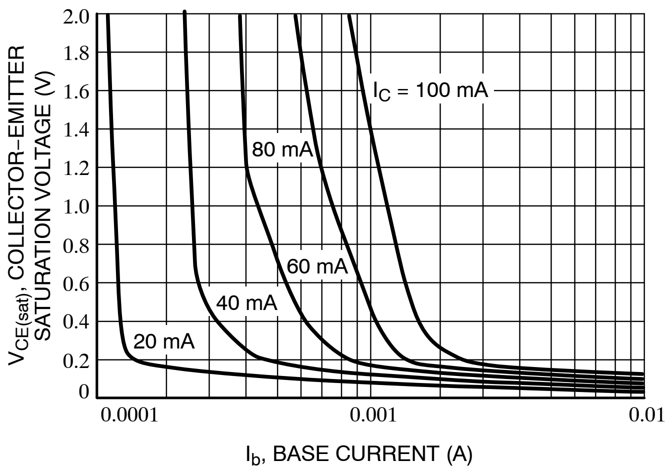


Figure 5. Saturation Region

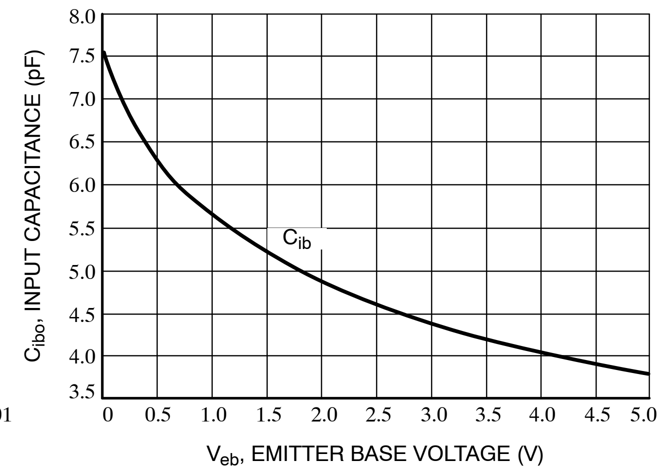


Figure 6. Input Capacitance

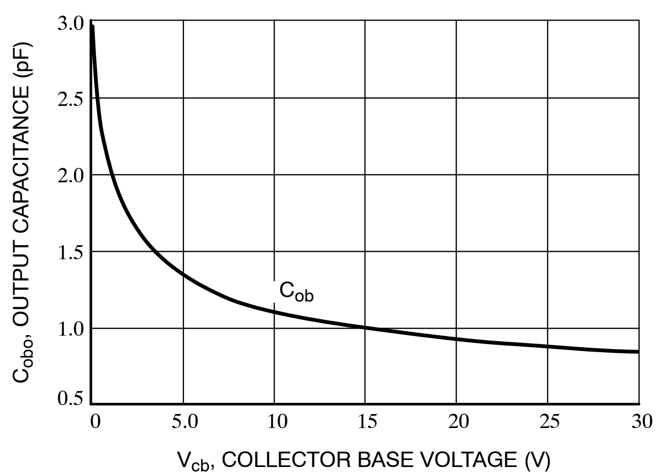


Figure 7. Output Capacitance

PNP TRANSISTOR

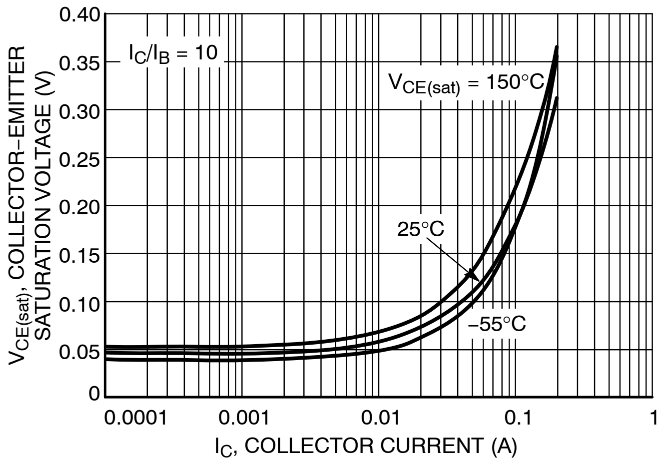


Figure 8. Collector Emitter Saturation Voltage vs. Collector Current

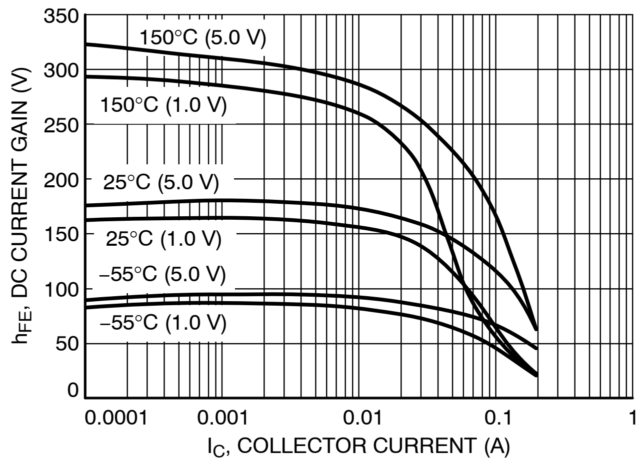


Figure 9. DC Current Gain vs. Collector Current

PNP TRANSISTOR

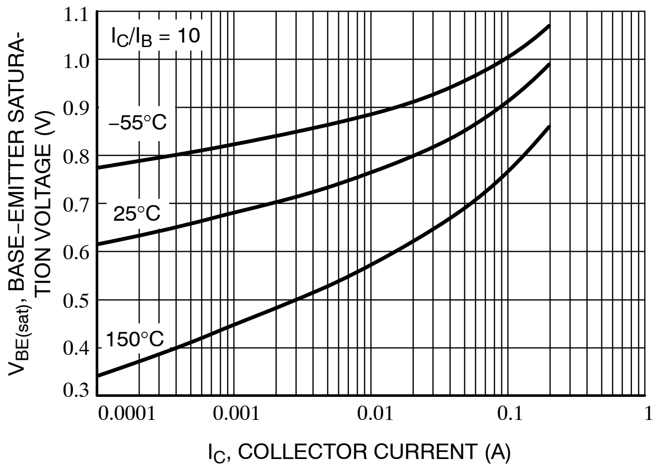


Figure 10. Base Emitter Saturation Voltage vs. Collector Current

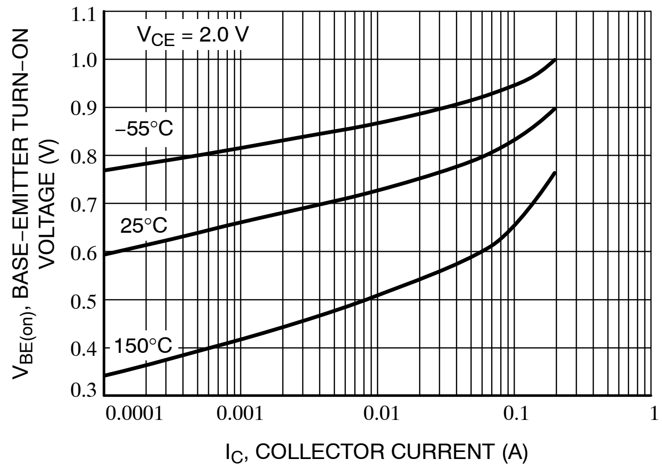


Figure 11. Base Emitter Turn−On Voltage vs. Collector Current

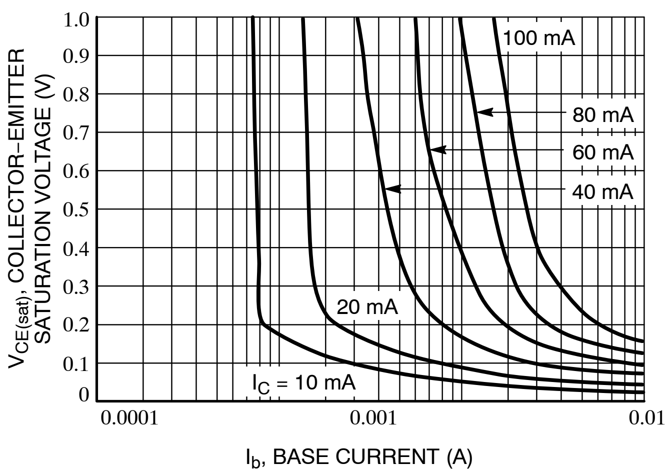


Figure 12. Saturation Region

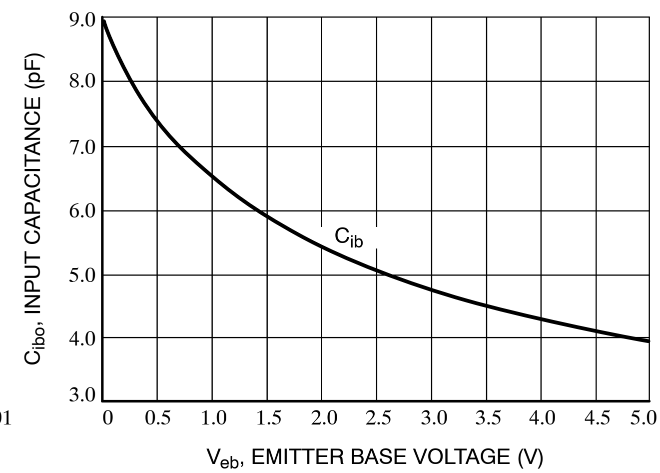


Figure 13. Input Capacitance

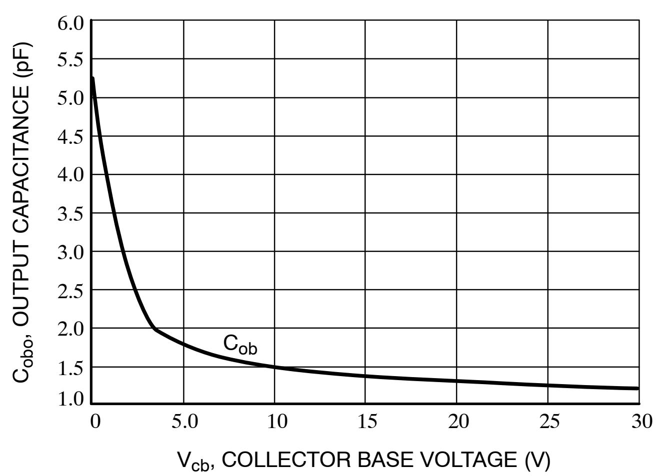
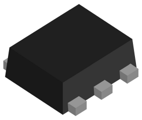


Figure 14. Output Capacitance

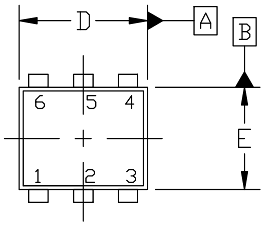


SOT−963 1.00x1.00x0.37, 0.35P
CASE 527AD
ISSUE F

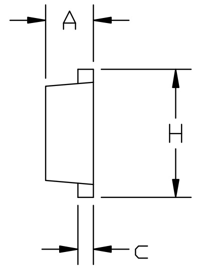
DATE 20 FEB 2024

NOTES:
1. DIMENSIONING AND TOLERANCING PER ASME Y14.5M, 2018.
2. CONTROLLING DIMENSION: MILLIMETERS.
3. MAXIMUM LEAD THICKNESS INCLUDES LEAD FINISH THICKNESS. MINIMUM LEAD THICKNESS IS THE MINIMUM THICKNESS OF BASE MATERIAL.
4. DIMENSIONS D AND E DO NOT INCLUDE MOLD FLASH, PROTRUSIONS, OR GATE BURRS.

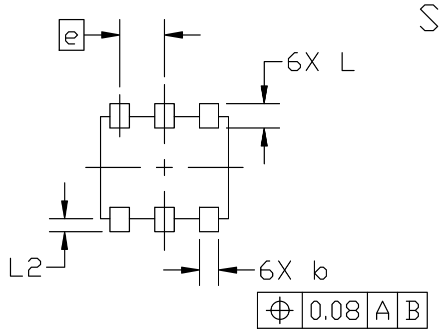
DIM	MILLIMETERS		
	MIN.	NOM.	MAX.
A	0.34	0.37	0.40
b	0.10	0.15	0.20
c	0.07	0.12	0.17
D	0.95	1.00	1.05
E	0.75	0.80	0.85
e	0.35 BSC		
H	0.95	1.00	1.05
L	0.19 REF		
L2	0.05	0.10	0.15



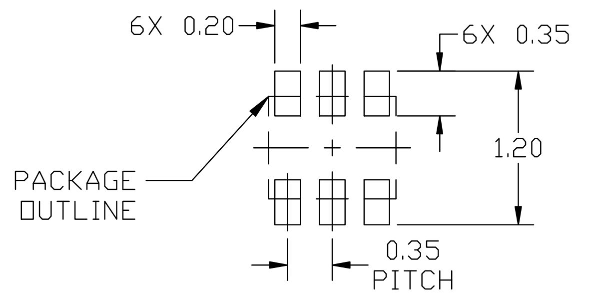
TOP VIEW



SIDE VIEW



BOTTOM VIEW



RECOMMENDED MOUNTING FOOTPRINT

*For additional information on our Pb−Free strategy and soldering details, please download the ON Semiconductor Soldering and Mounting Techniques Reference manual, SOLDERRM/D.

STYLE 1:
PIN 1. EMITTER 1
2. BASE 1
3. COLLECTOR 2
4. EMITTER 2
5. BASE 2
6. COLLECTOR 1

STYLE 2:
PIN 1. EMITTER 1
2. EMITTER2
3. BASE 2
4. COLLECTOR 2
5. BASE 1
6. COLLECTOR 1

STYLE 3:
PIN 1. CATHODE 1
2. CATHODE 1
3. ANODE/ANODE 2
4. CATHODE 2
5. CATHODE 2
6. ANODE/ANODE 1

STYLE 4:
PIN 1. COLLECTOR
2. COLLECTOR
3. BASE
4. EMITTER
5. COLLECTOR
6. COLLECTOR

STYLE 5:
PIN 1. CATHODE
2. CATHODE
3. ANODE
4. ANODE
5. CATHODE
6. CATHODE

STYLE 6:
PIN 1. CATHODE
2. ANODE
3. CATHODE
4. CATHODE
5. CATHODE
6. CATHODE

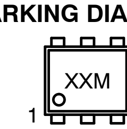
STYLE 7:
PIN 1. CATHODE
2. ANODE
3. CATHODE
4. CATHODE
5. ANODE
6. CATHODE

STYLE 8:
PIN 1. DRAIN
2. DRAIN
3. GATE
4. SOURCE
5. DRAIN
6. DRAIN

STYLE 9:
PIN 1. SOURCE 1
2. GATE 1
3. DRAIN 2
4. SOURCE 2
5. GATE 2
6. DRAIN 1

STYLE 10:
PIN 1. CATHODE 1
2. N/C
3. CATHODE 2
4. ANODE 2
5. N/C
6. ANODE 1

GENERIC MARKING DIAGRAM*



XX = Specific Device Code
M = Month Code

*This information is generic. Please refer to device data sheet for actual part marking. Pb−Free indicator, “G” or microdot “▪”, may or may not be present. Some products may not follow the Generic Marking.

DOCUMENT NUMBER:	**98AON26456D**	Electronic versions are uncontrolled except when accessed directly from the Document Repository. Printed versions are uncontrolled except when stamped “CONTROLLED COPY” in red.
DESCRIPTION:	**SOT−963 1.00x1.00x0.37, 0.35P**	**PAGE 1 OF 1**

ADDITIONAL INFORMATION

TECHNICAL PUBLICATIONS:
Technical Library: www.onsemi.com/design/resources/technical−documentation
onsemi Website: www.onsemi.com

ONLINE SUPPORT: www.onsemi.com/support
For additional information, please contact your local Sales Representative at
www.onsemi.com/support/sales

◊