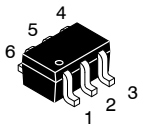
PNP General Purpose and NPN Bias Resistor Transistor Combination

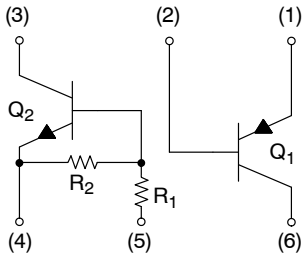
NSTB60BDW1



SOT−363
CASE 419B
STYLE 1

Features

- Simplifies Circuit Design
- Reduces Board Space
- Reduces Component Count
- Available in 8 mm, 7 inch/3000 Unit Tape and Reel
- ESD Rating − Human Body Model: Class 1B
  − Machine Model: Class B
- NSV Prefix for Automotive and Other Applications Requiring Unique Site and Control Change Requirements; AEC−Q101 Qualified and PPAP Capable
- These Devices are Pb−Free, Halogen Free/BFR Free and are RoHS Compliant



MAXIMUM RATINGS

(T_A = 25°C unless otherwise noted, common for Q_1 and Q_2)

Symbol	Rating	Q_1	Q_2	Unit
V_{CEO}	Collector-Emitter Voltage	−50	50	Vdc
V_{CBO}	Collector-Base Voltage	−50	50	Vdc
V_{EBO}	Emitter−Base Voltage	−6.0	5.0	Vdc
I_C	Collector Current − Continuous	−150	150	mAdc

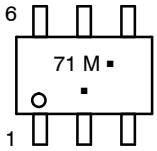
Stresses exceeding those listed in the Maximum Ratings table may damage the device. If any of these limits are exceeded, device functionality should not be assumed, damage may occur and reliability may be affected.

THERMAL CHARACTERISTICS

Symbol	Characteristic (One Junction Heated)	Max	Unit
P_D	Total Device Dissipation T_A = 25°C Derate above 25°C	187 (Note 1) 256 (Note 2) 1.5 (Note 1) 2.0 (Note 2)	mW mW/°C
$R_{\theta JA}$	Thermal Resistance − Junction-to-Ambient	670 (Note 1) 490 (Note 2)	°C/W
Symbol	**Characteristic (Both Junctions Heated)**	**Max**	**Unit**
P_D	Total Device Dissipation T_A = 25°C Derate above 25°C	250 (Note 1) 385 (Note 2) 2.0 (Note 1) 3.0 (Note 2)	mW mW/°C
$R_{\theta JA}$	Thermal Resistance − Junction-to-Ambient	493 (Note 1) 325 (Note 2)	°C/W
$R_{\theta JL}$	Thermal Resistance − Junction-to-Lead	188 (Note 1) 208 (Note 2)	°C/W
T_J, T_{stg}	Junction and Storage Temperature	−55 to +150	°C

1. FR−4 @ Minimum Pad
2. FR−4 @ 1.0 x 1.0 inch Pad

MARKING DIAGRAM



71 = Device Code
M = Date Code*
▪ = Pb−Free Package

(Note: Microdot may be in either location)

*Date Code orientation may vary depending upon manufacturing location.

ORDERING INFORMATION

Device	Package	Shipping†
NSTB60BDW1T1G	SOT−363 (Pb−Free)	3,000 / Tape & Reel
NSVTB60BDW1T1G	SOT−363 (Pb−Free)	3,000 / Tape & Reel

†For information on tape and reel specifications, including part orientation and tape sizes, please refer to our Tape and Reel Packaging Specification Brochure, BRD8011/D.

ELECTRICAL CHARACTERISTICS (T_A = 25°C unless otherwise noted)

Symbol	Characteristic	Min	Typ	Max	Unit
Q_1					
$V_{(BR)CBO}$	Collector-Base Breakdown Voltage (I_C = −50 μAdc, I_E = 0)	−50	–	–	Vdc
$V_{(BR)CEO}$	Collector-Emitter Breakdown Voltage (I_C = −1.0 mAdc, I_B = 0)	−50	–	–	Vdc
$V_{(BR)EBO}$	Emitter−Base Breakdown Voltage (I_E = −50 μAdc, I_E = 0)	−6.0	–	–	Vdc
I_{CBO}	Collector−Base Cutoff Current (V_{CB} = −50 Vdc, I_E = 0)	–	–	−0.1	μA
I_{EBO}	Emitter−Base Cutoff Current (V_{EB} = −6.0 Vdc, I_B = 0)	–	–	−0.1	μA
$V_{CE(sat)}$	Collector-Emitter Saturation Voltage (I_C = −50 mAdc, I_B = −5.0 mAdc) (Note 3)	–	–	−0.5	Vdc
h_{FE}	DC Current Gain (V_{CE} = −10 V, I_C = −5.0 mA) (Note 3)	120	–	560	–
f_T	Transition Frequency (V_{CE} = −12 Vdc, I_C = −2.0 mAdc, f = 100 MHz)	–	140	–	MHz
C_{OB}	Output Capacitance (V_{CB} = −12 Vdc, I_E = 0 Adc, f = 1.0 MHz)	–	3.5	–	pF
Q_2					
$V_{(BR)CBO}$	Collector-Base Breakdown Voltage (I_C = 50 μA, I_E = 0)	50	–	–	Vdc
$V_{(BR)CEO}$	Collector-Emitter Breakdown Voltage (I_C = 1.0 mA, I_B = 0) (Note 3)	50	–	–	Vdc
I_{CBO}	Collector−Base Cutoff Current (V_{CB} = 50 V, I_E = 0)	–	–	100	nAdc
I_{CEO}	Collector−Emitter Cutoff Current (V_{CE} = 50 V, I_B = 0)	–	–	500	nAdc
I_{EBO}	Emitter−Base Cutoff Current (V_{EB} = 6.0 V, I_C = 0)	–	–	0.13	mAdc
$V_{CE(sat)}$	Collector-Emitter Saturation Voltage (I_C = 10 mA, I_B = 5.0 mA) (Note 3)	–	–	0.25	Vdc
h_{FE}	DC Current Gain (V_{CE} = 10 V, I_C = 5.0 mA) (Note 3)	80	–	–	
V_{OL}	Output Voltage (on) (V_{CC} = 5.0 V, V_B = 4.0 V, R_L = 1.0 kΩ) (Note 3)	–	–	0.2	Vdc
V_{OH}	Output Voltage (off) (V_{CC} = 5.0 V, V_B = 0.25 V, R_L = 1.0 kΩ) (Note 3)	4.9	–	–	Vdc
R1	Input Resistor (Note 3)	15.4	22	28.6	kΩ
R2/R1	Resistor Ratio (Note 3)	1.70	2.13	2.55	

Product parametric performance is indicated in the Electrical Characteristics for the listed test conditions, unless otherwise noted. Product performance may not be indicated by the Electrical Characteristics if operated under different conditions.

3. Pulse Test: Pulse Width < 300 μs, Duty Cycle < 2.0%

TYPICAL ELECTRICAL CHARACTERISTICS – PNP TRANSISTOR

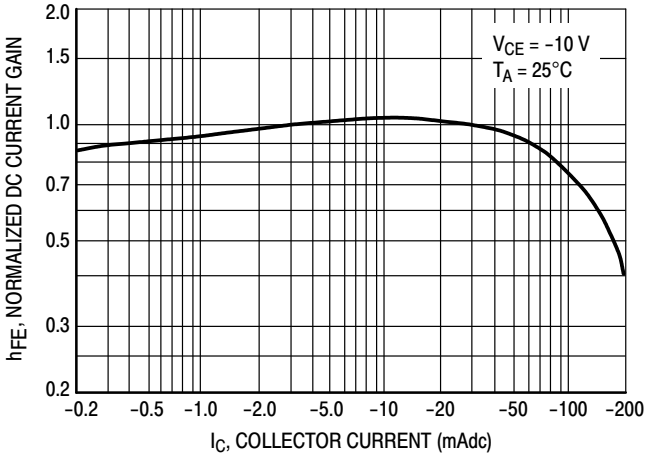


Figure 1. Normalized DC Current Gain

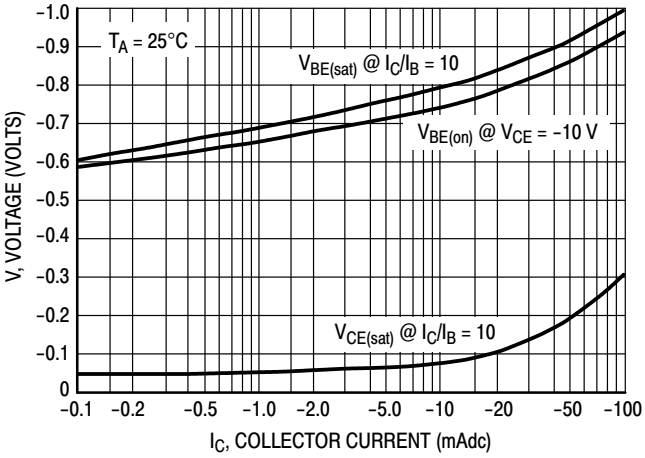


Figure 2. "Saturation" and "On" Voltages

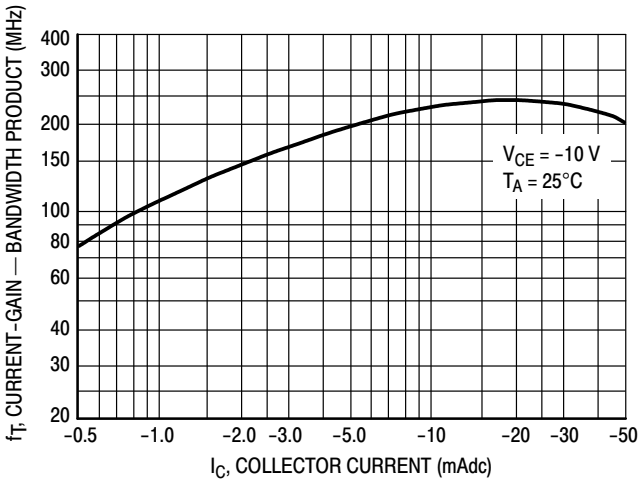


Figure 3. Current−Gain − Bandwidth Product

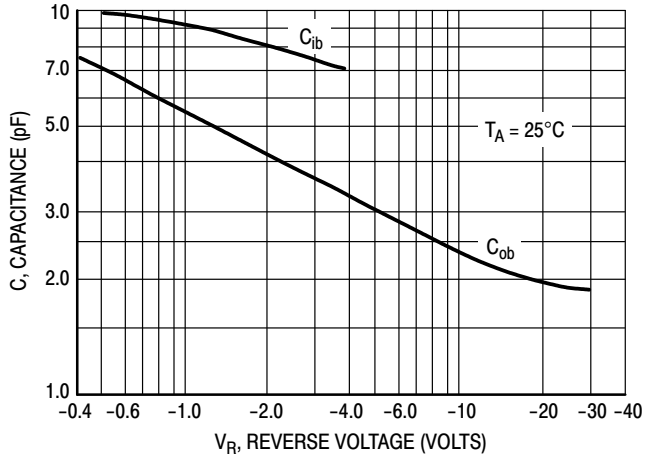


Figure 4. Capacitances

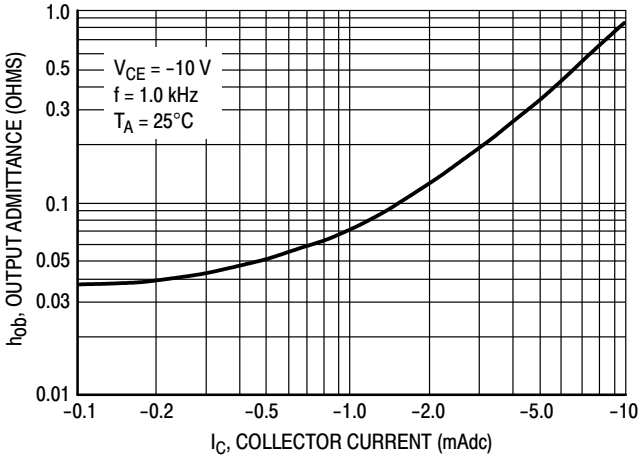


Figure 5. Output Admittance

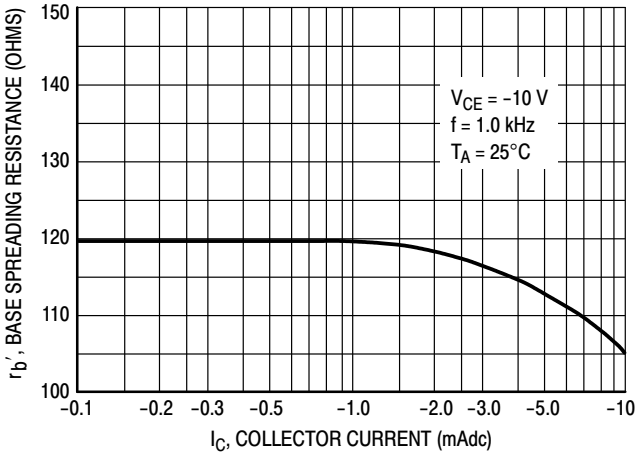


Figure 6. Base Spreading Resistance

TYPICAL ELECTRICAL CHARACTERISTICS – NPN TRANSISTOR

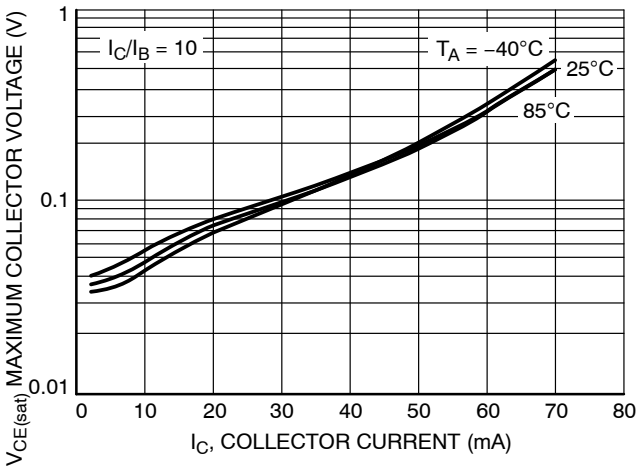


Figure 7. Maximum Collector Voltage versus Collector Current

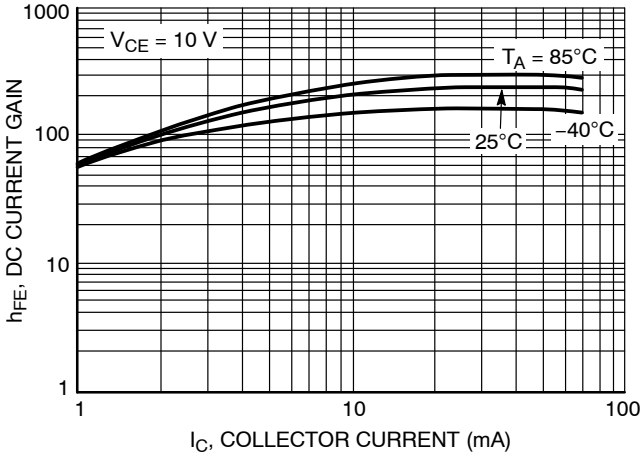


Figure 8. DC Current Gain

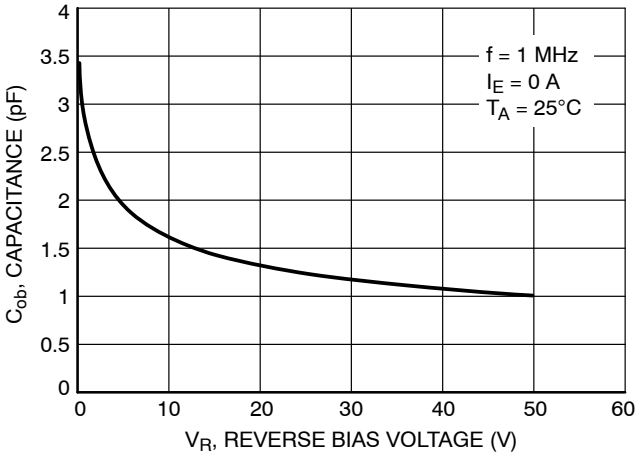


Figure 9. Output Capacitance

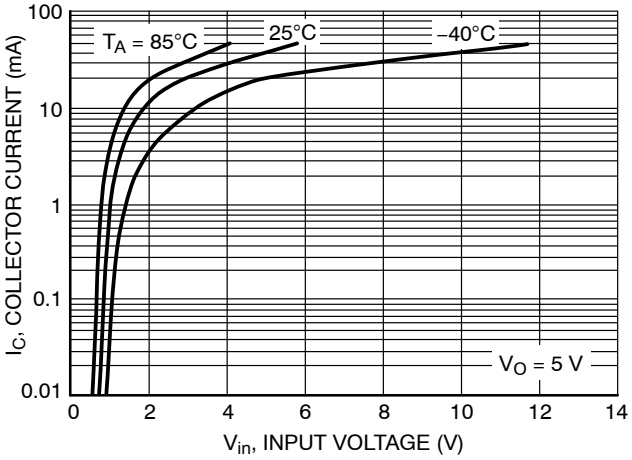


Figure 10. Output Current versus Input Voltage

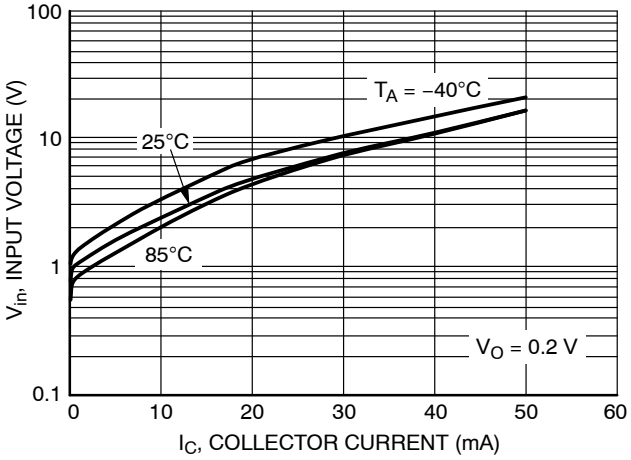
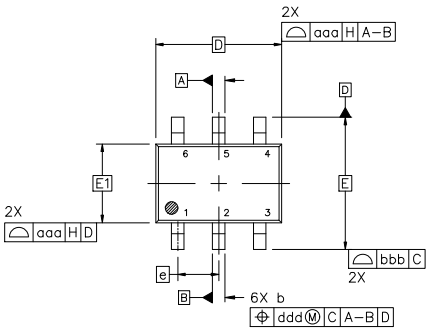


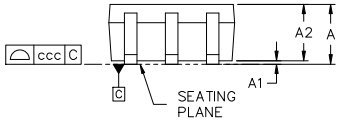
Figure 11. Input Voltage versus Output Current

SC−88 2.00x1.25x0.90, 0.65P
CASE 419B−02
ISSUE Z

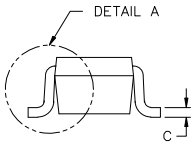
DATE 18 APR 2024



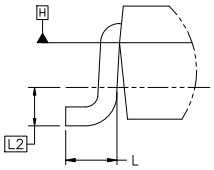
TOP VIEW



SIDE VIEW



END VIEW

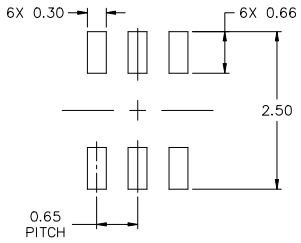


DETAIL A
SCALE 2:1

NOTES:

1. DIMENSIONING AND TOLERANCING CONFORM TO ASME Y14.5−2018.
2. ALL DIMENSION ARE IN MILLIMETERS.
3. DIMENSIONS D AND E1 DO NOT INCLUDE MOLD FLASH, PROTRUSIONS, OR GATE BURRS. MOLD FLASH, PROTRUSIONS, OR GATE BURRS SHALL NOT EXCEED 0.20 PER END.
4. DIMENSIONS D AND E1 AT THE OUTERMOST EXTREMES OF THE PLASTIC BODY AND DATUM H.
5. DATUMS A AND B ARE DETERMINED AT DATUM H.
6. DIMENSIONS b AND c APPLY TO THE FLAT SECTION OF THE LEAD BETWEEN 0.08 AND 0.15 FROM THE TIP.
7. DIMENSION b DOES NOT INCLUDE DAMBAR PROTRUSION. ALLOWABLE DAMBAR PROTRUSION SHALL BE 0.08 TOTAL IN EXCESS OF DIMENSION b AT MAXIMUM MATERIAL CONDITION. THE DAMBAR CANNOT BE LOCATED ON THE LOWER RADIUS OF THE FOOT.

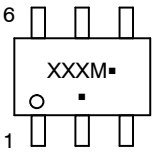
	MILLIMETERS		
DIM	MIN.	NOM.	MAX.
A	−−−	−−−	1.10
A1	0.00	−−−	0.10
A2	0.70	0.90	1.00
b	0.15	0.20	0.25
c	0.08	0.15	0.22
D	2.00 BSC		
E	2.10 BSC		
E1	1.25 BSC		
e	0.65 BSC		
L	0.26	0.36	0.46
L2	0.15 BSC		
aaa	0.15		
bbb	0.30		
ccc	0.10		
ddd	0.10		



RECOMMENDED MOUNTING FOOTPRINT*

* FOR ADDITIONAL INFORMATION ON OUR Pb−FREE STRATEGY AND SOLDERING DETAILS, PLEASE DOWNLOAD THE ONSEMI SOLDERING AND MOUNTING TECHNIQUES REFERENCE MANUAL, SOLDERRM/D.

GENERIC MARKING DIAGRAM*



XXX = Specific Device Code
M = Date Code*
▪ = Pb−Free Package

(Note: Microdot may be in either location)

*Date Code orientation and/or position may vary depending upon manufacturing location.

*This information is generic. Please refer to device data sheet for actual part marking. Pb−Free indicator, “G” or microdot “▪”, may or may not be present. Some products may not follow the Generic Marking.

STYLES ON PAGE 2

DOCUMENT NUMBER:	**98ASB42985B**	Electronic versions are uncontrolled except when accessed directly from the Document Repository. Printed versions are uncontrolled except when stamped “CONTROLLED COPY” in red.	
DESCRIPTION:	**SC−88 2.00x1.25x0.90, 0.65P**		**PAGE 1 OF 2**

SC−88 2.00x1.25x0.90, 0.65P
CASE 419B−02
ISSUE Z

DATE 18 APR 2024

STYLE 1:
PIN 1. EMITTER 2
2. BASE 2
3. COLLECTOR 1
4. EMITTER 1
5. BASE 1
6. COLLECTOR 2

STYLE 2:
CANCELLED

STYLE 3:
CANCELLED

STYLE 4:
PIN 1. CATHODE
2. CATHODE
3. COLLECTOR
4. EMITTER
5. BASE
6. ANODE

STYLE 5:
PIN 1. ANODE
2. ANODE
3. COLLECTOR
4. EMITTER
5. BASE
6. CATHODE

STYLE 6:
PIN 1. ANODE 2
2. N/C
3. CATHODE 1
4. ANODE 1
5. N/C
6. CATHODE 2

STYLE 7:
PIN 1. SOURCE 2
2. DRAIN 2
3. GATE 1
4. SOURCE 1
5. DRAIN 1
6. GATE 2

STYLE 8:
CANCELLED

STYLE 9:
PIN 1. EMITTER 2
2. EMITTER 1
3. COLLECTOR 1
4. BASE 1
5. BASE 2
6. COLLECTOR 2

STYLE 10:
PIN 1. SOURCE 2
2. SOURCE 1
3. GATE 1
4. DRAIN 1
5. DRAIN 2
6. GATE 2

STYLE 11:
PIN 1. CATHODE 2
2. CATHODE 2
3. ANODE 1
4. CATHODE 1
5. CATHODE 1
6. ANODE 2

STYLE 12:
PIN 1. ANODE 2
2. ANODE 2
3. CATHODE 1
4. ANODE 1
5. ANODE 1
6. CATHODE 2

STYLE 13:
PIN 1. ANODE
2. N/C
3. COLLECTOR
4. EMITTER
5. BASE
6. CATHODE

STYLE 14:
PIN 1. VREF
2. GND
3. GND
4. IOUT
5. VEN
6. VCC

STYLE 15:
PIN 1. ANODE 1
2. ANODE 2
3. ANODE 3
4. CATHODE 3
5. CATHODE 2
6. CATHODE 1

STYLE 16:
PIN 1. BASE 1
2. EMITTER 2
3. COLLECTOR 2
4. BASE 2
5. EMITTER 1
6. COLLECTOR 1

STYLE 17:
PIN 1. BASE 1
2. EMITTER 1
3. COLLECTOR 2
4. BASE 2
5. EMITTER 2
6. COLLECTOR 1

STYLE 18:
PIN 1. VIN1
2. VCC
3. VOUT2
4. VIN2
5. GND
6. VOUT1

STYLE 19:
PIN 1. I OUT
2. GND
3. GND
4. V CC
5. V EN
6. V REF

STYLE 20:
PIN 1. COLLECTOR
2. COLLECTOR
3. BASE
4. EMITTER
5. COLLECTOR
6. COLLECTOR

STYLE 21:
PIN 1. ANODE 1
2. N/C
3. ANODE 2
4. CATHODE 2
5. N/C
6. CATHODE 1

STYLE 22:
PIN 1. D1 (i)
2. GND
3. D2 (i)
4. D2 (c)
5. VBUS
6. D1 (c)

STYLE 23:
PIN 1. Vn
2. CH1
3. Vp
4. N/C
5. CH2
6. N/C

STYLE 24:
PIN 1. CATHODE
2. ANODE
3. CATHODE
4. CATHODE
5. CATHODE
6. CATHODE

STYLE 25:
PIN 1. BASE 1
2. CATHODE
3. COLLECTOR 2
4. BASE 2
5. EMITTER
6. COLLECTOR 1

STYLE 26:
PIN 1. SOURCE 1
2. GATE 1
3. DRAIN 2
4. SOURCE 2
5. GATE 2
6. DRAIN 1

STYLE 27:
PIN 1. BASE 2
2. BASE 1
3. COLLECTOR 1
4. EMITTER 1
5. EMITTER 2
6. COLLECTOR 2

STYLE 28:
PIN 1. DRAIN
2. DRAIN
3. GATE
4. SOURCE
5. DRAIN
6. DRAIN

STYLE 29:
PIN 1. ANODE
2. ANODE
3. COLLECTOR
4. EMITTER
5. BASE/ANODE
6. CATHODE

STYLE 30:
PIN 1. SOURCE 1
2. DRAIN 2
3. DRAIN 2
4. SOURCE 2
5. GATE 1
6. DRAIN 1

Note: Please refer to datasheet for style callout. If style type is not called out in the datasheet refer to the device datasheet pinout or pin assignment.

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DESCRIPTION:	**SC−88 2.00x1.25x0.90, 0.65P**		**PAGE 2 OF 2**

ADDITIONAL INFORMATION

TECHNICAL PUBLICATIONS:
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