Three Phase Inverter Automotive Power MOSFET Module

NXV08V110DB1

ON Semiconductor®

www.onsemi.com

Features

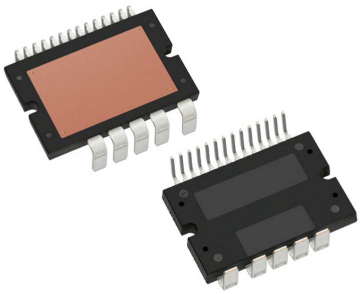
- Three−Phase Inverter Bridge for Variable Speed Motor Drive
- RC Snubber for Low EMI
- Current Sensing and Temperature Sensing
- Electrically Isolated DBC Substrate for Low Thermal Resistance
- Compact Design for Low Total Module Resistance
- Module Serialization for Full Traceability
- AEC Qualified − AQG324
- PPAP Capable
- This Device is Pb−free, RoHS and UL94−V0 Compliant

Applications

- 24 V and 48 V Motor Control
- DC−DC Converter

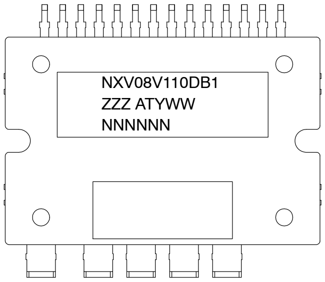
Benefits

- Enable Design of Small, Efficient and Reliable System for Reduced Vehicle Fuel Consumption and CO_2 Emission
- Simplified Vehicle Assembly
- Enable Low Thermal Resistance to Junction−to−Heat Sink by Direct Mounting via Thermal Interface Material between Module Case and Heat Sink



19LD, APM, PDD STD
CASE MODCD

MARKING DIAGRAM



NXV08V110DB1 = Specific Device Code
ZZZ = Lot ID
AT = Assembly & Test Location
Y = Year
WW = Work Week
NNN = Serial Number

ORDERING INFORMATION

See detailed ordering and shipping information on page 2 of this data sheet.

October, 2019 − Rev. 0

PACKAGE MARKING AND ORDERING INFORMATION

Part Number	Package	Pb−Free and RoHS Compliant	Operating Temperature Range	Packing Method
NXV08V110DB1	APM19−CBC	yes	−40 ~ 125°C	Tube

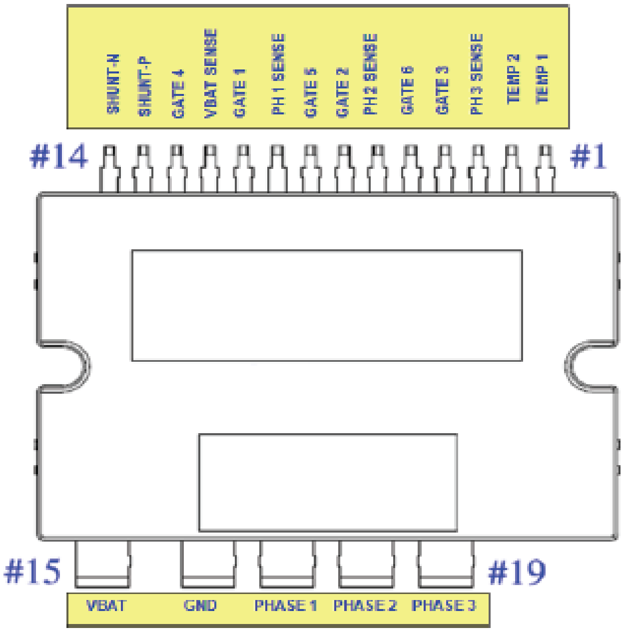


Figure 1. Pin Configuration

PIN DESCRIPTION

Pin Number	Pin Name	Pin Description
1	TEMP 1	NTC Thermistor Terminal 1
2	TEMP 2	NTC Thermistor Terminal 2
3	PHASE 3 SENSE	Source of Q3 and Drain of Q6
4	GATE 3	Gate of Q3, high side Phase 3 MOSFET
5	GATE 6	Gate of Q6, low side Phase 3 MOSFET
6	PHASE 2 SENSE	Source of Q2 and Drain of Q5
7	GATE 2	Gate of Q2, high side Phase 2 MOSFET
8	GATE 5	Gate of Q5, low side Phase 2 MOSFET
9	PHASE 1 SENSE	Source of Q1 and Drain of Q4
10	GATE 1	Gate of Q2, high side Phase 1 MOSFET
11	VBAT SENSE	Sense pin for battery voltage and Drain of high side MOSFETs
12	GATE 4	Gate of Q4, low side Phase 1 MOSFET
13	SHUNT P	Positive CSR sense pin and source connection for low side MOSFETs
14	SHUNT N	Negative CSR sense pin and sense pin for battery return
15	VBAT	Battery voltage power lead
16	GND	Battery return power lead
17	PHASE 1	Phase 1 power lead
18	PHASE 2	Phase 2 power lead
19	PHASE 3	Phase 3 power lead

Schematic Diagram

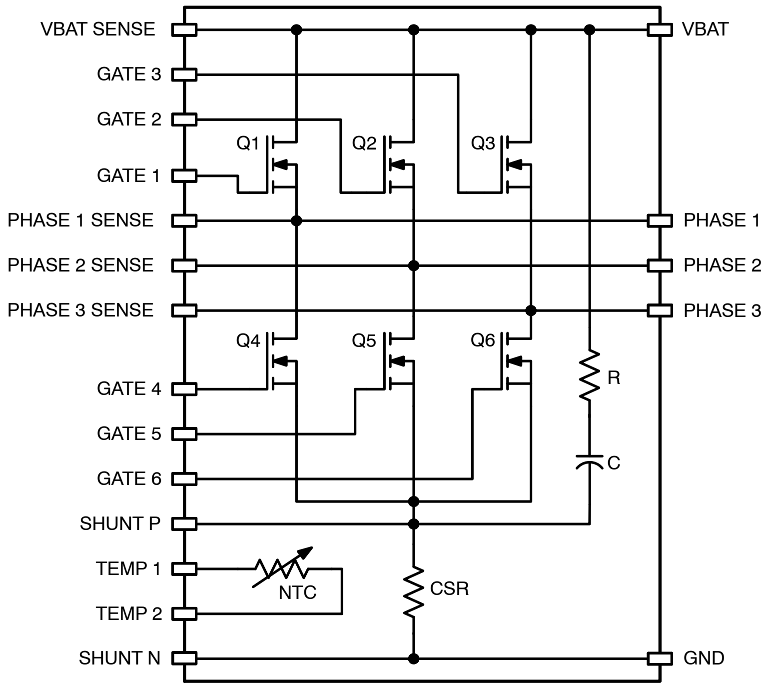


Figure 2. Schematic

Flammability Information

All materials present in the power module meet UL flammability rating class 94V−0.

Compliance to RoHS Directives

The power module is 100% lead free and RoHS compliant 2000/53/C directive.

Solder

Solder used is a lead free SnAgCu alloy.

Base of the leads, at the interface with the package body should not be exposed to more than 200°C during mounting on the PCB, this to prevent the remelt of the solder joints.

ABSOLUTE MAXIMUM RATINGS (T_J = 25°C unless otherwise specified)

Symbol	Parameter	Max.	Unit
VDS(Q1~Q6)	Drain to Source Voltage	80	V
VGS(Q1~Q6)	Gate to Source Voltage	±20	V
EAS(Q1~Q6)	Single Pulse Avalanche Energy (Note 2)	324	mJ
T_J	Maximum Junction Temperature	175	°C
T_{STG}	Storage Temperature	125	°C
T_{lead}	Temperature at the base of the leads at the interface with the package body during PCB mounting	200	°C
V_{ISO}	Isolation Voltage (60Hz, Sinusoidal, AC 1minute, Connection Pins to heat sink plate)	2500	Vrms

Stresses exceeding those listed in the Maximum Ratings table may damage the device. If any of these limits are exceeded, device functionality should not be assumed, damage may occur and reliability may be affected.

1. Defined by design, not subject to production testing.
2. Starting T_J = 25°C, L = 0.08 mH, I_{AS} = 90 A, V_{DD} = 80 V during inductor charging and V_{DD} = 0 V during time in avalanche.

THERMAL CHARACTERISTICS

Symbol	Parameter	Min.	Typ.	Max.	Unit
$R_{\theta JC}$	Thermal Resistance, Junction−to−Case (Note 3)	–	–	0.9	K/W

3. Test method compliant with MIL−STD−883−1012.1, case temperature measured below the package at the chip center. Cosmetic oxidation and discolor on the DBC surface is allowed.

MODULE SPECIFIC CHARACTERISTICS

Parameters	Test Conditions	Symbol	Min.	Typ.	Max.	Unit
Drain−to−Source Breakdown Voltage	ID = 250 μA, VGS = 0 V	BVDSS	80			V
Gate to Source Threshold Voltage	VGS = VDS, ID = 250 μA	VGS(th)	2		4	V
Gate−to−Source Leakage Current	VGS = ±20 V, VDS = 0 V	IGSS	−100		+100	nA
Drain−to−Source Leakage Current	VDS = 80 V, VGS = 0 V	IDSS			2	uA
Source−to−Drain Diode Voltage	ISD = 80 A, VGS = 0 V	VSD			1.25	V
Q1 Inverter High Side MOSFETs (See Note 4)	I_D = 80 A, V_{GS} = 10 V (Note 4)	RDS(ON)Q1		1.3	1.7	mΩ
Q2 Inverter High Side MOSFETs (See Note 4)		RDS(ON)Q2		1.4	1.8	mΩ
Q3 Inverter High Side MOSFETs (See Note 4)		RDS(ON)Q3		1.5	1.9	mΩ
Q4 Inverter Low Side MOSFETs (See Note 4)		RDS(ON)Q4		1.6	1.9	mΩ
Q5 Inverter Low Side MOSFETs (See Note 4)		RDS(ON)Q5		1.7	2.1	mΩ
Q6 Inverter Low Side MOSFETs (See Note 4)		RDS(ON)Q6		2.0	2.4	mΩ
VBAT to PHASE 1	I_D = 80 A, V_{GS} = 10 V	$R_{DS(ON)MQ1}$		2.2	2.6	mΩ
VBAT to PHASE 2		$R_{DS(ON)MQ2}$		2.3	2.6	mΩ
VBAT to PHASE 3		$R_{DS(ON)MQ3}$		2.4	2.6	mΩ
PHASE1 to GND		$R_{DS(ON)MQ4}$		2.4	3.0	mΩ
PHASE2 to GND		$R_{DS(ON)MQ5}$		2.6	3.0	mΩ
PHASE3 to GND		$R_{DS(ON)MQ6}$		2.9	3.2	mΩ
Total loop resistance B+ ≥ Phase ≥ GND	V_{GS} = 10 V, I_D = 80 A			4.9	7.3	mΩ

4. All MOSFETs have same size and on resistance. However, the different values listed due to the different access points available inside the module for on resistance measurement. Q1 has the shortest measurement path in the layout, in this reason, on resistance of Q1 can be used for simple power loss calculation.

COMPONENTS

Symbol	Spec	Quantity	Size
RESISTOR	1.0 Ω	1	142 × 55 mil
CAPACITOR	100 V, 0.022 uF	1	79 × 49 mil
CURRENT SENSING RESISTOR	0.5 mΩ	1	250 × 120 mil
NTC	NCP18XH103F0SRB, 10 kΩ	1	63 × 32 mil

ELECTRICAL CHARACTERISTICS

(T_J = 25°C unless otherwise noted, Reference typical characteristics of FDBL86363−F085, TOLL)

Symbol	Parameter	Test Conditions	Min.	Typ.	Max.	Unit
DYNAMIC CHARACTERISTICS						
C_{iss}	Input Capacitance	V_{DS} = 40 V, V_{GS} = 0 V, f = 1 MHz	–	10000	–	pF
C_{oss}	Output Capacitance		–	1540	–	pF
C_{rss}	Reverse Transfer Capacitance		–	70	–	pF
R_g	Gate Resistance	f = 1 MHz	–	2.8	–	Ω
$Q_{g(ToT)}$	Total Gate Charge at 10 V	V_{GS} = 0 to 10 V V_{DD} = 40 V, I_D = 80 A	–	130	169	nC
$Q_{g(th)}$	Threshold Gate Charge	V_{GS} = 0 to 2 V	–	18	27	nC
Q_{gs}	Gate−to−Source Gate Charge		–	47	–	nC
Q_{gd}	Gate−to−Drain “Miller” Charge		–	24	–	nC

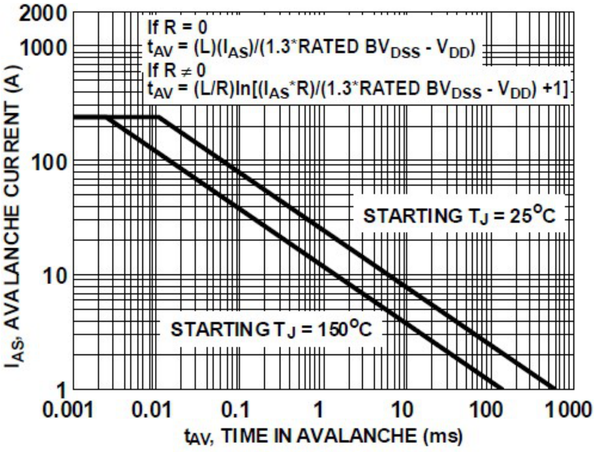
ELECTRICAL CHARACTERISTICS (continued)
(T_J = 25°C unless otherwise noted, Reference typical characteristics of FDBL86363−F085, TOLL)

Symbol	Parameter	Test Conditions	Min.	Typ.	Max.	Unit
SWITCHING CHARACTERISTICS						
t_{on}	Turn−On Time	V_{DD} = 40 V, I_D = 80 A, V_{GS} = 10 V, R_{GEN} = 6 Ω	–	–	133	ns
$t_{d(on)}$	Turn−On Delay		–	39	–	ns
t_r	Rise Time		–	63	–	ns
$t_{d(off)}$	Turn−Off Delay		–	61	–	ns
t_f	Fall Time		–	33	–	ns
t_{off}	Turn−Off Time		–	–	140	ns

Product parametric performance is indicated in the Electrical Characteristics for the listed test conditions, unless otherwise noted. Product performance may not be indicated by the Electrical Characteristics if operated under different conditions.

TYPICAL CHARACTERISTICS

(Graphs are generated using the die assembled in discrete package for reference purposes only. Datasheet of FDBL86363−F085 is available in the web)



NOTE: Refer to ON Semiconductor Application Notes AN7514 and AN7515.

Figure 3. Unclamped Inductive Switching Capability

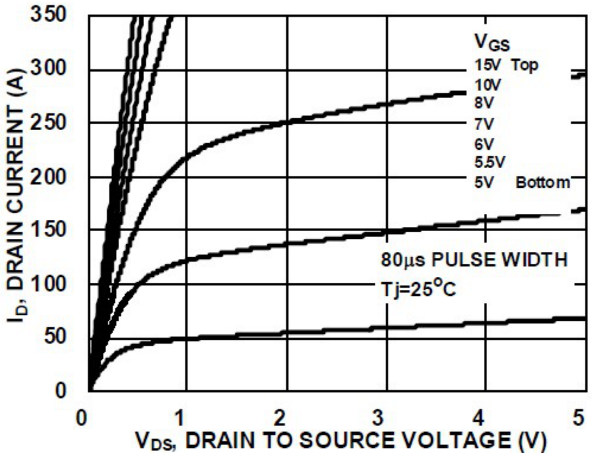


Figure 4. Saturation Characteristics

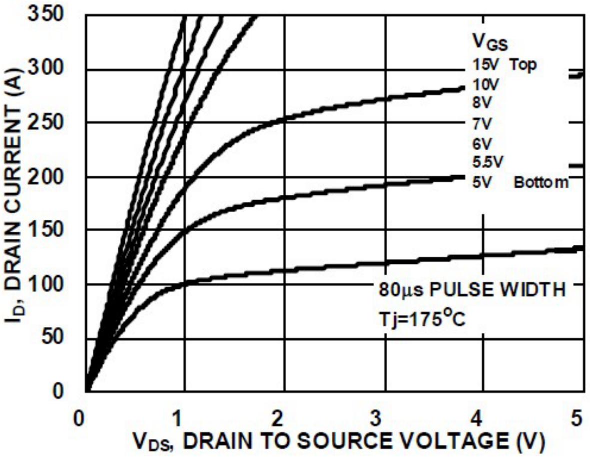


Figure 5. Saturation Characteristics

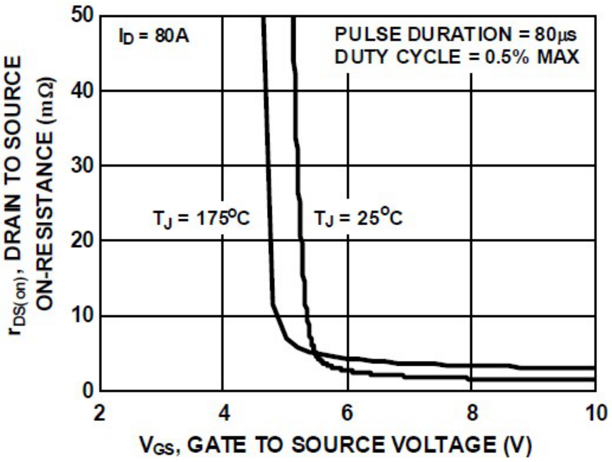


Figure 6. R_{DSON} vs. Gate Voltage

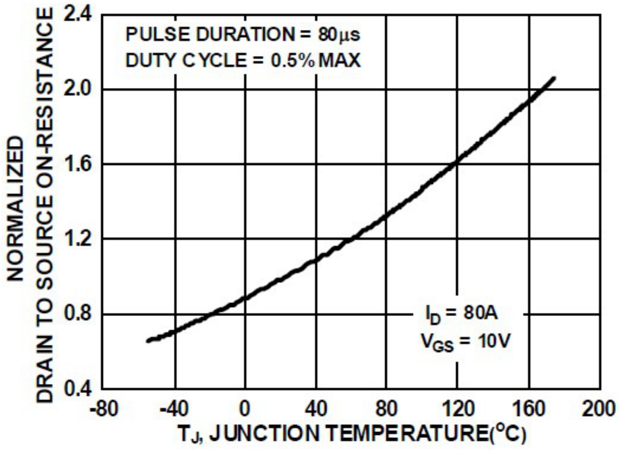


Figure 7. Normalized R_{DSON} vs. Junction Temperature

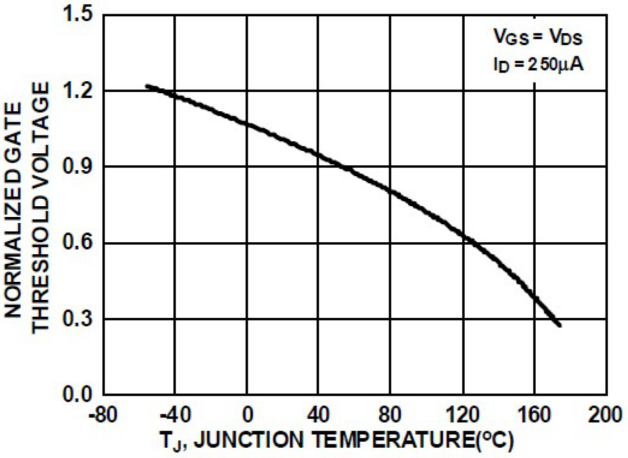


Figure 8. Normalized Gate Threshold Voltage vs. Temperature

TYPICAL CHARACTERISTICS (continued)

(Graphs are generated using the die assembled in discrete package for reference purposes only. Datasheet of FDBL86363−F085 is available in the web)

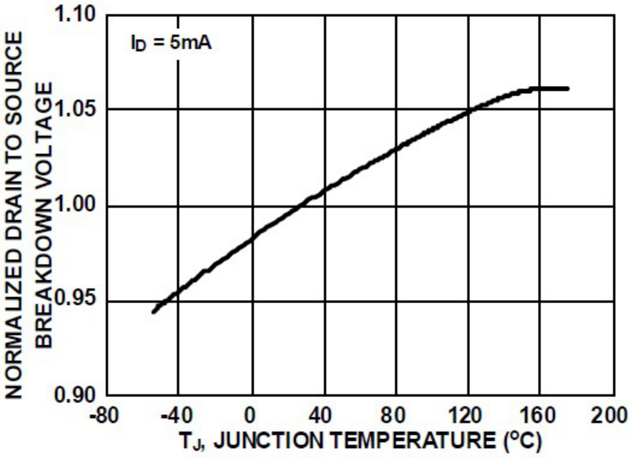


Figure 9. Normalized Drain to Source Breakdown Voltage vs. Junction Temperature

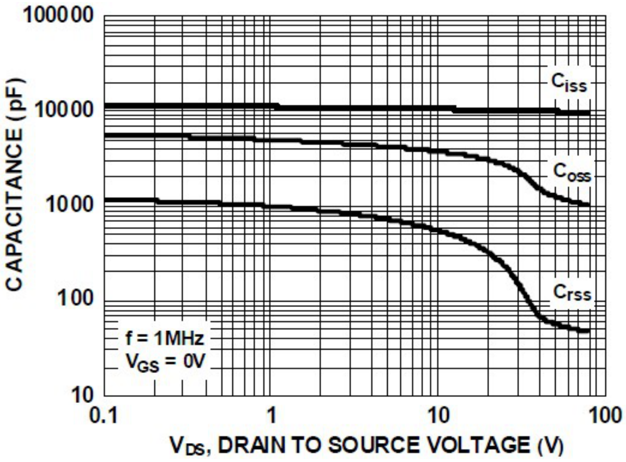


Figure 10. Capacitance vs. Drain to Source Voltage

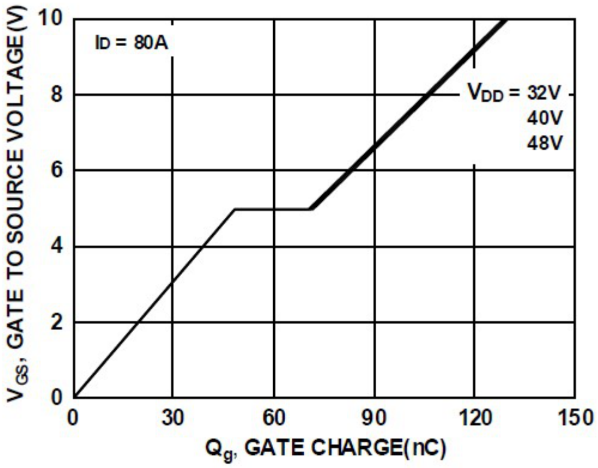


Figure 11. Gate Charge vs. Gate to Source Voltage

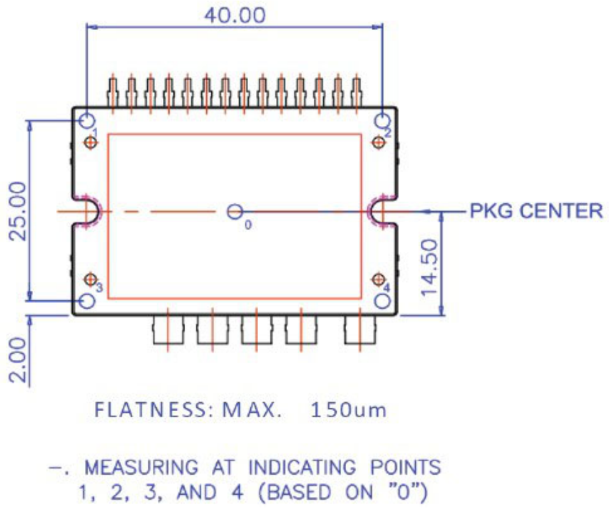


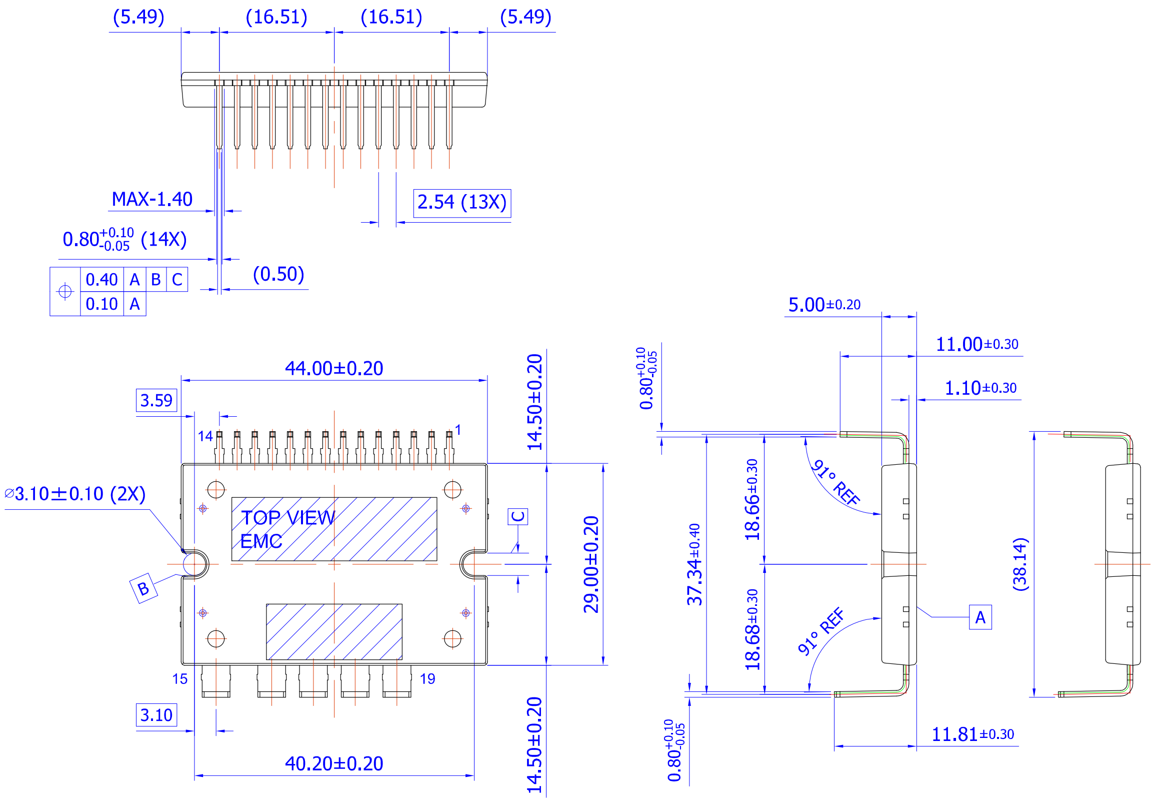
Figure 12. Flatness Measurement Position

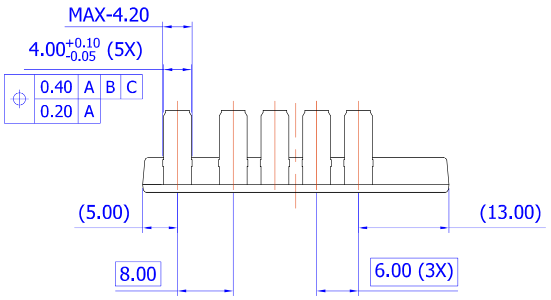
MECHANICAL CHARACTERISTICS AND RATINGS

Parameter	Test Conditions	Min.	Typ.	Max.	Units
Device Flatness	Refer to the package dimensions	0	–	150	um
Mounting Torque	Mounting screw: M3, recommended 0.7 N•m	0.4	–	0.8	N•m
Weight		–	20	–	g

19LD, APM, PDD STD (APM19−CBC)
CASE MODCD
ISSUE O

DATE 30 NOV 2016





NOTES: UNLESS OTHERWISE SPECIFIED
- A) THIS PACKAGE DOES NOT COMPLY TO ANY CURRENT PACKAGING STANDARD
- B) ALL DIMENSIONS ARE IN MILLIMETERS
- C) DIMENSIONS ARE EXCLUSIVE OF BURRS, MOLD FLASH, AND TIE BAR EXTRUSIONS
- D) ( ) IS REFERENCE

DOCUMENT NUMBER:	**98AON13505G**	Electronic versions are uncontrolled except when accessed directly from the Document Repository. Printed versions are uncontrolled except when stamped “CONTROLLED COPY” in red.
DESCRIPTION:	**19LD, APM, PDD STD (APM19−CBC)**	**PAGE 1 OF 1**

onsemi, onsemi, , and other names, marks, and brands are registered and/or common law trademarks of Semiconductor Components Industries, LLC dba "**onsemi**" or its affiliates and/or subsidiaries in the United States and/or other countries. **onsemi** owns the rights to a number of patents, trademarks, copyrights, trade secrets, and other intellectual property. A listing of **onsemi**'s product/patent coverage may be accessed at www.onsemi.com/site/pdf/Patent−Marking.pdf. **onsemi** reserves the right to make changes at any time to any products or information herein, without notice. The information herein is provided "as−is" and **onsemi** makes no warranty, representation or guarantee regarding the accuracy of the information, product features, availability, functionality, or suitability of its products for any particular purpose, nor does **onsemi** assume any liability arising out of the application or use of any product or circuit, and specifically disclaims any and all liability, including without limitation special, consequential or incidental damages. Buyer is responsible for its products and applications using **onsemi** products, including compliance with all laws, regulations and safety requirements or standards, regardless of any support or applications information provided by **onsemi**. "Typical" parameters which may be provided in **onsemi** data sheets and/or specifications can and do vary in different applications and actual performance may vary over time. All operating parameters, including "Typicals" must be validated for each customer application by customer's technical experts. **onsemi** does not convey any license under any of its intellectual property rights nor the rights of others. **onsemi** products are not designed, intended, or authorized for use as a critical component in life support systems or any FDA Class 3 medical devices or medical devices with a same or similar classification in a foreign jurisdiction or any devices intended for implantation in the human body. Should Buyer purchase or use **onsemi** products for any such unintended or unauthorized application, Buyer shall indemnify and hold **onsemi** and its officers, employees, subsidiaries, affiliates, and distributors harmless against all claims, costs, damages, and expenses, and reasonable attorney fees arising out of, directly or indirectly, any claim of personal injury or death associated with such unintended or unauthorized use, even if such claim alleges that **onsemi** was negligent regarding the design or manufacture of the part. **onsemi** is an Equal Opportunity/Affirmative Action Employer. This literature is subject to all applicable copyright laws and is not for resale in any manner.

ADDITIONAL INFORMATION

TECHNICAL PUBLICATIONS:
Technical Library: www.onsemi.com/design/resources/technical−documentation
onsemi Website: www.onsemi.com

ONLINE SUPPORT: www.onsemi.com/support
For additional information, please contact your local Sales Representative at
www.onsemi.com/support/sales