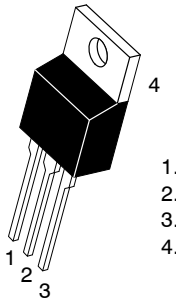
Complementary Silicon Transistors, Plastic, Medium-Power

TIP100, TIP101, TIP102 (NPN); TIP105, TIP106, TIP107 (PNP)

Designed for general−purpose amplifier and low−speed switching applications.



1. Base
2. Collector
3. Emitter
4. Collector

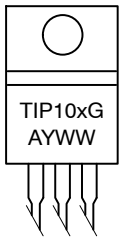
TO−220AB
CASE 221A
STYLE 1

DARLINGTON 8 AMPERE COMPLEMENTARY SILICON POWER TRANSISTORS 60−80−100 VOLTS, 80 WATTS

Features

- High DC Current Gain −
  h_{FE} = 2500 (Typ) @ I_C = 4.0 Adc
- Collector−Emitter Sustaining Voltage − @ 30 mAdc
  $V_{CEO(sus)}$ = 60 Vdc (Min) − TIP100, TIP105
  = 80 Vdc (Min) − TIP101, TIP106
  = 100 Vdc (Min) − TIP102, TIP107
- Low Collector−Emitter Saturation Voltage −
  $V_{CE(sat)}$ = 2.0 Vdc (Max) @ I_C = 3.0 Adc
  = 2.5 Vdc (Max) @ I_C = 8.0 Adc
- Monolithic Construction with Built−in Base−Emitter Shunt Resistors
- These Devices are Pb−Free and are RoHS Compliant

MARKINGDIAGRAM



TIP10x	= Device Code
x	= 0, 1, 2, 5, 6, or 7
A	= Assembly Location
Y	= Year
WW	= Work Week
G	= Pb−Free Package

ORDERING INFORMATION

See detailed ordering and shipping information on page 7 of this data sheet.

MAXIMUM RATINGS

Symbol	Rating	TIP100, TIP105	TIP101, TIP106	TIP102, TIP107	Unit
V_{CEO}	Collector – Emitter Voltage	60	80	100	Vdc
V_{CB}	Collector – Base Voltage	60	80	100	Vdc
V_{EB}	Emitter – Base Voltage		5.0		Vdc
I_C	Collector Current – Continuous – Peak		8.0 15		Adc
I_B	Base Current		1.0		Adc
P_D	Total Power Dissipation @ T_C = 25°C Derate above 25°C		80 0.64		W W/°C
E	Unclamped Inductive Load Energy (Note 1)		30		mJ
P_D	Total Power Dissipation @ T_A = 25°C Derate above 25°C		2.0 0.016		W W/°C
T_J, T_{stg}	Operating and Storage Junction Temperature Range		−65 to +150		°C

Stresses exceeding those listed in the Maximum Ratings table may damage the device. If any of these limits are exceeded, device functionality should not be assumed, damage may occur and reliability may be affected.

THERMAL CHARACTERISTICS

Symbol	Characteristic	Max	Unit
$R_{\theta JC}$	Thermal Resistance, Junction−to−Case	1.56	°C/W
$R_{\theta JA}$	Thermal Resistance, Junction−to−Ambient	62.5	°C/W

1. I_C = 1.1 A, L = 50 mH, P.R.F. = 10 Hz, V_{CC} = 20 V, R_{BE} = 100 Ω

ELECTRICAL CHARACTERISTICS (T_C = 25°C unless otherwise noted)

Symbol	Characteristic		Min	Max	Unit
OFF CHARACTERISTICS					
$V_{CEO(sus)}$	Collector−Emitter Sustaining Voltage (Note 1) (I_C = 30 mAdc, I_B = 0)	TIP100, TIP105 TIP101, TIP106 TIP102, TIP107	60 80 100	– – –	Vdc
I_{CEO}	Collector Cutoff Current (V_{CE} = 30 Vdc, I_B = 0) (V_{CE} = 40 Vdc, I_B = 0) (V_{CE} = 50 Vdc, I_B = 0)	 TIP100, TIP105 TIP101, TIP106 TIP102, TIP107	 – – –	 50 50 50	μAdc
I_{CBO}	Collector Cutoff Current (V_{CB} = 60 Vdc, I_E = 0) (V_{CB} = 80 Vdc, I_E = 0) (V_{CB} = 100 Vdc, I_E = 0)	 TIP100, TIP105 TIP101, TIP106 TIP102, TIP107	 – – –	 50 50 50	μAdc
I_{EBO}	Emitter Cutoff Current (V_{BE} = 5.0 Vdc, I_C = 0)		–	8.0	mAdc
ON CHARACTERISTICS (Note 1)					
h_{FE}	DC Current Gain (I_C = 3.0 Adc, V_{CE} = 4.0 Vdc) (I_C = 8.0 Adc, V_{CE} = 4.0 Vdc)		 1000 200	 20,000 –	–
$V_{CE(sat)}$	Collector−Emitter Saturation Voltage (I_C = 3.0 Adc, I_B = 6.0 mAdc) (I_C = 8.0 Adc, I_B = 80 mAdc)		 – –	 2.0 2.5	Vdc
$V_{BE(on)}$	Base−Emitter On Voltage (I_C = 8.0 Adc, V_{CE} = 4.0 Vdc)		–	2.8	Vdc
DYNAMIC CHARACTERISTICS					
h_{fe}	Small−Signal Current Gain (I_C = 3.0 Adc, V_{CE} = 4.0 Vdc, f = 1.0 MHz)		4.0	–	–
C_{ob}	Output Capacitance (V_{CB} = 10 Vdc, I_E = 0, f = 0.1 MHz)	TIP105, TIP106, TIP107 TIP100, TIP101, TIP102	– –	300 200	pF

Product parametric performance is indicated in the Electrical Characteristics for the listed test conditions, unless otherwise noted. Product performance may not be indicated by the Electrical Characteristics if operated under different conditions.

2. Pulse Test: Pulse Width ≤ 300 μs, Duty Cycle ≤ 2%.

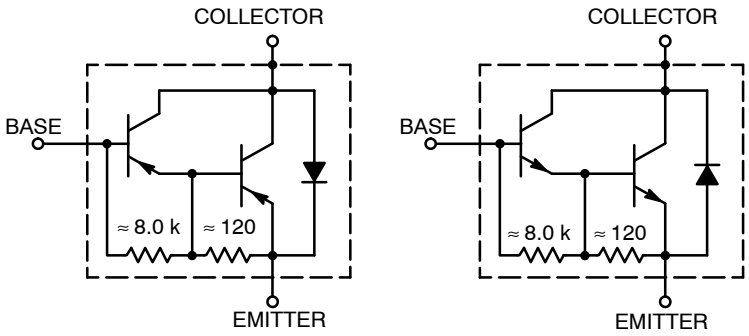


Figure 1. Darlington Circuit Schematic

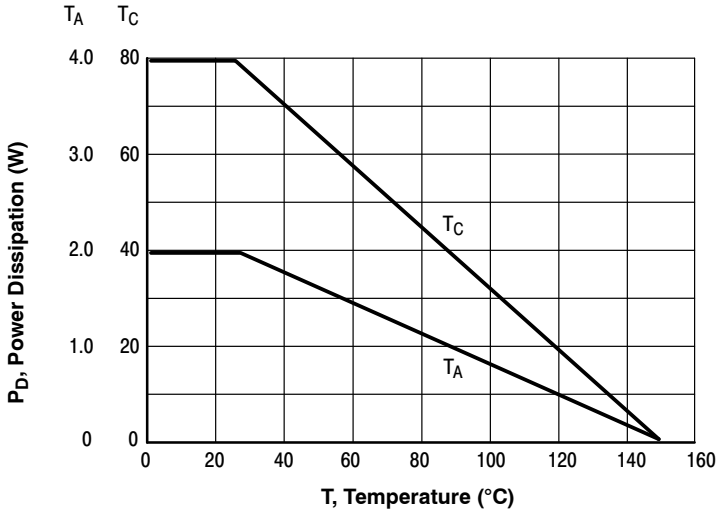


Figure 2. Power Derating

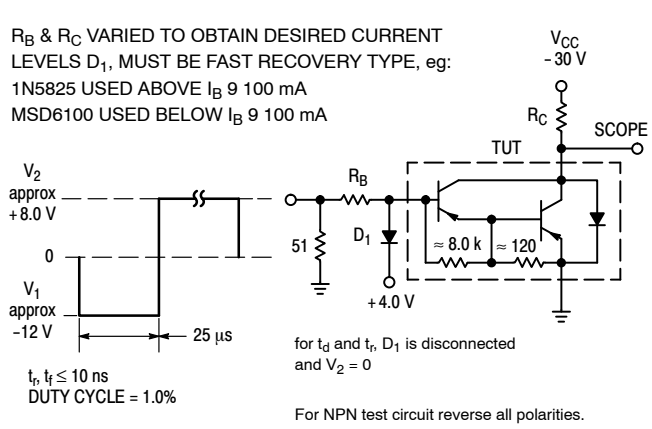


Figure 3. Switching Times Test Circuit

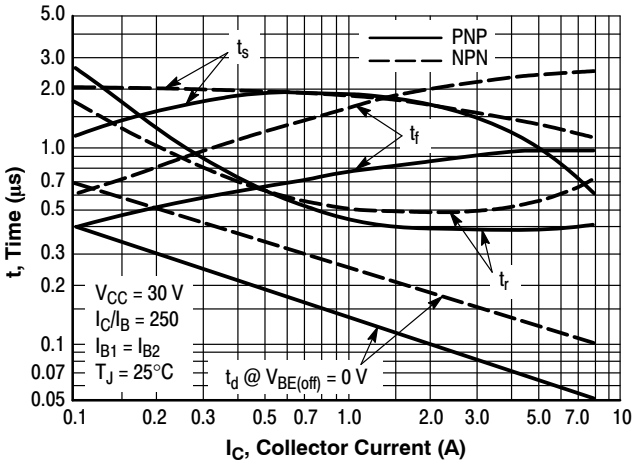


Figure 4. Switching Times

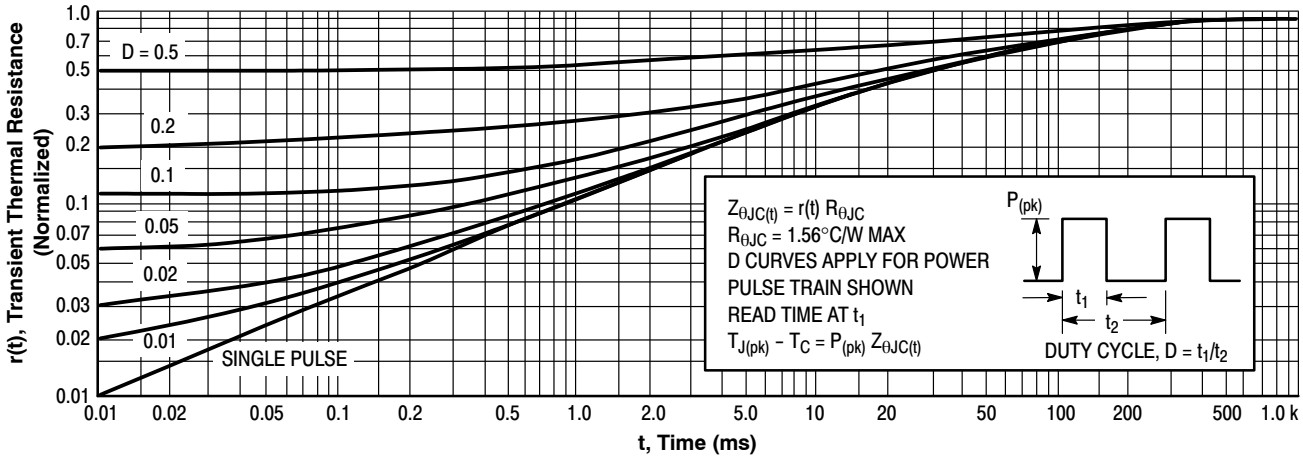


Figure 5. Thermal Response

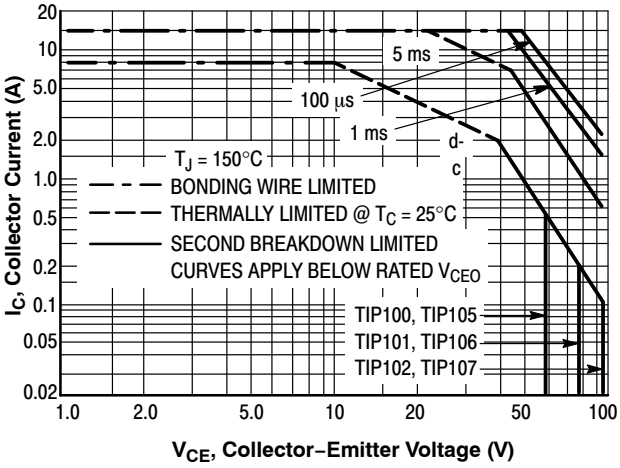


Figure 6. Active−Region Safe Operating Area

There are two limitations on the power handling ability of a transistor: average junction temperature and second breakdown. Safe operating area curves indicate $I_C - V_{CE}$ limits of the transistor that must be observed for reliable operation; i.e., the transistor must not be subjected to greater dissipation than the curves indicate.

The data of Figure 6 is based on $T_{J(pk)}$ = 150°C; T_C is variable depending on conditions. Second breakdown pulse limits are valid for duty cycles to 10% provided $T_{J(pk)}$ < 150°C. $T_{J(pk)}$ may be calculated from the data in Figure 5. At high case temperatures, thermal limitations will reduce the power that can be handled to values less than the limitations imposed by second breakdown

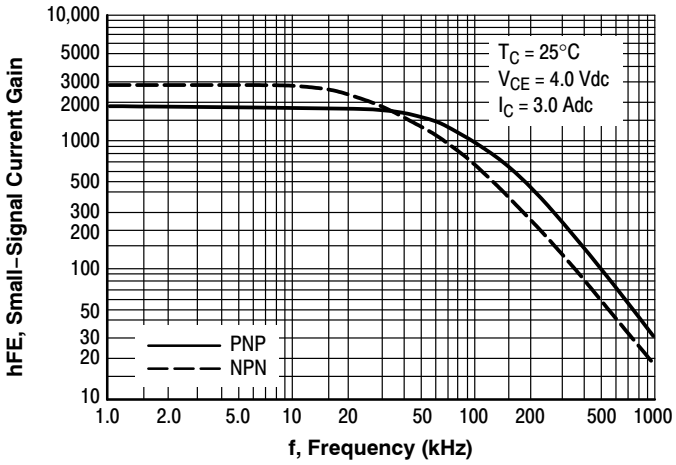


Figure 7. Small−Signal Current Gain

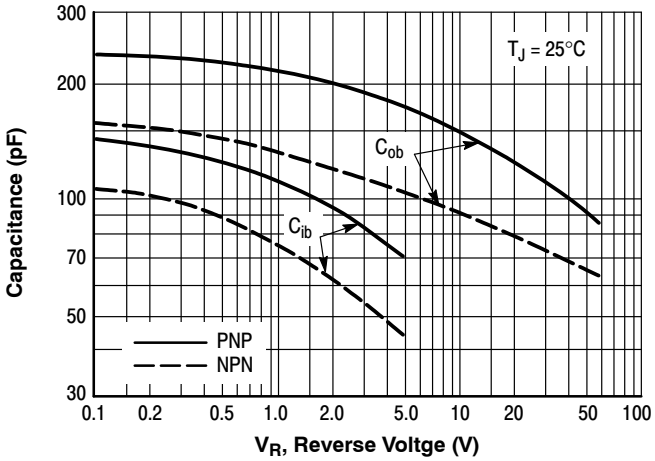


Figure 8. Capacitance

NPN
TIP100, TIP101, TIP102

PNP
TIP105, TIP106, TIP107

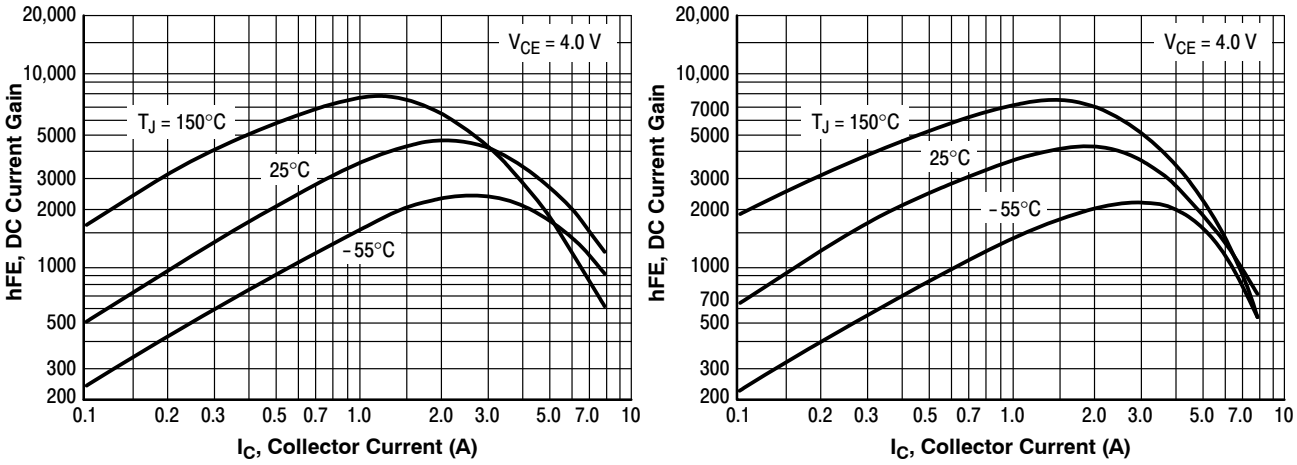


Figure 9. DC Current Gain

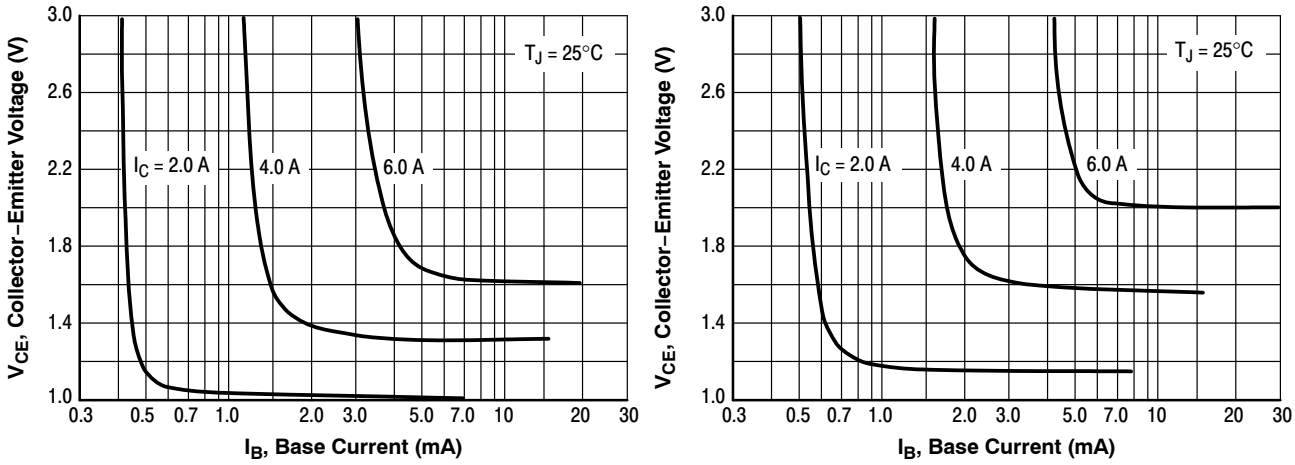


Figure 10. Collector Saturation Region

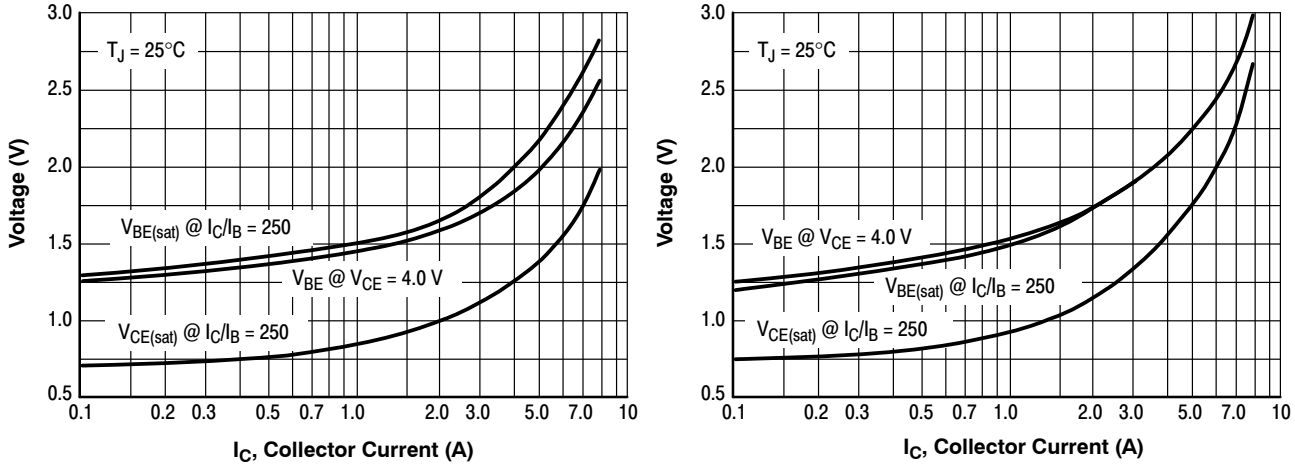
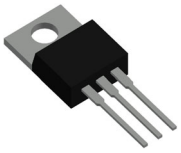


Figure 11. “On” Voltages

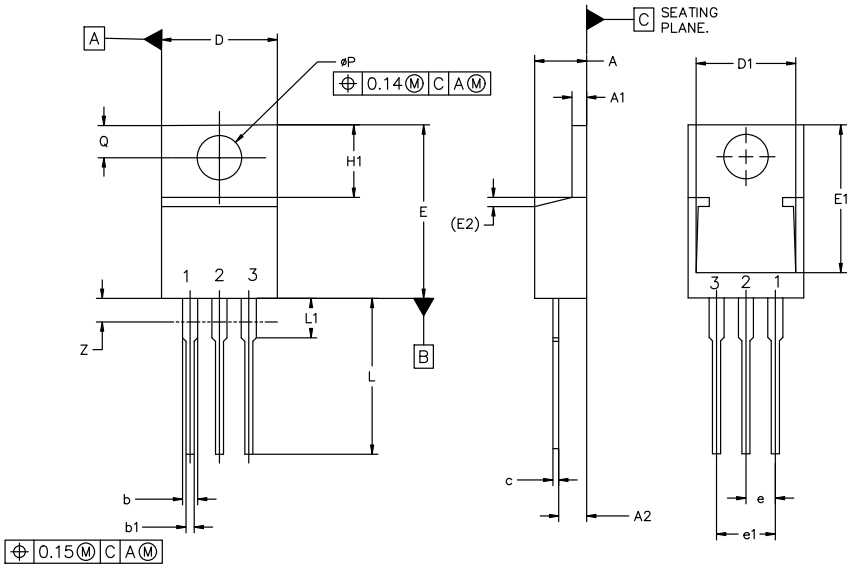
ORDERING INFORMATION

Device	Package	Shipping
TIP100	TO−220	50 Units / Rail
TIP100G	TO−220 (Pb−Free)	50 Units / Rail
TIP101	TO−220	50 Units / Rail
TIP101G	TO−220 (Pb−Free)	50 Units / Rail
TIP102	TO−220	50 Units / Rail
TIP102G	TO−220 (Pb−Free)	50 Units / Rail
TIP105	TO−220	50 Units / Rail
TIP105G	TO−220 (Pb−Free)	50 Units / Rail
TIP106	TO−220	50 Units / Rail
TIP106G	TO−220 (Pb−Free)	50 Units / Rail
TIP107	TO−220	50 Units / Rail
TIP107G	TO−220 (Pb−Free)	50 Units / Rail



TO−220−3 10.10x15.12x4.45, 2.54P
CASE 221A
ISSUE AL

DATE 05 FEB 2025



MILLIMETERS			
DIM	MIN	NOM	MAX
A	4.07	4.45	4.83
A1	1.15	1.28	1.41
A2	2.04	2.42	2.79
b	1.15	1.34	1.52
b1	0.64	0.80	0.96
c	0.36	0.49	0.61
D	9.66	10.10	10.53
D1	8.43	8.63	8.83
E	14.48	15.12	15.75
E1	12.58	12.78	12.98
E2	1.27 REF		

MILLIMETERS			
DIM	MIN	NOM	MAX
e	2.42	2.54	2.66
e1	4.83	5.08	5.33
H1	5.97	6.22	6.47
L	12.70	13.49	14.27
L1	2.80	3.45	4.10
Q	2.54	2.79	3.04
øP	3.60	3.85	4.09
Z	−.−−	−.−−	3.48

NOTES:
1. DIMENSIONING AND TOLERANCING PER ASME Y14.5M, 2018.
2. CONTROLLING DIMENSION: MILLIMETERS.
3. DIMENSION Z DEFINES A ZONE WHERE ALL BODY AND LEAD IRREGULARITIES ARE ALLOWED.

STYLE 1:
PIN 1. BASE
2. COLLECTOR
3. EMITTER
4. COLLECTOR

STYLE 2:
PIN 1. BASE
2. EMITTER
3. COLLECTOR
4. EMITTER

STYLE 3:
PIN 1. CATHODE
2. ANODE
3. GATE
4. ANODE

STYLE 4:
PIN 1. MAIN TERMINAL 1
2. MAIN TERMINAL 2
3. GATE
4. MAIN TERMINAL 2

STYLE 5:
PIN 1. GATE
2. DRAIN
3. SOURCE
4. DRAIN

STYLE 6:
PIN 1. ANODE
2. CATHODE
3. ANODE
4. CATHODE

STYLE 7:
PIN 1. CATHODE
2. ANODE
3. CATHODE
4. ANODE

STYLE 8:
PIN 1. CATHODE
2. ANODE
3. EXTERNAL TRIP/DELAY
4. ANODE

STYLE 9:
PIN 1. GATE
2. COLLECTOR
3. EMITTER
4. COLLECTOR

STYLE 10:
PIN 1. GATE
2. SOURCE
3. DRAIN
4. SOURCE

STYLE 11:
PIN 1. DRAIN
2. SOURCE
3. GATE
4. SOURCE

STYLE 12:
PIN 1. MAIN TERMINAL 1
2. MAIN TERMINAL 2
3. GATE
4. NOT CONNECTED

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DESCRIPTION:	**TO−220−3 10.10x15.12x4.45, 2.54P**	**PAGE 1 OF 1**

ADDITIONAL INFORMATION

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onsemi Website: www.onsemi.com

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