



## **Application Note: General Purpose Demo Hardware Description**

# **AS3911**

## **NFC Initiator / HF Reader IC**

---



## Table of Contents

- 1. Introduction ..... 2
- 2. Hardware ..... 2
  - 2.1. Block diagram ..... 2
  - 2.2. EMC and Power Supply Concept..... 3
  - 2.3. Digital Section (Microcontroller) ..... 4
    - 2.3.1. Programming Header P1..... 5
  - 2.4. Analog Section ..... 6
    - 2.4.1. Power concept ..... 7
    - 2.4.2. Antenna stage ..... 7
    - 2.4.3. Capacitive wake up ..... 8
- 3. Measurement..... 8
  - 3.1. Current consumption..... 8
  - 3.2. Antenna stage ..... 9
  - 3.3. Antenna stage ..... 9
  - 3.4. Determination of the antenna resistor .....11
  - 3.5. Determination of the antenna resistor .....12
  - 3.6. Verification of the Q factor in the time domain .....14
  - 3.7. Measurement with standard assembly of 2200  $\Omega$  .....14
- 4. Layout recommendation ..... 16
- 5. PCB stack ..... 16
- 6. Gerber top ..... 17
- 7. Gerber bottom ..... 17
- 8. Assembly top ..... 18
- 9. Bill of material ..... 19
- Copyright..... 22
- Disclaimer ..... 22

# 1. Introduction

This application note describes the AS3911 general purpose demo board and its usage. The general purpose board is made for a flexible use; hence the digital part can be separated from the analog part. This enables fast software development since the analog part can be used out of the box.

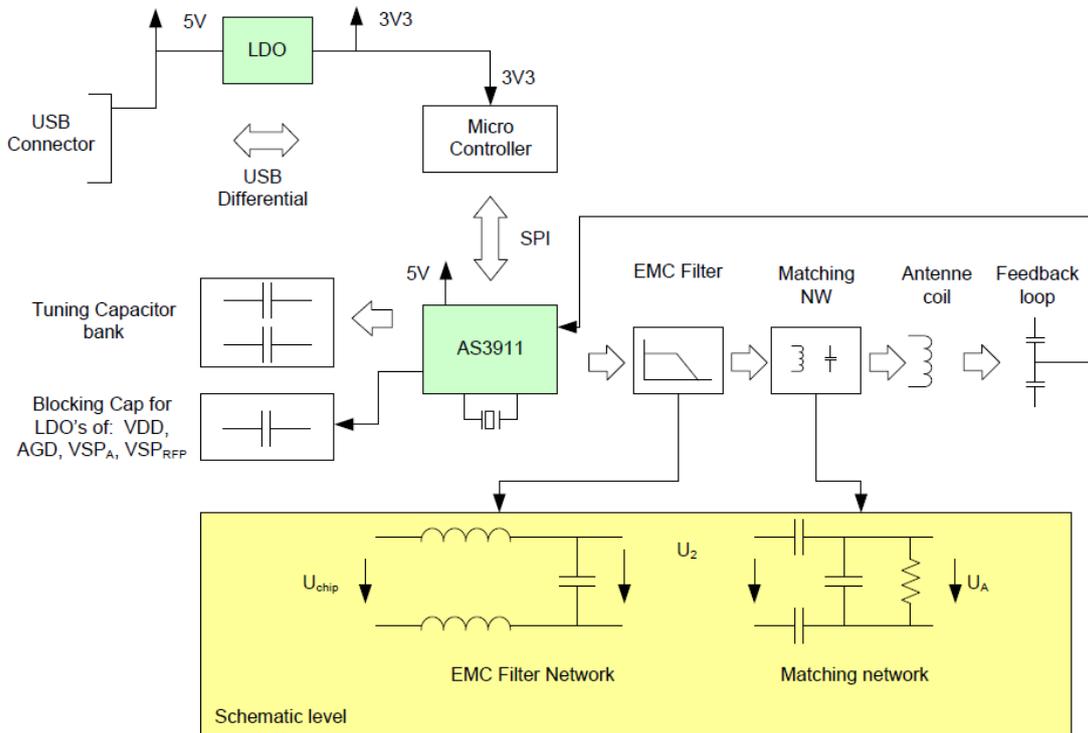
The analog section has several jumpers to allow a custom antenna and capacitive electrodes to be used.

# 2. Hardware

## 2.1. Block diagram

The board includes a microcontroller with USB support, a LDO to supply the microcontroller and the HF reader IC AS3911.

Figure 1: Blockdiagram of the demo board

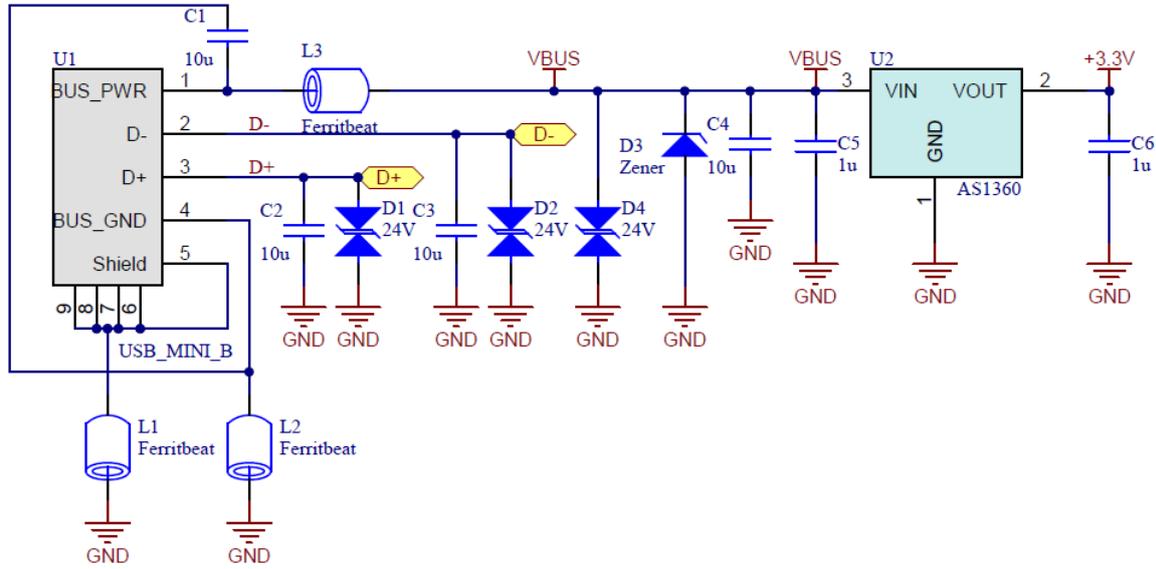




**2.2. EMC and Power Supply Concept**

For EMC rejection due to the rectangular carrier field generation, ferrite beads are placed close to the supply with additional capacitors next to the connector.

Figure 2: **EMC and power Supply concept**



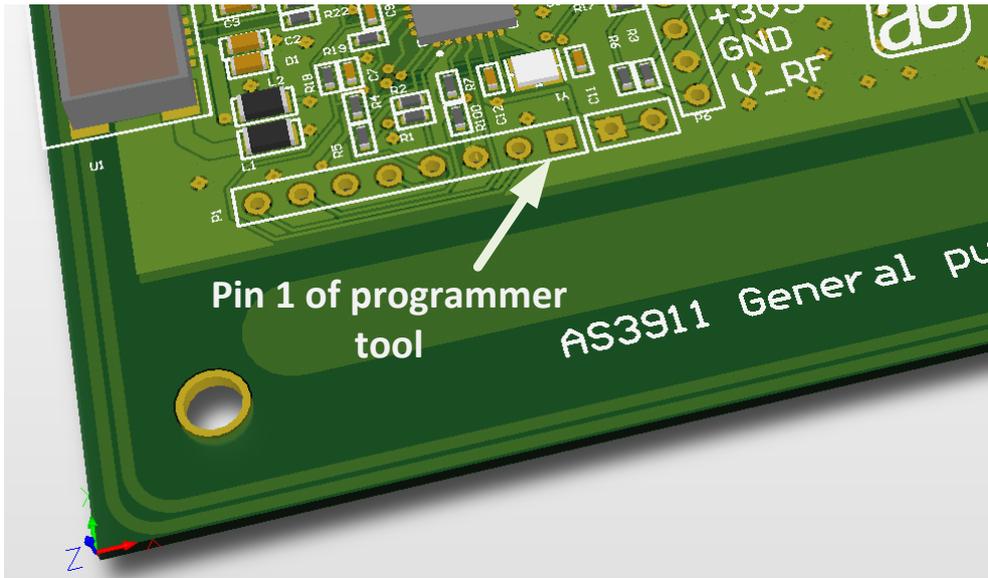
Since the worst case specification for USB-supply voltage is 4.5V, the supply voltage of the device might vary. AS3911 features an internal regulator that measures the voltage and adjusts the voltage on the output driver (i.e. the antenna driver) to 0.3V below the supply voltage. This adjustment assures that the digital noise on the antenna driver supply can be rejected and the voltage maximized. For evaluation purposes, the jumper P5 is placed. It can be used to apply an external voltage supply or measure the current of the reader IC.



### 2.3.1. Programming Header P1

P1 is the programming header for the microchip controller. The pin order on the header P1 is exactly the same as used by the microchip tool chain. Therefore no special adapter is needed.

Figure 4: Microcontroller schematic

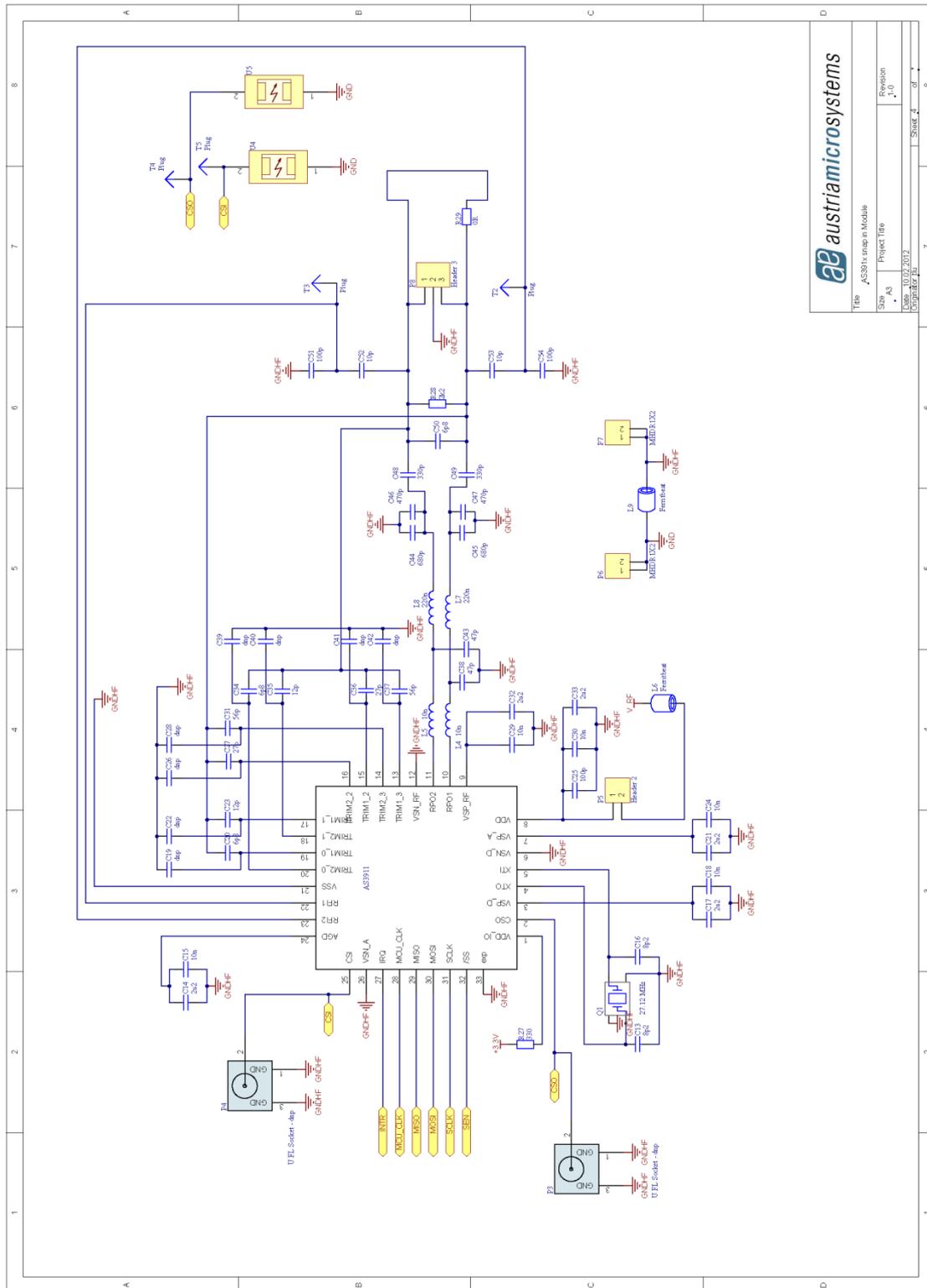




2.4. Analog Section

The following schematic shows the analog section incl. AS3911 and its external components.

Figure 5: Analog schematic



Title		AS3911: analog in Module	
Size	A3	Project Title	Revision
Drawn	10.02.2012	Author	1.0
Checked		Computer File	
		Sheet 2	of 8



This setup is made to demonstrate almost all the capabilities of AS3911. The salient features are:

- Differential antenna
- Capacitive wakeup (possibility to attach external electrodes)
- Antenna tuning trimming capacitors
- 27MHz Crystal
- Supply noise rejection
- High sensitivity
- Low impedance driver stage

#### **2.4.1. Power concept**

AS3911 features an internal LDO that needs to be decoupled with capacitors of 2.2  $\mu$ F and 10 nF. These pins are:

- AGD (analogue ground)
- VSP\_D (to supply the logic of AS3911)
- VSP\_A (to supply the analog part of AS3911)
- VSP\_RF (to supply the driver stage of AS3911)

AS3911 contains an internal level shifter that enables the connection to a microcontroller with different VDD than AS3911. Pin 1 should be connected to the same voltage as the supply of the microcontroller.

GND as well as the supply line are connected with a ferrite bead to reject the EMC disturbances caused by the HF driver.

#### **2.4.2. Antenna stage**

The antenna stage consists of a two stage filter and a matching network. The two stage filter rejects higher harmonics of the 13,56 MHz carrier. Since inductors are non-ideal components and the self-resonant frequency of the second coil is around 400 MHz, a two staged filter is implemented.



The first stage has a corner frequency above 200 MHz and will reduce harmonics at higher frequencies.

The second stage has a corner frequency below 10 MHz and will reject frequencies in the lower frequency band.

The matching network follows the filter and adapts the power from the driver to the antenna.

The tuning network consists of external capacitors and chip internal switches. In case the switches are open, the antenna voltage is directly applied to the input pin of the chip.

Since the expected voltage of the antenna can be high, additional capacitors for voltage limitation can be applied. The AS3911 can accept voltages up to 30V on its antenna tuning pins.

The input pins are connected by a capacitive divider. The voltage on these pins should be less than 3.3 Volt.

**2.4.3. Capacitive wake up**

The capacitive wakeup comprises two pins that are each connected to an electrode. They are protected against ESD with a gas discharge element.

Since these pins can also be used as test outputs, an additional UFL connector is mounted.

**3. Measurement**

**3.1. Current consumption**

The measurement is performed across the AS3911 supply jumper P5.

AS3911 working condition	Current consumption in
	mA
After startup en=1, rx_en=0, tx_en=0	7.58
en=1, rx_en=1, tx_en=0	14.97
en=1, rx_en=1, tx_en=1	150
en=0, rx_en=0, tx_en=0, wu=1	0.002

### 3.2. Antenna stage

Used equipment:

- Network Analyser HP 8753C Network Analyser
- Parameter test set 85047A Test set

### 3.3. Antenna parameter measurement

The parameter measurements are done in the following sequence:

1. Start with the measurement of the serial inductance and the serial resistor at a frequency that is far off the self-resonance of the antenna. The chosen frequency is 1MHz.

@ 1 MHz:  $L_{PC} = 940 \text{ nH}$   $R_{SDC} = 470 \text{ mOhm}$

2. Measurement of the self-resonance (point at which the impedance is real)

=>  $f_{res} \sim 59 \text{ MHz}$   $R_{res} = 5000 \text{ Ohm}$

Using the inductance values measured at 1 MHz, the resonance capacitance can be calculated with the formula:

$$C = \frac{1}{(2 \cdot \pi \cdot f_{res})^2 \cdot L_{PC}} = \frac{1}{(2 \cdot \pi \cdot 59 \text{ MHz})^2 \cdot 940 \text{ nH}} = 7.74 \text{ pF}$$

The value of the parallel resistor has to be converted from the self-resonance to the working frequency. The main reason for that conversion is the skin effect of the antenna. A correction factor can be given by:

$$K = \sqrt{\frac{f_{res}}{f_{tune}}} = \sqrt{\frac{59}{13,56}} = 2,085$$

$R_{res2}$  can then be calculated as:

$$R_{res2} = K \cdot R_{res} \approx 10.4 \text{ k}\Omega$$

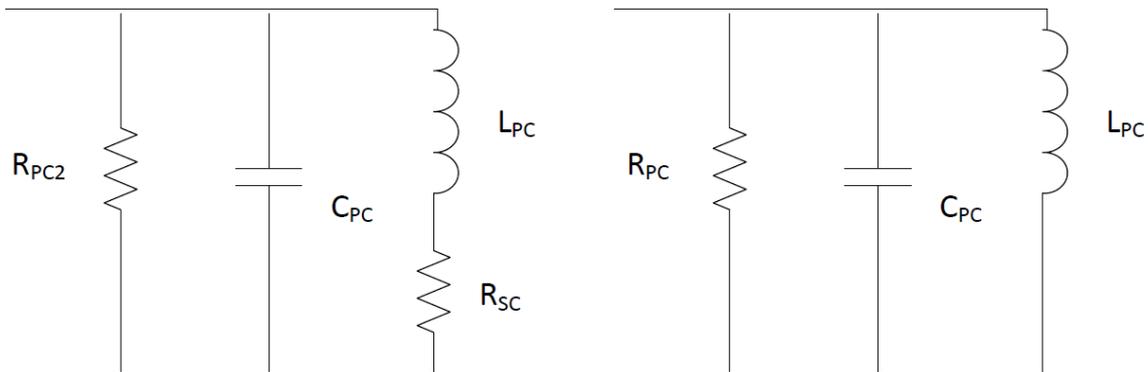
All antenna components are now known and a replacement for the antenna circuit can be drawn.

The serial resistor of the coil can be converted with the approximation formula of the Q-factor

$$Q = \frac{\omega L}{R_{SDC}} \approx \frac{R_{PDC}}{\omega L} \Rightarrow R_{PDC} = \frac{(\omega L)^2}{R_{SDC}} = 14 \text{ k}\Omega$$

The complete resistance will thus be a parallel connection of the resistor due to the DC component and the self-resonance component.

$$R_{PC} = \frac{R_{PDC} \cdot R_{res2}}{R_{PDC} + R_{res2}} \approx 6.02 \text{ k}\Omega$$



The values for the wanted resonance circuit are therefore:

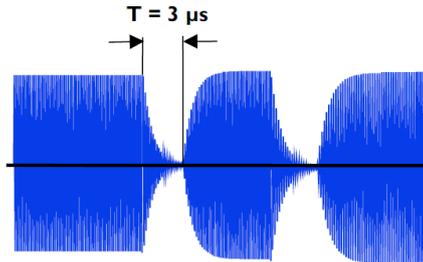
- $R_{PC} = 6.02 \text{ k}\Omega$
- $C_{PC} = 7.74 \text{ pF}$
- $L_{PC} = 940 \text{ nH}$

### 3.4. Determination of the antenna resistor

The bandwidth – time product and the definition of the quality factor Q results in the following equations:

$$B \cdot T \geq 1 \quad ; \quad Q = \frac{f_{res}}{B} \quad \Rightarrow \quad Q \leq f_{res} \cdot T \rightarrow Q \leq 13,56MHz \cdot 3\mu s = 41$$

The time T is defined by the lowest data rate of the ISO 14443 standard, 106kbits/s:



For the current board it is set to 20.

The parallel target resistor can then be calculated as:

$$R_T = Q \cdot \omega L$$

$$R_T = 20 \cdot 2 \cdot \pi \cdot 13MHz \cdot 940nH = 1601\Omega$$

Taking the parasitic resistor  $R_{PC}$  from the antenna into account, the effective resistance can be calculated to

$$R_p = \frac{R_{PC} R_T}{R_{PC} - R_T} = \frac{6020 \cdot 1601}{6020 - 1601} = 2181\Omega$$

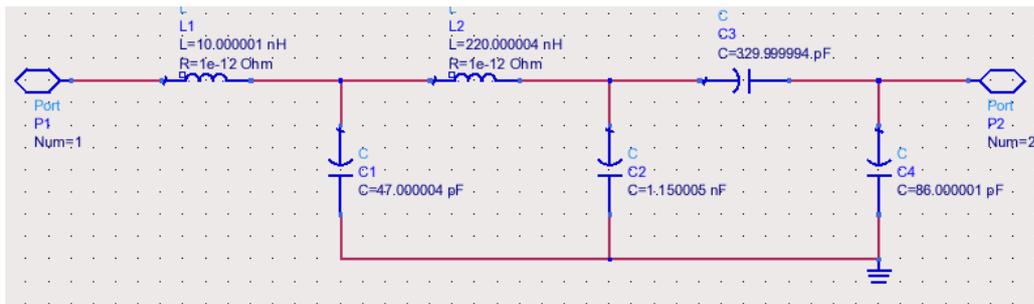
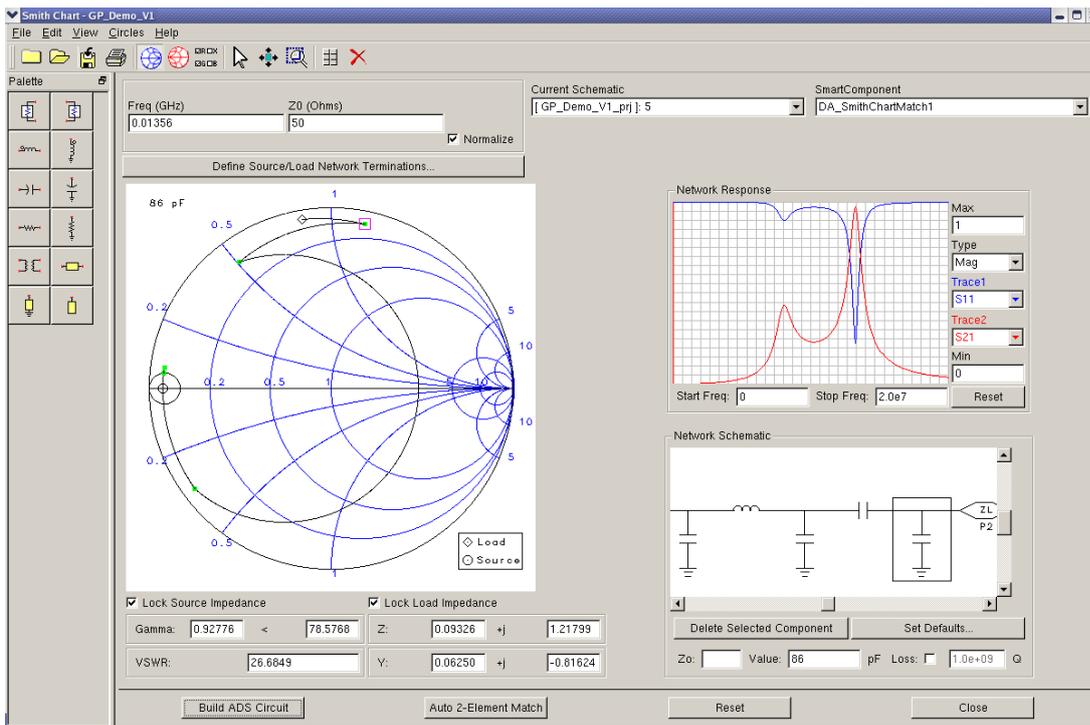
The next available value is 2200Ω.

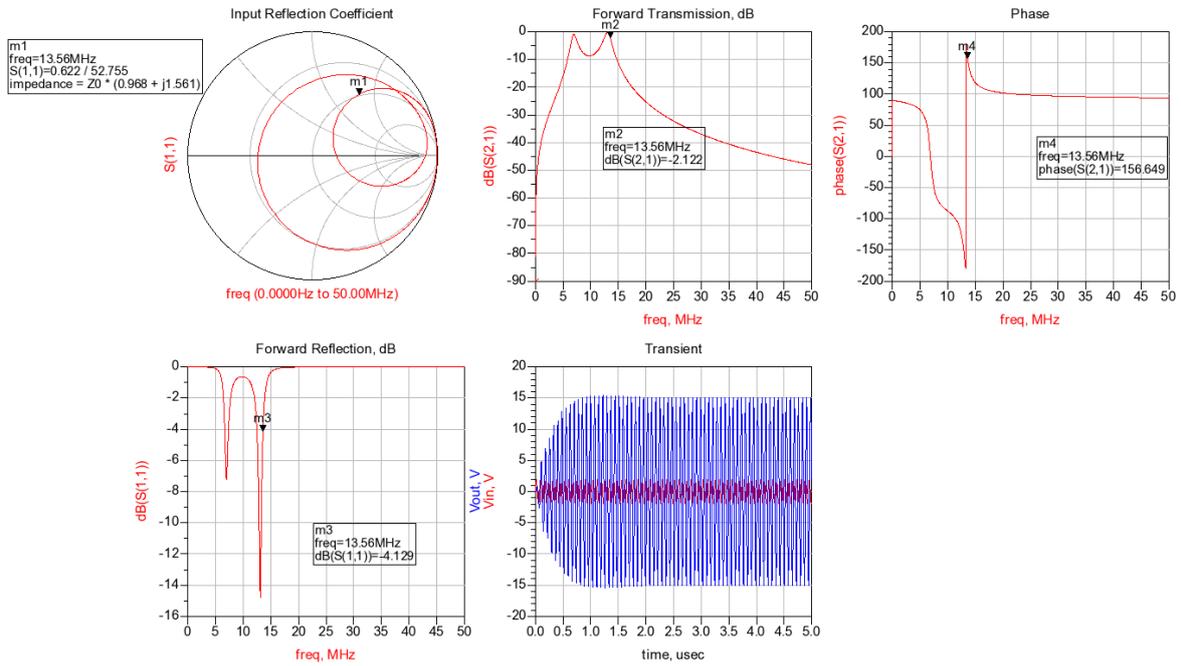
### 3.5.Determination of the matching network

- The matching is done from the driver resistor towards the antenna impedance.
- The driver resistor can be assumed with  $2\Omega$
- Converting the antenna parameters into single-ended ones for the Smith chart:

Parallel target antenna resistor:  $RT/2 = 800 \Omega$   
 Antenna coil inductance  $LP/2 = 470 \text{ nH}$   
 Antenna coil capacitance  $2*CP = 15,5 \text{ pF}$

The matching was done with ADS (Advanced Design System):





According to the simulations, the parallel capacitor should be 86 pF/2 (because of the conversion from single-ended to differential).

The procedure of splitting up this 43 pF capacitance is shown in the excel sheet "PCD\_AntennaMatching\_V1".



### 3.6. Verification of the Q factor in the time domain

The resonance circuit envelope can be calculated with an exponential function

Falling edge:

$$U_f = e^{\frac{-t}{\tau}} = \exp\left(-t \cdot \frac{2 \cdot \pi \cdot f_c}{Q}\right)$$

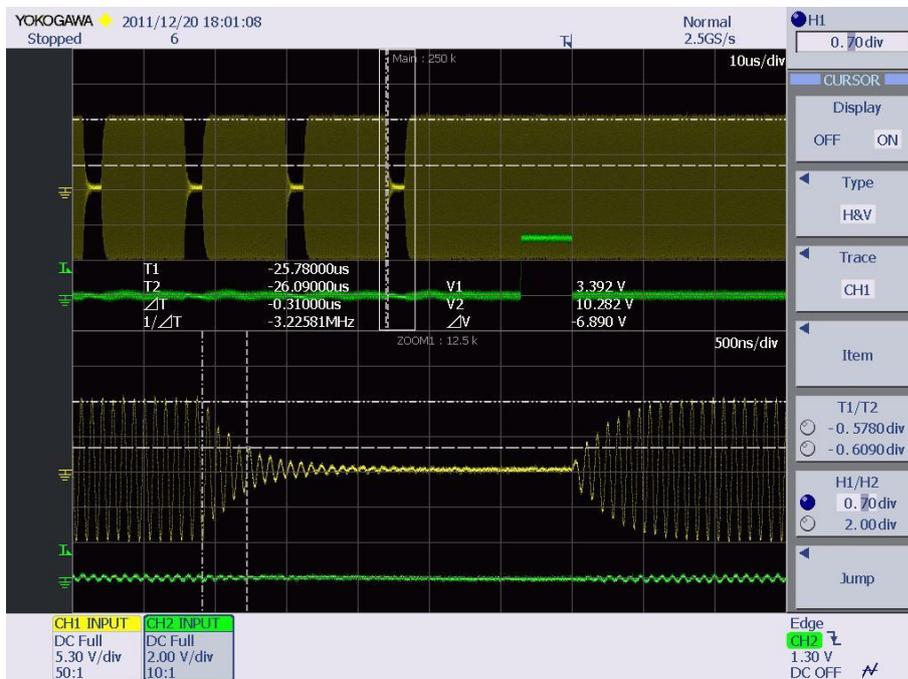
Rising edge:

$$U_r = 1 - e^{\frac{-t}{\tau}} = 1 - \exp\left(-t \cdot \frac{2 \cdot \pi \cdot f_c}{Q}\right)$$

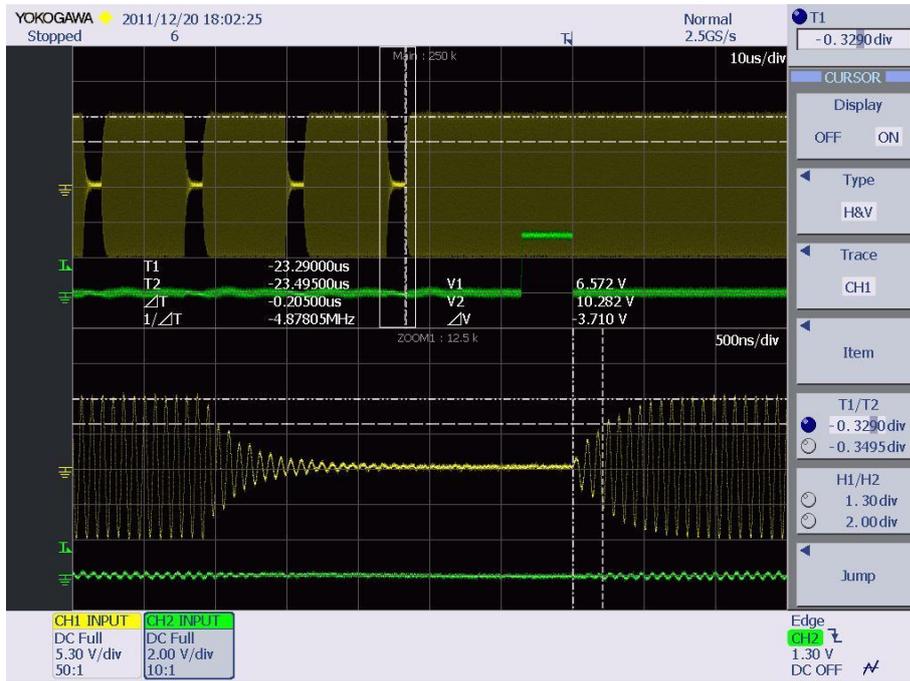
Thus if the time constant (37% of the maximum amplitude) is known, the Q factor is calculated to:

$$Q_B = \tau \cdot 2 \cdot \pi \cdot f_c$$

### 3.7. Measurement with standard assembly of 2200 Ω



- TF=310 ns
- QF=17



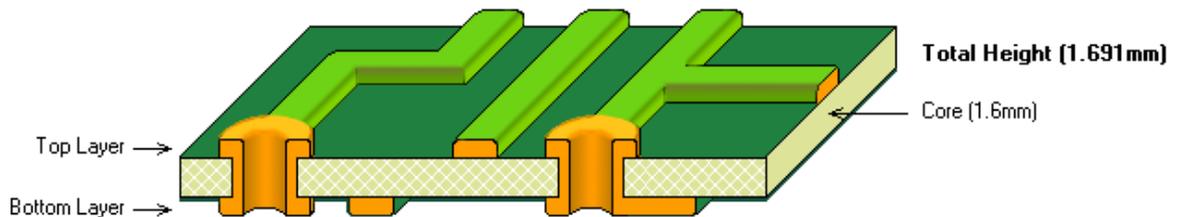
- With TR=205 ns
- QR=26

## 4. Layout recommendation

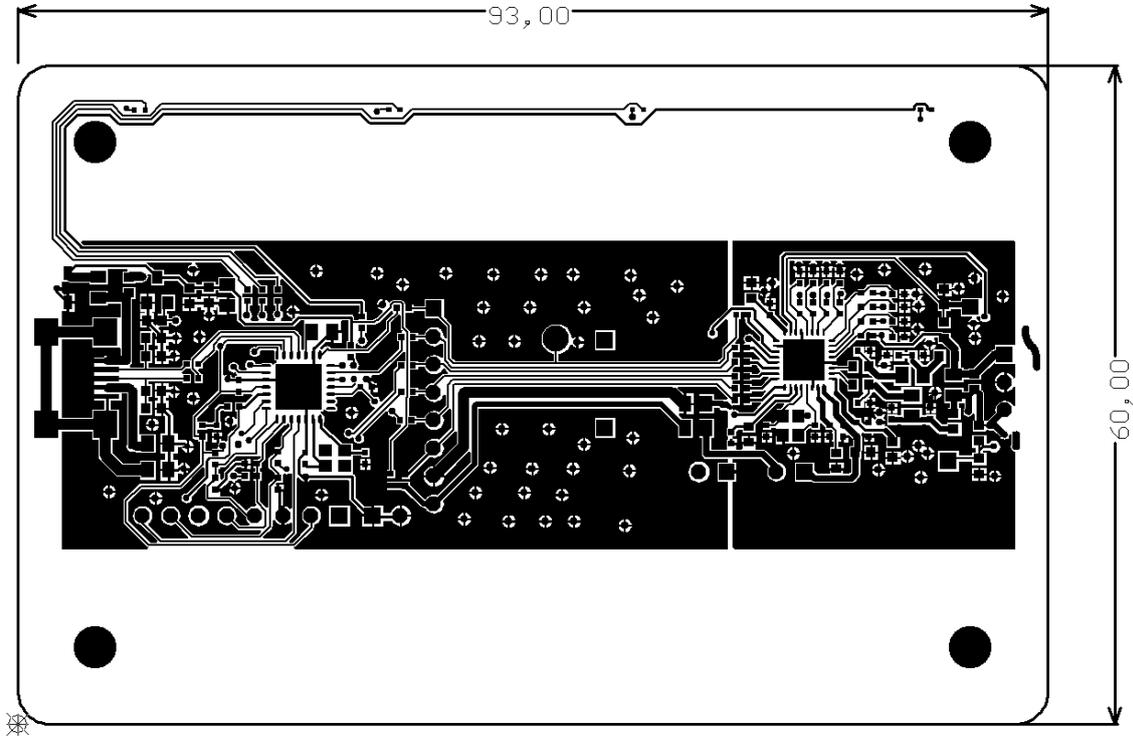
- Use a solid ground plane under the chip and thermal vias under the chip that are being used to dissipate the heat of and enable a low ohmic connection of the exposed pad to the ground plane.
- Take care that the decoupling capacitors of the LDO are close to the chip. Use thick wires for the decoupling tracks and place the 10nF capacitor closest to the chip.
- Use a symmetric layout for the antenna stage
- Do not cross digital lines with analog lines.
- Take care on the signals VSN\_RF, VSP\_RF and the two output pins RFO1 and RFO2. These pins build up the internal driver stage. Tracks on those four pins shall be short and ground connections must be solid.

## 5. PCB stack

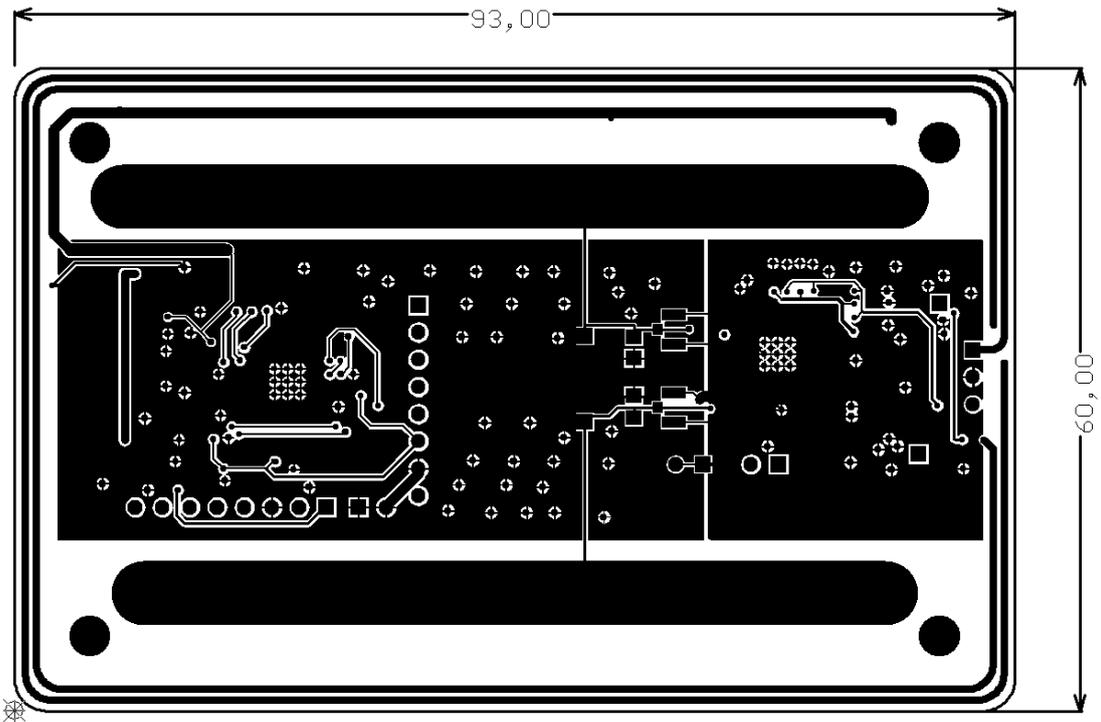
The PCB stack is made of a two layer PCB with 1.6 mm core material and 35micro (43 micro final ) copper.



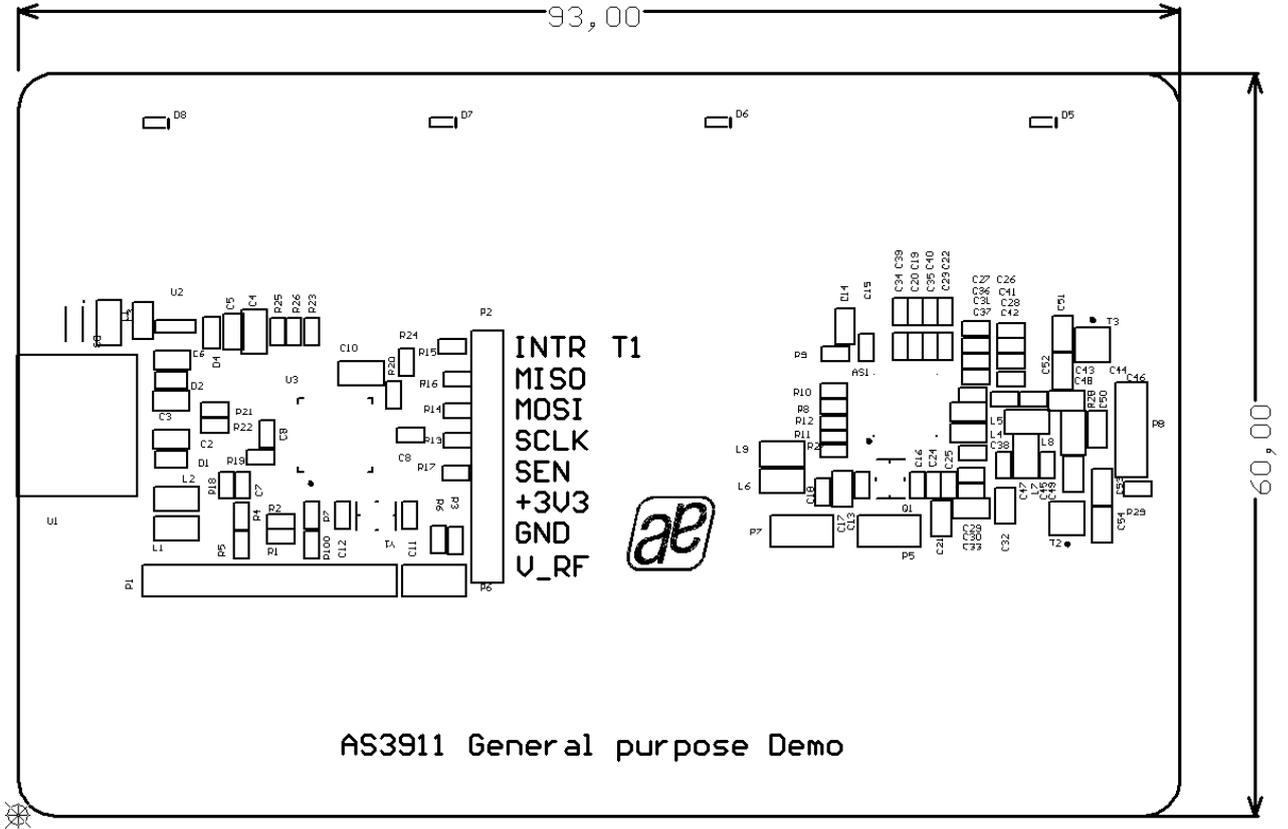
## 6. Gerber top



## 7. Gerber bottom



## 8. Assembly top



## 9. Bill of material

Part Info	Reference	Distributor	Distributor Number	count
<b>Integrated Circuits (IC)</b>				
AS3911	AS1			1
AS1360	U2			1
PIC27FJ64GB002	U3			1
<b>SMD resistor</b>				
10k	R1, R2, R4, R5, R7, R18, R20, R100	Digikey	311-10KGRTR-ND	8
0R	R6,R29	Digikey	311-0.0JRTR-ND	2
220R	R8, R9, R10, R11, R12, R13, R14, R15, R16, R17	Digikey	<a href="#">P220GTR-ND</a>	10
470R	R19, R23, R24, R25, R26	Digikey	<a href="#">RMCF0402JT470RTR-ND</a>	5
27R	R21, R22	Digikey	<a href="#">311-27JRTR-ND</a>	2
330R	R27	Digikey	<a href="#">311-330JRTR-ND</a>	1
2k2	R28	Digikey	<a href="#">311-2.2KJRTR-ND</a>	1
<b>SMD capacitors</b>				
10u	C1,C4,C10	Digikey	<a href="#">445-1371-2-ND</a>	3
10p	C2,C3	Digikey		2
1u	C5,C6	Digikey	587-2834-2-ND	2
10n	C7, C15, C18, C24, C29, C30	Digikey	311-1042-2-ND	6
100n	C8, C9	Digikey	478-1239-2-ND	2
18p	C11, C12	Digikey	445-1238-2-ND	4
8p2	C13, C16	Digikey	511-1029-2-ND	2
2u2	C14, C17, C21, C32, C33	Digikey	587-2983-2-ND	5
6p8	C20, C34	Digikey	445-4887-2-ND	2

12p	C23, C35	Digikey	311-1016-2-ND	2
100p	C25	Digikey	311-1024-2-ND	1
27p	C27, C36	Digikey	311-1019-2-ND	2
56p	C31, C37	Digikey	311-1022-2-ND	2
47p	C38, C43	Digikey	311-1021-2-ND	2
470p	C44, C47	Digikey	311-1028-2-ND	2
680p	C45, C46	Digikey	511-1068-2-ND	2
330p	C48, C49	Digikey	587-1217-2-ND	2
6p8	C50	Digikey	445-5039-2-ND	1
100p	C51, C54	Digikey	445-1281-2-ND	2
10p	C52, C53	Digikey	399-1049-2-ND	2
<b>SMD inductors</b>				
10n	L4,L5	Digikey	<a href="#">445-1492-2-ND</a>	2
220n	L7,L8	Digikey	<a href="#">490-5669-2-ND</a>	2
Ferritbead	L1, L2, L3, L6, L9	Digikey	<a href="#">587-1911-2-ND</a>	5
<b>SMD diodes</b>				
24V	D1, D2, D4	Farnell	1470613	3
Zener	D3	Digikey	641-1068-2-ND	1
<b>SMD LED</b>				
LED_LUMEX	D5,D6,D7,D8	Digikey	<a href="#">754-1104-2-ND</a>	4
<b>Oscillator</b>				
27.12MHz	Q1	Digikey	<a href="#">490-5581-2-ND</a>	1
<b>Mechanical components</b>				
Header 2	P5			1
USB_MINI_B	U1	Digikey	H2959TR-ND	1
<b>Not Used</b>				



U FL Socket - Surface Mount	P3, P4			2
Header 8H	P1, P2			2
8MHz	Y1			1
MHDR1X2	P6, P7			2
Header 3	P8			1
Plug	T1			1
Plug	T2, T3, T4, T5			4
dnp	C19, C22, C26, C28, C39, C40, C41, C42			8
dnp	R3			1
CSA20-141N DNP	U4, U5			2

Tolerance if not other specified	
Capacitor NP0/COG	2%
Capacitor X7R:	10%
Capacitor Y5V:	+80% - 20%
Tantalum	20%
Resistor	5%
Inductivity	5%

**Version History**

Version	Originator	Change log
1.00	tlu	Initial Version
1.02	tlu	Changed load cap on 27 MHz crystal, BOM
1.03	mram	Changing of the ams corporate design
1.04	mram	Correction of chapters 3.4 & 3.5



## Copyright

Copyright © 1997-2012, ams AG, Tobelbader Strasse 30, 8141 Unterpremstaetten, Austria-Europe. Trademarks Registered ®. All rights reserved. The material herein may not be reproduced, adapted, merged, translated, stored, or used without the prior written consent of the copyright owner.

All products and companies mentioned are trademarks or registered trademarks of their respective companies.

## Disclaimer

Devices sold by ams AG are covered by the warranty and patent indemnification provisions appearing in its Term of Sale. ams AG makes no warranty, express, statutory, implied, or by description regarding the information set forth herein or regarding the freedom of the described devices from patent infringement. ams AG reserves the right to change specifications and prices at any time and without notice. Therefore, prior to designing this product into a system, it is necessary to check with ams AG for current information.

This product is intended for use in normal commercial applications. Applications requiring extended temperature range, unusual environmental requirements, or high reliability applications, such as military, medical life-support or life sustaining equipment are specifically not recommended without additional processing by ams AG for each application. For shipments of less than 100 parts the manufacturing flow might show deviations from the standard production flow, such as test flow or test location.

The information furnished here by ams AG is believed to be correct and accurate. However, ams AG shall not be liable to recipient or any third party for any damages, including but not limited to personal injury, property damage, loss of profits, loss of use, interruption of business or indirect, special, incidental or consequential damages, of any kind, in connection with or arising out of the furnishing, performance or use of the technical data herein. No obligation or liability to recipient or any third party shall arise or flow out of ams AG rendering of technical or other services.

## Contact Information

### Headquarters

ams AG  
Tobelbader Strasse 30  
8141 Unterpremstaetten  
Austria

T. +43 (0) 3136 500 0

For Sales Offices, Distributors and Representatives, please visit:

<http://www.ams.com/contact>