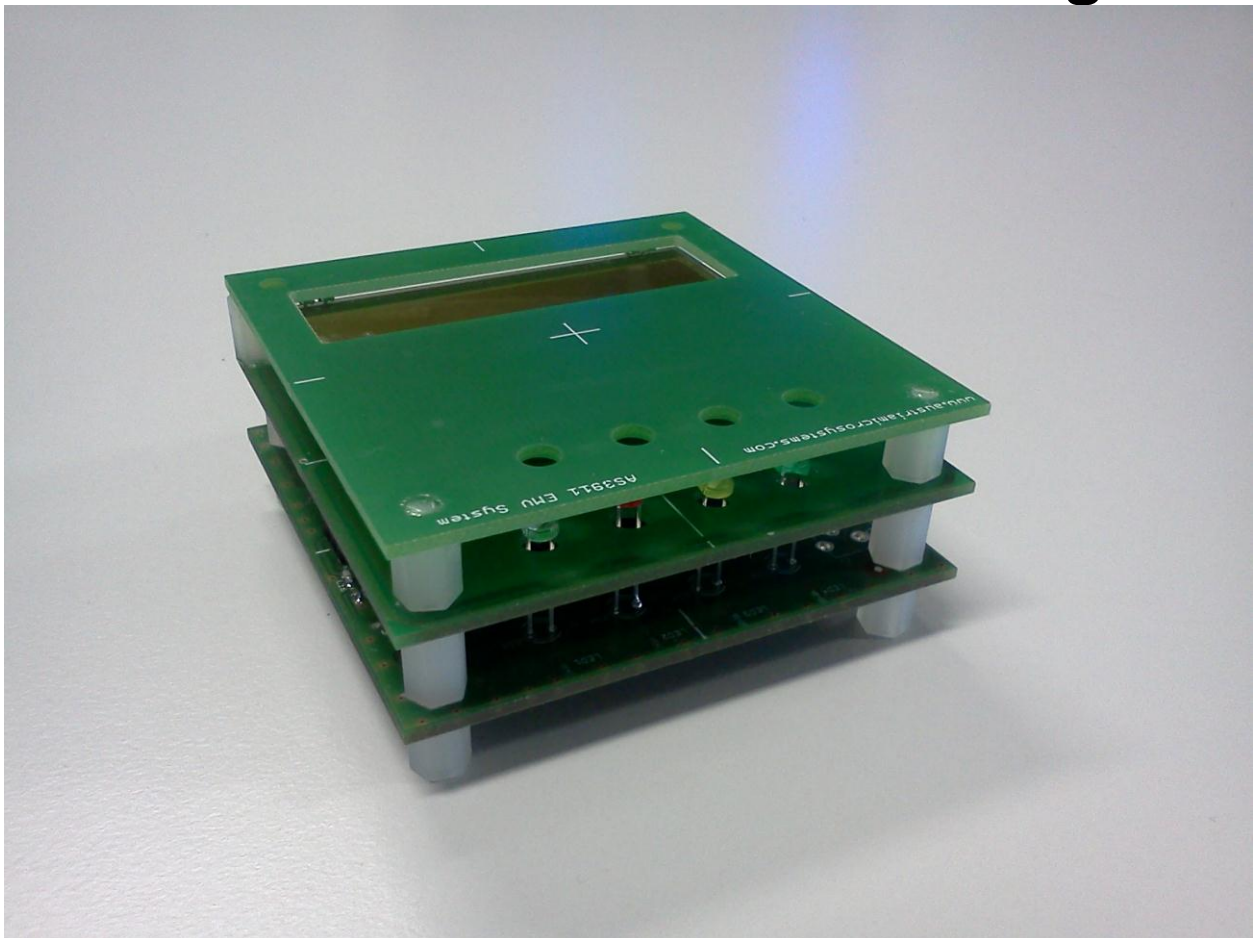


# AS3911

## AS3911 EMVco reference design



**Application note**  
**Rev 0V6 April 2012**

Application engineer: Thomas Luecker  
Marketing contact: Mark Dickson

1	Introduction.....	3
2	Hardware.....	3
2.1	Block diagram .....	3
2.1.1	Power supply noise rejection.....	4
2.1.2	AS3911.....	5
2.2	Measurements.....	6
2.2.1	Operating field.....	6
2.2.1	Timing Type A .....	8
2.2.2	Timing Type B .....	9
2.2.3	modulation depth verification Type B .....	9
3	Software .....	10
3.1	Graphical user Interface .....	10
3.1.1	Main/Startup Window .....	10
3.1.2	Settings Dialog .....	11
3.1.3	EMV analogue test mode .....	14
3.1.4	EMV digital test mode .....	15
3.1.5	EMV Pre-Validation Test Mode .....	16
3.2	AS3911 EMV Firmware .....	18
3.2.1	<b>AS3911 EMV Firmware setup</b> .....	18
3.2.2	AS3911 RFID Communication.....	19
3.2.3	AS3911 Interrupt handling module.....	20
3.2.4	AS3911 SPI module .....	20
3.3	EMV module .....	21
3.3.1	EMV RFID Hardware Abstraction Layer.....	21
3.3.2	EMV compliant ISO 14443 Layer 4 and Terminal Main Loop.....	21
3.3.3	EMV Card Technology Specific Functions .....	22
3.4	AS3911 EMV reader debug option .....	22
3.4.1	Hardware Configuration.....	22
3.4.2	Settings for UART .....	23
4	Test of the reader system.....	24
5	Appendix .....	25
5.1	Error handling procedures .....	25
5.1.1	Detection of residual Bits.....	25
5.1.2	Deaf time Definition.....	25
5.1.3	Ignore faulty messages .....	25
5.1.4	Soft framing error.....	26
5.2	Handling procedures for Type B load modulation.....	26
5.3	Controller programming procedure.....	28
5.4	EMC considerations .....	30
5.4.1	Power supply noise rejection.....	30
5.4.2	Antenna coil .....	30
5.4.3	EMC filter .....	30
5.4.4	Layout considerations .....	30
5.5	Adaption to different controller platform.....	30
5.6	Reference Documents .....	31
5.7	Revision Information.....	31
6	Disclaimer.....	32

# 1 Introduction

The three major credit card organizations Euro Card, Master Card and Visa (EMVco) started to adapt existing ISO 14443 standards and add testing and application relevant features to harmonize the equipment. EMVco describes hundreds of test cases that the solution needs to pass. Since it is an agreed standard and new credit cards are already RFID enabled, it is very likely that this system will see a broad adaption in the future.

RFID chips on the card can contain a huge amount of data and in addition the chip on the credit card can be connected with the RFID Interface. Since RFID will provide also energy to the credit card, a high sophisticated encryption without the need of battery is possible. This allows a high level on security and also new function of the credit card.

The solution of austriamicrosystems is designed to pass the high standards on analogue as well as digital test requirements of EMVco and has furthermore additional functions like antenna tuning which makes this solution attractive to the customer.

The application note describes complete reference design kit for the customer that he can use off the shelf and start his development.

## 2 Hardware

### 2.1 Block diagram

The EMV board compromise of a Micro controller with USB interface, a LDO to filter noise from the USB supply and to supply the AS3911. Since the micro controller requires a Voltage less than 3.6 Volt, two diodes from the LDO voltage are being used to supply the micro controller.

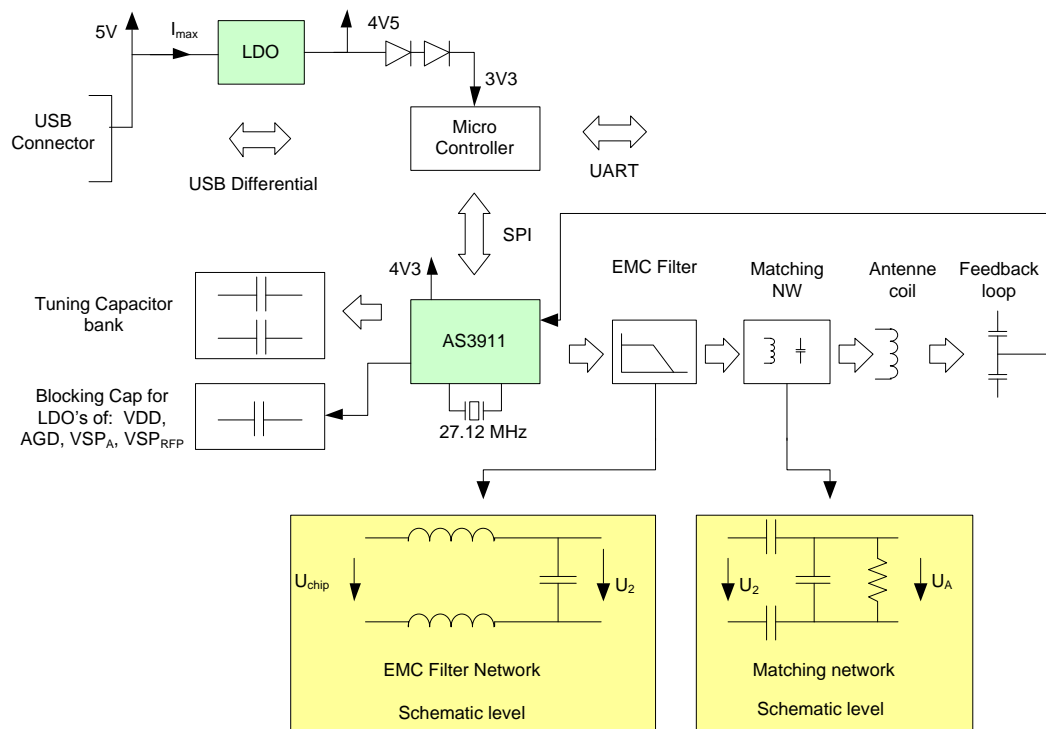
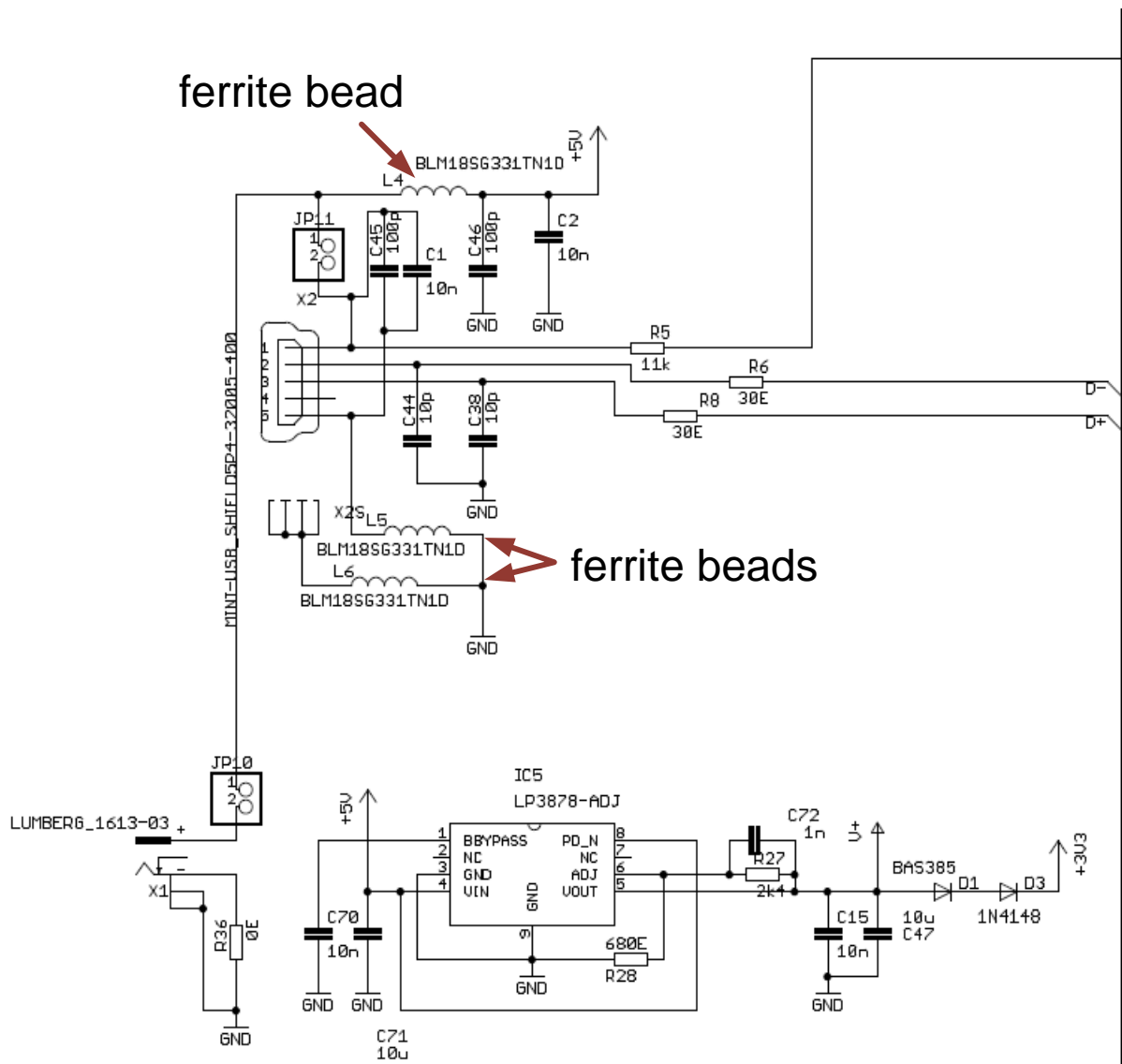


Figure 1, EMVco reference design block diagram

### 2.1.1 Power supply noise rejection

The power supply noise rejection will block the noise that is generated from the DCDC converters from the PC as well as limit the harmonics that are generated due the rectangular driver and distributed over the connector cable.

The rejection is done with ferrite close to the supply and additional capacitors after the connector.



**Figure 2, EMVco board Power supply section**

The board is supplied with 5 Volt either by USB supply ( max 500 mA) or with by an additional power jack in case USB has not sufficient current. Since the specification of USB-supply voltage can have worst case 4.5 Volt, the user needs to take care that USB supply is sufficient and not lower than 4.7 Volt during operation of the EMVco reader system.

The board provides two options for LDO assembly: One LP3878adjustable version and an option to use an AS1363-45 from austriamicrosystems.

### 2.1.2 AS3911

The antenna stage compromises an EMC Filter network, a matching network and the Antenna tank.

The filter network is set to a cut off frequency lower than the resonance frequency and compromises of the components L1, L2 and C20,C21,C23,C27.

The matching network adapts the low impedance of the outputs to the antenna and consists of the components. C25, C29 and in parallel to the antenna inductor the capacitor C31 and the resistor R3 that determine the quality factor of the reader system.

The tuning is composed out of external capacitors and chip internal switches. Since the input pins of the tuning are direct applied to the antenna, additional capacitors for voltage limitation are needed to limit the voltage below 30 Volt. The input pins are being connected through a capacitive voltage divider with the components C16,C17 and C19 and C24.

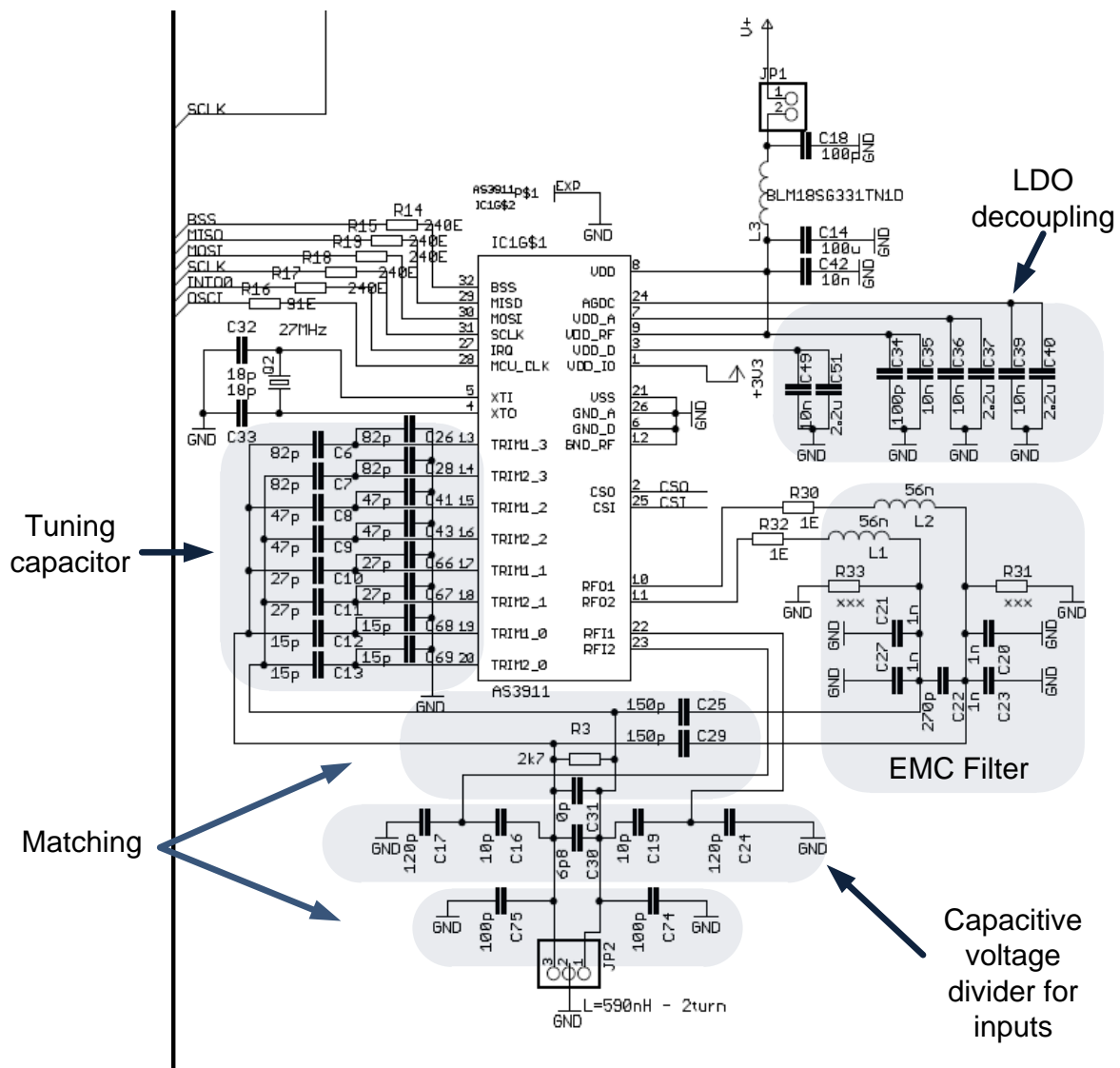


Figure 3, EMVco board AS3911 section

## 2.2 Measurements

### 2.2.1 Operating field

EMVco describes an operating Volume in which the test PICC should be placed. The test points within the operating volume are referenced to the center position and on top of the reader antenna.

Following picture shows on left side the definition of the EMVco test bench and on right side a 3D picture on which the blue cylinder is the operating volume for positions of the Test PICC. The operating volume has to be verified on 25 defined positions. These positions are grouped in 8 subgroups which represent the corner positions of two circles.

The Sub-group 1,3,5,7 are defined with a radius of 1.5 cm and at the elevation positions of zero and 4 cm. The sub-group 2,4,6,8 are defined with a radius of 2.5 cm.

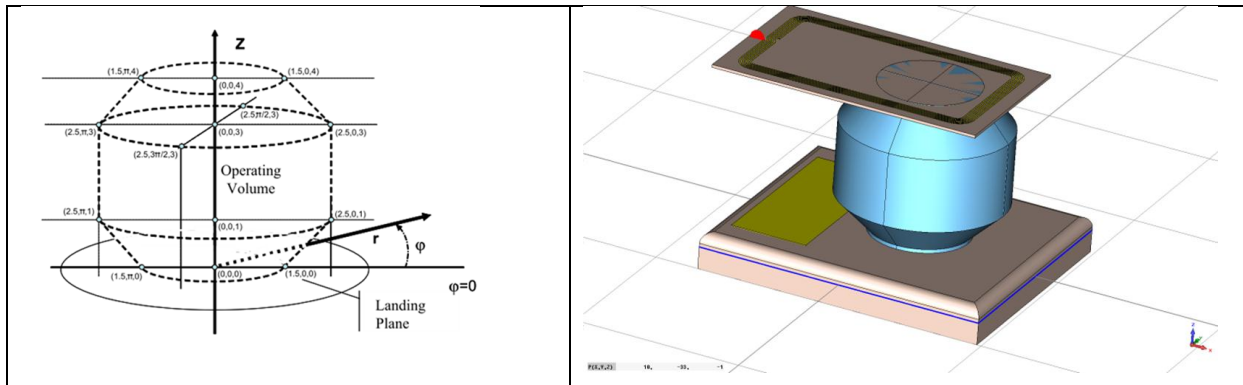


Figure 4, Operating Volume

Following table gives the Voltage of the test PICC on the defined test positions.

Position (z,r,f)	0 (r=0,f=0) [Volt]	1 (r=1,f=0) [Volt]	2 (r=2,f=0) [Volt]	3 (r=1,f=3) [Volt]	4 (r=2,f=3) [Volt]	5 (r=1,f=6) [Volt]	6 (r=2,f=6) [Volt]	7 (r=1,f=9) [Volt]	8 (r=2,f=9) [Volt]	Criteria	Verdict
z = 0 cm	7.69	7.48		7.71		7.58		7.66		$\geq 3.10 \text{ V}$ $\leq 8.2 \text{ V}$	PASS
z = 1 cm	7.25		5.70		5.91		5.86		6.01	$\geq 3.05 \text{ V}$ $\leq 8.2 \text{ V}$	PASS
z = 2 cm	5.81		4.48		4.39		4.61		4.46	$\geq 3.00 \text{ V}$ $\leq 8.2 \text{ V}$	PASS
z = 3 cm	4.32		3.34		3.19		3.42		3.22	$\geq 2.775 \text{ V}$ $\leq 8.2 \text{ V}$	PASS
z = 4 cm	3.08	2.79		2.76		2.84		2.78		$\geq 2.55 \text{ V}$ $\leq 8.2 \text{ V}$	PASS

Figure 5, Operating Volume measurement table

## 2.2.1 Timing Type A

The timings are defined in ISO 14443-2 Standard.

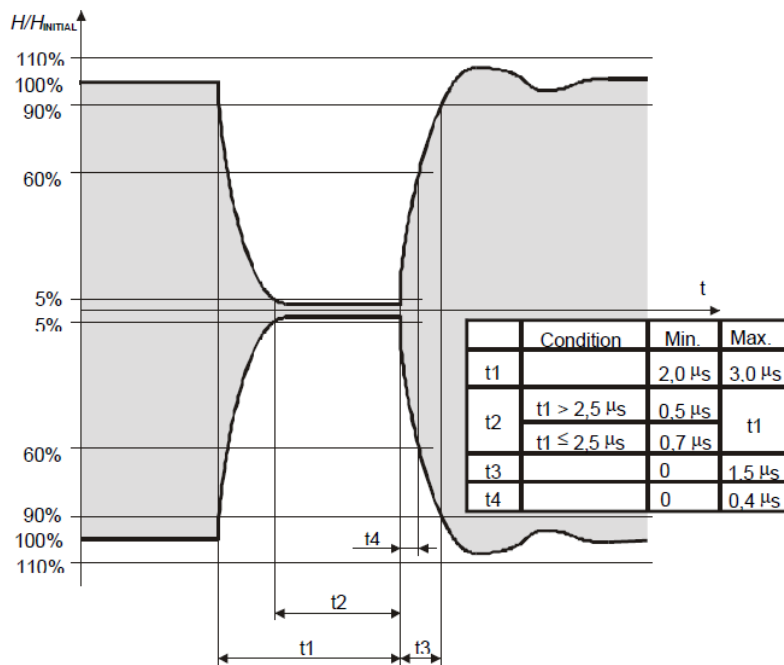


Figure 6, ISO 14443 A timing definition

TA121.z00	Verifying the t <sub>1</sub> Timing	PASS	z = 0 cm: t <sub>1</sub> = 2.56 $\mu$ s z = 1 cm: t <sub>1</sub> = 2.56 $\mu$ s z = 2 cm: t <sub>1</sub> = 2.57 $\mu$ s z = 3 cm: t <sub>1</sub> = 2.56 $\mu$ s z = 4 cm: t <sub>1</sub> = 2.56 $\mu$ s
TA124.z00	Verifying the t <sub>2</sub> Timing	PASS	z = 0 cm: t <sub>2</sub> = 2.3 $\mu$ s z = 1 cm: t <sub>2</sub> = 2.0 $\mu$ s z = 2 cm: t <sub>2</sub> = 1.9 $\mu$ s z = 3 cm: t <sub>2</sub> = 1.8 $\mu$ s z = 4 cm: t <sub>2</sub> = 1.7 $\mu$ s
TA125.z00	Verifying the t <sub>4</sub> Timing	PASS	z = 0 cm: t <sub>4</sub> = 127 ns z = 1 cm: t <sub>4</sub> = 187 ns z = 2 cm: t <sub>4</sub> = 228 ns z = 3 cm: t <sub>4</sub> = 246 ns z = 4 cm: t <sub>4</sub> = 254 ns
TA126.z00	Verifying the t <sub>3</sub> Timing	PASS	z = 0 cm: t <sub>3</sub> = 0.26 $\mu$ s z = 1 cm: t <sub>3</sub> = 0.43 $\mu$ s z = 2 cm: t <sub>3</sub> = 0.55 $\mu$ s z = 3 cm: t <sub>3</sub> = 0.60 $\mu$ s z = 4 cm: t <sub>3</sub> = 0.61 $\mu$ s

Figure 7, ISO 14443 A timing measurement



### 2.2.2 Timing Type B

The timings are defined in ISO 14443-2 Standard.

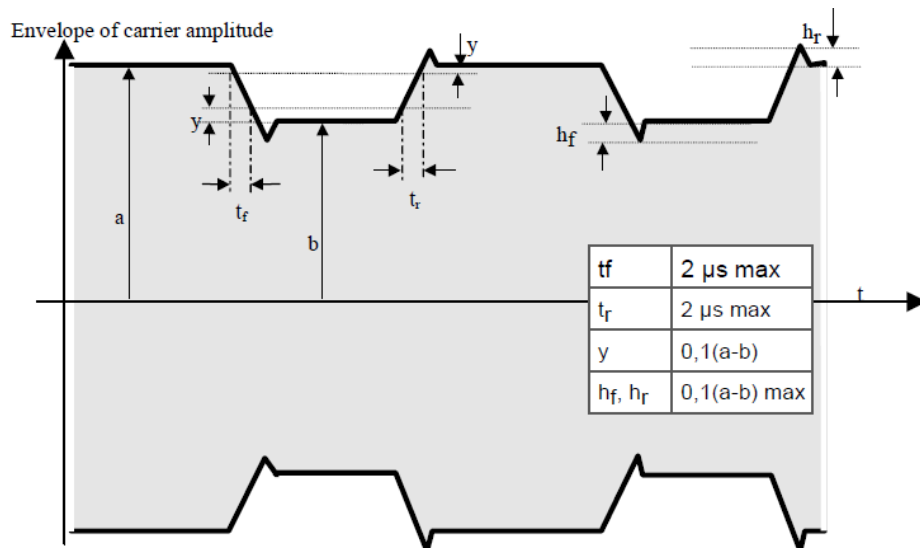


Figure 8 ISO 14443 timing definition

TB122.z00	Verifying the Fall Time	PASS	$z = 0$ cm: $t_f = 317$ ns $z = 1$ cm: $t_f = 541$ ns $z = 2$ cm: $t_f = 705$ ns $z = 3$ cm: $t_f = 819$ ns $z = 4$ cm: $t_f = 882$ ns
TB123.z00	Verifying the Rise Time	PASS	$z = 0$ cm: $t_r = 308$ ns $z = 1$ cm: $t_r = 506$ ns $z = 2$ cm: $t_r = 645$ ns $z = 3$ cm: $t_r = 701$ ns $z = 4$ cm: $t_r = 742$ ns

Figure 9 ISO 14443 B timing measurement

### 2.2.3 modulation depth verification Type B

TB121.z00	Verifying the Modulation Index	PASS	$z = 0$ cm: $m_i = 10.5$ % $z = 1$ cm: $m_i = 12.0$ % $z = 2$ cm: $m_i = 11.7$ % $z = 3$ cm: $m_i = 11.8$ % $z = 4$ cm: $m_i = 11.6$ %
-----------	--------------------------------	------	--

Figure 10 ISO 14443 B modulation depth measurement

## 3 Software

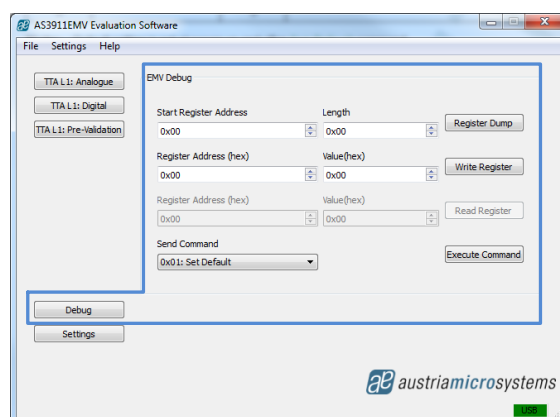
### 3.1 Graphical user Interface

The AS3911 EMV Evaluation Suite GUI's main purpose is to act as Device Test Environment as specified in the "EMVCo Type Approval Contactless Terminal Level 1 Device Test Environment Version 1.0 Draft V1 (July 2008)" Standard. The layout and behavior thus follows the recommendations made in the above mentioned document.

The following sections will introduce the various test modes available in the GUI.

#### 3.1.1 Main/Startup Window

The AS3911 EMV Evaluation Suite GUI consists of two parts. Controls on the left side are shown permanently whereas the right side is changed dependent on the selected TTA (terminal type approval) L1 test mode. The Tests are described in the described in PCD Analogue Test Bench and Test Case Requirements and PCD Digital Test Bench & Test Cases.



**Figure 11 main/ startup of EMVco GUI Software**

Following TTA L1 test modes are available

1. TTA L1: Analog  
Select the analog test modes according to Document PCD Analogue Test Bench, Chapter 7, PCD Analogue Test Plan.
2. TTA L1: Digital  
Selects the digital test application according Document PCD Digital Test Bench & Test Cases in Chapter 4 , TYPE A TEST CASES and Chapter 5, TYPE B TEST CASES.
3. TTA L1: Pre-Validation  
Selects the pre-validation test application.

The "Debug" option on the lower left side will display the start screen. This debug screen can be used to read out the register map of the AS3911 register content (using the UART connection) and load the defined register file from a file.

The "Settings" button opens a dialogue box for various analogue settings of the AS3911 EMV reader board.

The "Send commands" options allow sending of direct commands to the AS3911 reader.

### 3.1.2 Settings Dialog

EMV Settings

Supply Voltage: ☐ 3.3V ☒ 5V

Voltage Regulator: Disabled

Antenna Trim: 0010

RX Channel: AM

First Stage Gain Reduction AM: 0.0dB

First Stage Gain Reduction PM: 0.0dB

Digitizer and 2nd/3rd stage gain reduction AM: Digitizer:0.0dB, 2/3 Stage:0.0dB

Digitizer and 2nd/3rd stage gain reduction PM: Digitizer:0.0dB, 2/3 Stage:0.0dB

Test Output (CSI/CSO): None

Gain Control Squelch

☒ Enable AGC

Mode

☒ First 8 Subcarriers

☐ Complete Receive Period

Algorithm

☒ Preset

☐ Reset

☒ EnableDynamic Squelch

☐ Enable Additional Limiter

☐ Enable Gain Adoption

X (hex) Y (hex)

Add Item Remove Item Clear

ISO 14443B Modulation Depth

	X (hex)	Y (hex)
1	66	74
2	9a	80
3	bd	88
4	cc	8e
5	d3	8e

☒ Fixed Driver Strength 0x ##

☐ Automatic Modulation 0x ## 0x00

☐ Use Lookup Table

Add Item Remove Item Clear

Load Settings Save Settings OK Cancel

Figure 12 Settings of the AS3911 EMVco reference system

The settings dialog allows manipulating different parameters of the analog front end of the AS3911 reader chip.

#### 3.1.2.1 Supply Voltage

Select the supply voltage which is applied to the AS3911. Since the board is supplied by 4.3 Volt, the setting should be 5 Volt.

#### 3.1.2.2 Voltage Regulator

Select the regulated supply voltage for the power amplifiers of the AS3911 RF outputs. The available regulated voltage levels depend on the selected supply voltage. If the setting “disabled” is selected, the internal voltage regulators will be bypassed and the power

amplifiers will be directly connected to the supply voltage. This is the correct setting on the EMVco board since an external LDO is being used.

### 3.1.2.3 Antenna Trim

Select the setting of the antenna trim bits of AS3911. The available settings designate the value of the antenna trim bits from the most significant bit (bit tre\_3 in the antenna calibration control register) to the least significant bit (bit tre\_0 in the antenna calibration control register). Please refer to chapter “8.19 Antenna Tuning” of AS3911 datasheet.

### 3.1.2.4 RX Channel

Select the receiver channel. Available options are:

1. AM and PM  
Both, the AM and the PM channel are active during reception and the chip internally decides which signal to use based on signal quality.
2. AM  
Only the AM channel is active and used for data reception.
3. PM  
Only the PM channel is active and used for data reception.

### 3.1.2.5 First Stage Gain Reduction AM/PM

Selects the first stage gain reduction of the AM and PM receiver channel, respectively. The available settings reflect all possible configurations of the am and pm first stage gain reduction bits in the receiver configuration register 3. The lim and the rg\_nfc bits of receiver configuration register 3 are always set to zero (limiter disabled, no fixing of the gain reduction to 15dB) no matter which AM and PM channel gain reduction setting combination is selected.

### 3.1.2.6 Digitizer and 2<sup>nd</sup>/3<sup>rd</sup> stage gain reduction AM/PM

Select the gain reduction of the 2<sup>nd</sup> and 3<sup>rd</sup> stage for the AM and PM channel, respectively. The available settings reflect all possible configurations of the am and pm 2<sup>nd</sup> and 3<sup>rd</sup> stage gain reduction bits in the receiver configuration register 4. For further Information please refer to chapter “8.3 Receiver” of the AS3911 DatasheetR1.0.

### 3.1.2.1 Gain control squelch

The second gain stage of the AS3911 provides an automatic gain control algorithm (AGC) stage which can be enabled to ensure that the receiver keep in a linear range on large input signals.

The AGC can be set within the first 8 subcarriers or over the complete receive frame.

The “reset” option will reduce from the maximum gain in single steps. Using the “preset” option will reduce to the gain on a predefined value. For further information, please refer to the chapter “8.3.4 AGC, Squelch and RSSI” of the AS3911 datasheet R1.0.

Enable “dynamic squelch” will enable the squelch feature of the AS3911 on all receive states (even in deaf time period on which no data are received)

“Enable additional limit” This option is to clamp the input signal to 0.6 Volt which is the case for NFC peer to peer communication.

“Enable gain adaption”

This is a firmware feature that will reduce the gain in dependency of the distance of the test PICC.

The table define the gain values in dependency of the detuning of the antenna.

Table X measure amplitude for the reader

Table Y define the needed gain reduction setting for that amplitude

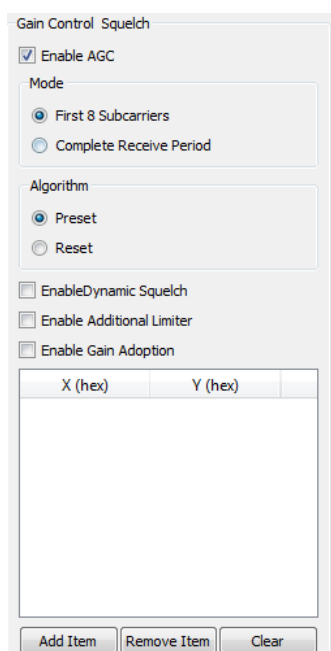


Figure 13 gain control section of the setting dialogue

### 3.1.2.2 Test Output (CSI/CSO)

Select the test output signal for the CSI and CSO pins. The signals of this pin are available on two pads on the AS3911 EMV reader PCB. Available are all test output signal combinations which can be accessed during normal chip operation (i.e. chip is not in any special test mode).

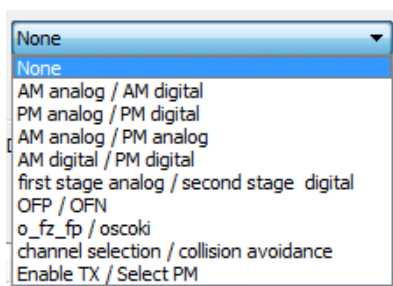


Figure 14 available test modes of AS3911 reference system

### 3.1.2.3 ISO 14443 Modulation Depth control

We typically aim for around 11% modulation index.

The AS3911 provide a register to define the resistor of the driving stage. This variable resistor is used in the AS3911 firmware to control the modulation depth in dependency of the detuning of the PICC. A detailed description can be found in Annex chapter 5.25.2 .

The GUI provides three options:

- for a fixed driver strength that uses the static register setting of the modulation depth control register.
- Automatic modulation depth control: This option uses the automatic modulation depth adjustment that is provided by the AS3911.
- Use of a look up table: The look up table represent the internal `envioIso14443bModulationLevelX` which is the Amplitude measured at various distances (typically 0-4 or 0-5) and `envioIso14443bModulationLevelY` which is the

Antenna driver strength register value needed to achieve a type B modulation index that lies comfortably in the allowed range.

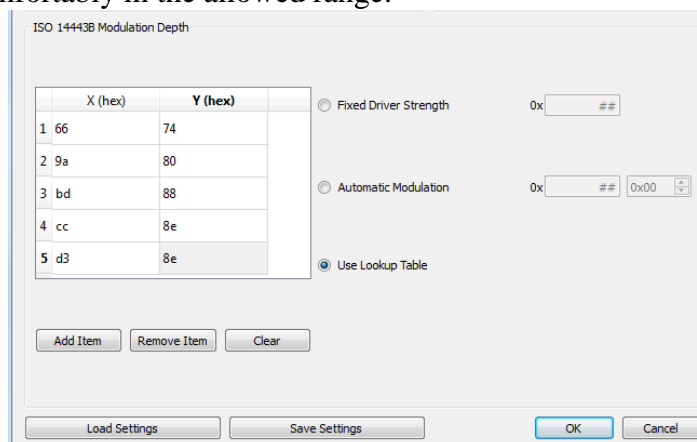


Figure 15 modulation depth adjustment section of the settings dialogue

### 3.1.3 EMV analogue test mode

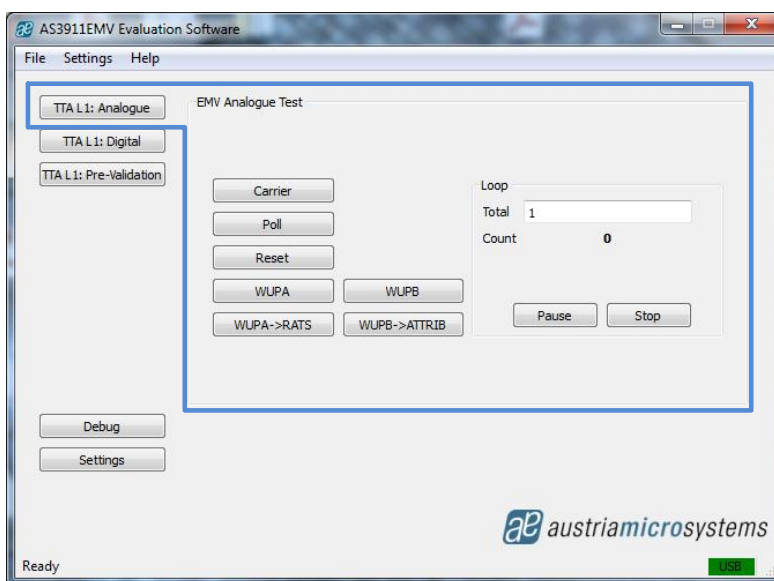


Figure 16 Analogue test mode

The analog test mode which can be selected via pressing button “TTA L1: Analogue” makes all functions available which are required for PCD Control (see Section 6 of the EMVCo Type Approval Contactless Terminal Level 1 Device Test Environment Version 1.0 Draft V1 (July 2008)). The “Total” text field lets the user select how often a function is executed. The “Stop” and “Pause” button can be used to either stop or pause multiple executions of the same command. The available commands are:

#### 3.1.3.1 Carrier

Toggles the state of the carrier of the EMV reader. If the reader field is currently on then the reader field will be turned off. If the reader field is currently off, then the reader field will be turned on.

#### 3.1.3.2 Poll

Performs a single round of the EMV polling loop.

### 3.1.3.3 Reset

Performs a single EMV field reset operation.

### 3.1.3.4 WUPA

Performs a single WUPA request.

### 3.1.3.5 WUPA->RATS

Performs a single type A card activation consisting of anticollision followed by RATS. The complete sequence is performed according to the EMV standard (i.e. including error handling and command retransmissions as required by the EMV standard).

### 3.1.3.6 WUPB

Performs a single WUPB request.

### 3.1.3.7 WUPB->ATTRIB

Performs a single type B card activation consisting of anti-collision, followed by ATTRIB. The complete sequence is performed according to the EMV standard (i.e. including error handling and command retransmissions as required by the EMV standard).

## 3.1.4 EMV digital test mode

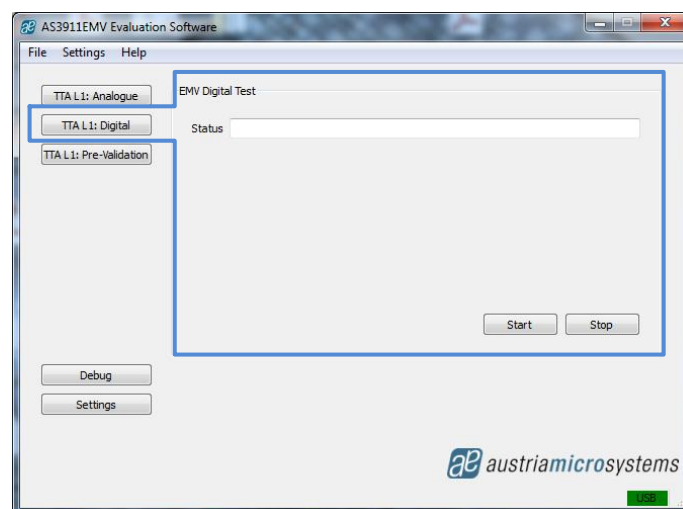


Figure 17 digital test mode screenshot

The digital test mode is selected by pressing the “TTA L1: Digital” button.

The digital test mode consists of only two command buttons – the “Start” and the “Stop” button. After the “Start” button was pressed, the PCD starts the so called Loop-Back Application (see Section 8: Requirements for Loop-Back Application in the EMVCo Type Approval Contactless Terminal Level 1 Device Test Environment Version 1.0 Draft V1 (July 2008)). This Loop-Back Application will continue to run autonomously on the EMV reader until the “Stop” button was pressed.

### 3.1.4.1 Loop-Back Application (Overview)

In the Loop-Back Application mode the EMV reader will continuously poll for type A and type B cards. If a card is detected it will be activated and the reader will start to send

commands to the card until a specified stop loopback data packed is received. After the reception of this stop packed the reader executes the card removal procedure and once the card has been removed from the field the reader restarts the loopback application and polls for a new card.

### 3.1.5 EMV Pre-Validation Test Mode

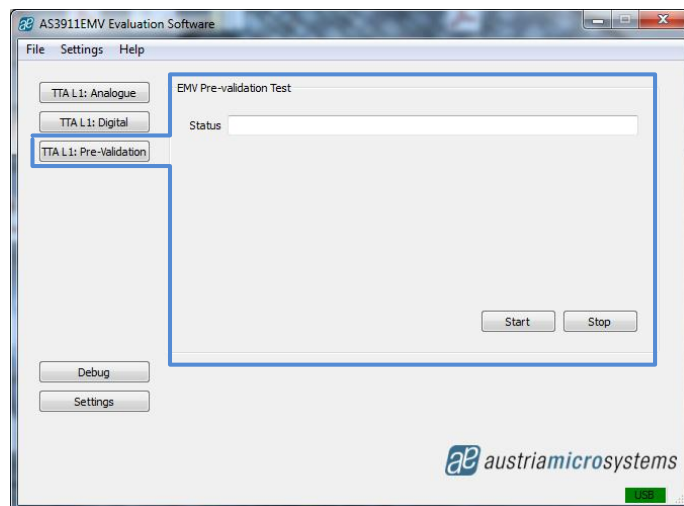


Figure 18 Pre validation test mode screen shot

The interface of the pre-validation test mode is essentially the same as the interface for the digital test mode.

When the “Start” button was pressed then the pre-validation test application is started on the EMV reader and continues to run autonomously until the “Stop” button was pressed. Details regarding the pre-validation test application can be found in Section 7: Requirements for Pre-Validation Test Application in the EMVCo Type Approval Contactless Terminal Level 1 Device Test Environment Version 1.0 Draft V1 (July 2008).

#### 3.1.5.1 Pre-Validation Application (Overview)

In the pre-validation test application the reader continuously polls for cards and once a card has been detected and successfully activated, it sends the SELECT PPSE command APDU to the card. After the card response the reader executes the card removal procedure. Once the card has been removed from the field the pre-validation application restarts from the beginning with polling for a card.

#### 3.1.5.2 File menu

Menu point “Exit” exit the application

#### 3.1.5.3 Menu point Help

The menu point help show the Version of the reader GUI.





**Figure 19** help screenshot

### 3.2 AS3911 EMV Firmware

The AS3911 EMV L1 certification firmware provides an example implementation of the EMV contactless communication protocol specification. It was used to get an EMV L1 certification for the AS3911 EMV demo system from an accredited test laboratory and can be used directly as a software module for customer specific EMV L2 applications or as a guideline to implement an EMV communication protocol stack.

#### 3.2.1 AS3911 EMV Firmware setup

The firmware consists of two main modules, the AS3911 module and the EMV module, respectively. The AS3911 module provides a driver for the AS3911 chip with support for special features required to implement EMV (e.g. dynamic modulation depth adjustment). The EMV module provides an implementation of the EMV contactless communication protocol stack on top of the AS3911 driver module. The picture, Figure 20 layer setup of EMVco reader system, gives an overview of the internal structure of these two modules.

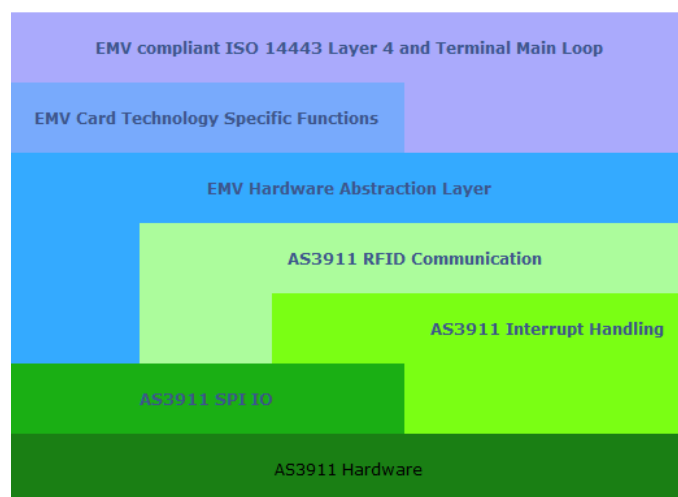


Figure 20 layer setup of EMVco reader system

#### AS3911

- AS3911 RFID Communication
- AS3911 Interrupt Handling
- AS3911 SPI IO

#### EMV

- EMV RFID Hardware Abstraction Layer.
- EMV Layer 4 and Example Terminal Application
- EMV Card Technology Specific Functions

Additionally to the modules depicted above, the firmware also has modules which are not directly related to the EMV protocol stack but provide utility functions which are used in various parts of the firmware. These modules are:

- LED driver
- sleep module

- USB communication with the PC

### **3.2.2 AS3911 RFID Communication**

This part of the AS3911 module consists of functions to configure parameters of the data transmission to and from an RFID card and functions to actually perform the transmissions.

#### **3.2.2.1 Receiver Deaf time**

After the data transmission from the reader is completed the receivers will be kept disabled until the receiver deaf time has expired. This deaf time ensures that the receiver does not pick up noise still present from the transmit operation.

For EMV the standard specifies that the PCD must ignore any load modulation produced by the PICC for a certain time immediately after the completion of the PCD message. The receiver dead time can be used to implement this EMV deaf time.

#### **3.2.2.2 Frame Delay Time**

The frame delay time is a forced delay between the end of the last message received from a card and the beginning of the next message send by the PCD.

#### **3.2.2.3 Receive Timeout**

The receive timeout specifies the time the AS3911 will wait for a card response after it has completed the transmission of the reader message. After the receive timeout expires the receiver will be disabled internally and no further card responses can be received. If a receive timeout occurs while a reception is in progress, then this reception continues until the message from the card has been completely received. So the receive timeout specifies a timeout for the start of the response from the RFID card.

#### **3.2.2.4 Error Handling**

To support EMV special error handling capabilities are built into the AS3911 RFID communication code.

If EMV error handling is disabled, then no special error handling takes place and any reception errors are reported.

If EMV error handling is enabled then a second parameter defines the details of the error handling namely the transmission error threshold. If a transmission error (parity error, crc error, error, data encoding error, or frame timing error) occurs during reception of a frame whose overall length is less than or equal to the transmission error threshold, then this received frame is ignored and the receiver is re-enabled to receive another card response. Also when EMV error handling is enabled then any frame with residual bits will be ignored no matter how long that frame was.

This is handled transparent to the caller. I.e. the caller will not be informed that an erroneous frame has been ignored. Instead either a timeout error is reported if no further frame follows

the ignored frame, or the content and error status of any frame received subsequent to the ignored one is reported.

### 3.2.2.5 Modulation Depth Adjustment

The AS3911 RFID communication module can adjust the modulation depth for the PCD to PICC communication based on the measured RF amplitude (on the RFI pins) or on the phase difference between the RFO and RFI pins. Both of these parameters depend on the coupling between the PCD and PICC antennas. So this provides a method to adjust the modulation depth based on the strength of the coupling between the PCD and PICC.

To adjust the modulation depth, the selected parameter is measured and then a table lookup is performed to derive the appropriate RF modulation on driver level. This lookup table defines a piece wise linear function. I.e. if the measured parameter value is not found in the table then a linear interpolation between the two closest values is performed. If the measured parameter value is out of the table range (either lower than the smallest x table value or higher than the highest x table value), then the RF on modulation driver level associated with the lowest or highest table entry is used.

### 3.2.2.6 Data Transmission and Reception

Data can be processed either by using [as3911Transmit\(\)](#) and [as3911Receive\(\)](#) directly as a two-step process or by calling [as3911Transceive\(\)](#). The latter of which will perform the complete transmit and receive operation and also allows to specify some additional options not available when using [as3911Transmit\(\)](#) and [as3911Receive\(\)](#) separately.

## 3.2.3 AS3911 Interrupt handling module

The AS3911 interrupt logic consists of three byte registers to mask or unmask interrupt sources and three additional registers to indicate which interrupts are pending. The content of this pending interrupt registers is automatically cleared on a register read. Additionally a single interrupt line is used to signal any interrupt pending interrupt condition to the microcontroller.

This module abstracts this so the user no longer needs to know to which interrupt register an interrupt source belongs to. To achieve this flat hierarchy of interrupt masks is provided. This module also serves any interrupt requests from the AS3911 and accumulates the pending interrupt requests until the user reads out the interrupt status ([as3911GetInterrupts\(\)](#), [as3911WaitForInterruptTimed\(\)](#)).

## 3.2.4 AS3911 SPI module

This module abstracts the SPI interface of the AS3911. It contains functions to read or write single registers:

- [as3911ReadRegister\(\)](#)
- [as3911WriteRegister\(\)](#)

to read or write a continuous block of registers in a single SPI operation (using AS3911 auto increment mode):

- [as3911ContinuousRead\(\)](#)

- `as3911ContinuousWrite()`  
to modify a register (performs a read, modify, write operation):
  - `as3911ModifyRegister()`
- to access the FIFO of the AS3911
  - `as3911ReadFifo()`
  - `as3911WriteFifo()`
- to send direct commands to the AS3911
  - `as3911ExecuteCommand()`
- and to access the test mode registers
  - `as3911ReadTestRegister()`
  - `as3911WriteTestRegister()`

All SPI data transfers are guaranteed to be completed after any of the function returns. But do note that the execution of a direct command might take some time to complete even after the transmission of that command is completed.

### 3.3 *EMV module*

#### 3.3.1 EMV RFID Hardware Abstraction Layer.

This module abstracts the RFID hardware in use from the EMV L1 contactless communication protocol stack. Any access to the RFID hardware from the EMV module is done via the API provided by this HAL. This allows adapting to future RFID chips from AMS with only minimum changes to the EMV software.

#### 3.3.2 EMV compliant ISO 14443 Layer 4 and Terminal Main Loop

This module contains the EMV layer 4 stacks, an example implementation of the EMV terminal main loop, and some examples for EMV terminal applications.

The ISO 14443 layer 4 implementation of the EMV stack consists of only two functions.

A function to initialize the ISO 14443 layer 4: [emvInitLayer4\(\)](#). This must be used after successful activation of a PICC to initialize the ISO14443-4 half duplex protocol stack.

And one function to communicate with a card on ISO 14443 layer 4 (in the context of APDUs): [emvTransceiveApu\(\)](#). This function deals with all the timeout, error handling, and retransmission requirements of the EMV contactless communication protocol and thus provides a transparent way to transmit an APDU to the RFID card and receive any RPDU send by the card in response.

##### 3.3.2.1 Example EMV Terminal Application Main Loop

The example terminal application main loop is intended as a blue print which shows how different parts of the EMV software stack should be used together to implement an EMV standard compliant terminal application.

The function [emvStartTerminalApplication\(\)](#) will start an EMV terminal main loop as defined in the EMV standard. This main loop polls for cards until a card can be successfully activated

and then transfers control to the specified application callback to perform the payment application. After the application callback returns a card removal is executed. Once the RFID card has been removed from the field the terminal main loop starts over again and polls for a new card.

This example terminal main loop continues to run until a call (from another thread) is made to [emvStopTerminalApplication\(\)](#). The emv layer does not check for terminal application stop requests while an RFID data transmission is in progress. Therefore it can take up to 5 seconds until a stop requests leads to the termination of the terminal main loop (about 5 seconds is the maximum allowed timeout for a single block transmission on layer 4).

### 3.3.3 EMV Card Technology Specific Functions

This module contains RFID operations which are typically available on ISO14443-A and ISO14443-B cards. But, due to differences between these two card technologies it is not possible to provide a single implementation for both technologies.

This operations include:

- Presence detection: Used by the polling loop to detect the presence of cards from a specific technology ([emvTypeACardPresent\(\)](#), [emvTypeBCardPresent\(\)](#)).
- Singulation: Used after cars of one technology only have been found to ensure that only one card of that technology is present in the reader field ([emvTypeAAnticollision\(\)](#), [emvTypeBAnticollision\(\)](#)).
- Card activation: Used to activate the ISO14443-4 layer on an already singulated card ([emvTypeAActivation\(\)](#), [emvTypeBActivation\(\)](#)).
- Card removal: Used to detect physical removal of the card from the reader field after a payment transaction is completed ([emvTypeARemoval\(\)](#), [emvTypeBRemoval\(\)](#)).

The activation and removal operations can also be used via the callbacks provided by [EmvPicc\\_t](#) after anticollision has been completed successfully.

## 3.4 AS3911 EMV reader debug option

The GUIs main purpose is to act as a Device Test Environment for the EMV L1 certification. So it only contains minimum user feedback. But, the AS3911 EMV reader actually outputs more data via the additional UART debug output.

To connect to the UART debug output connect to pin 3 (GND) and pin 7 (UART TX) of the 8 pin header on the AS3911 EMV reader PCB. On these pins you will have a 3.3V signal level 115200baud 8N1 serial data stream with detailed output from the command being executed.

The UART use 3.3 Volt levels and we recommend using a cable with integrated USB/UART converter like the TTL-232R-3V3-WE from FTDI.

### 3.4.1 Hardware Configuration

Following picture show the Controller board from top view. The programming and UART connector is P5, which is on the lower left side.

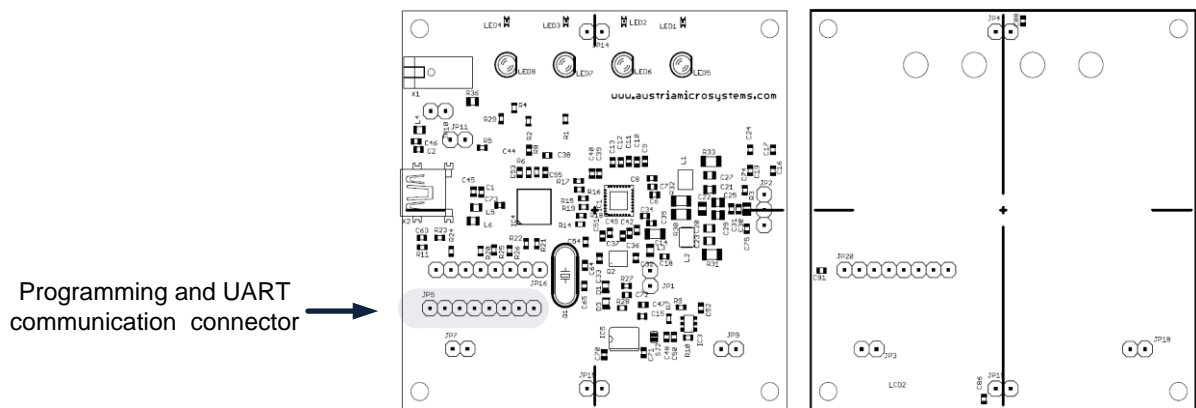
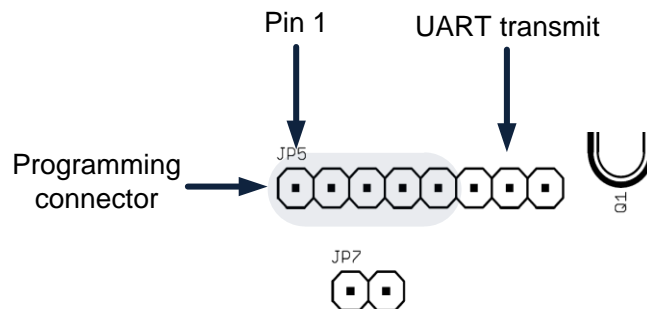


Figure 21 Hardware of EMVco reference system

Pin 1 is on the corner and the UART-transmit channel is on pin 7 (RP2) GND connection is on pin3



### 3.4.2 Settings for UART

Examples are made with the software utility teraterm-4.71.  
The settings dialogue can be opened with Setup-->serial port.

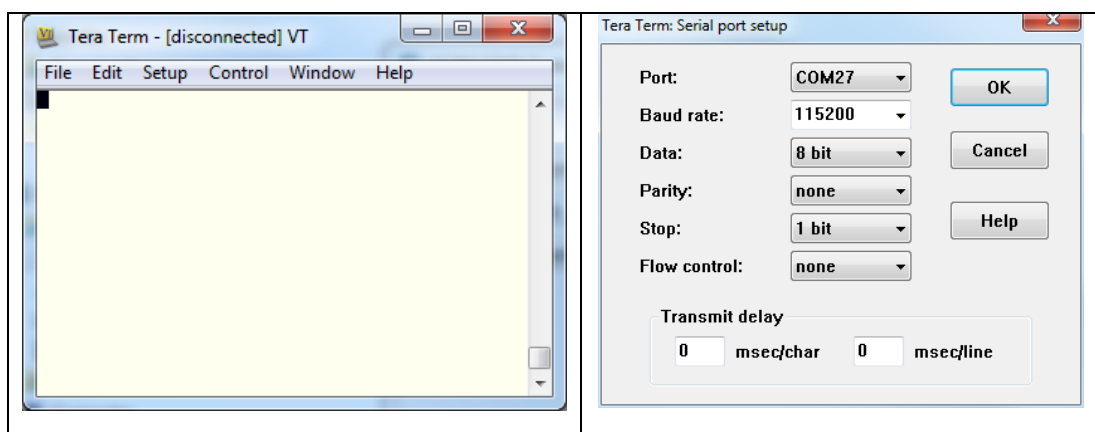


Figure 22, setting dialogue for terminal program

The settings for the connection with the AS3911 EMV reference design are 115k 8n1

After powering up, the reader display a status message of the firmware

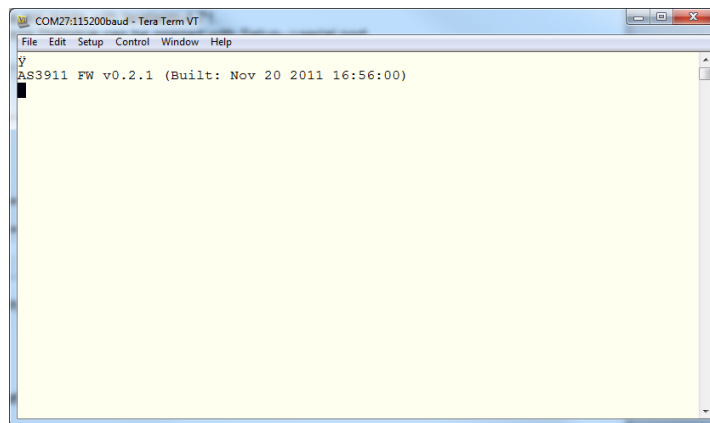


Figure 23, Status message of the EMVco reader

## 4 Test of the reader system

The test of the reader system can be done with the prevalidation function. In this function, the reader scans for a card and display the UID once it is found.

Following screen shows the sequence:

1. Powering the board
2. Start prevalidation in the GUI
3. Move the card in the proximity of the reader
4. Remove the card
5. Stop the prevalidation

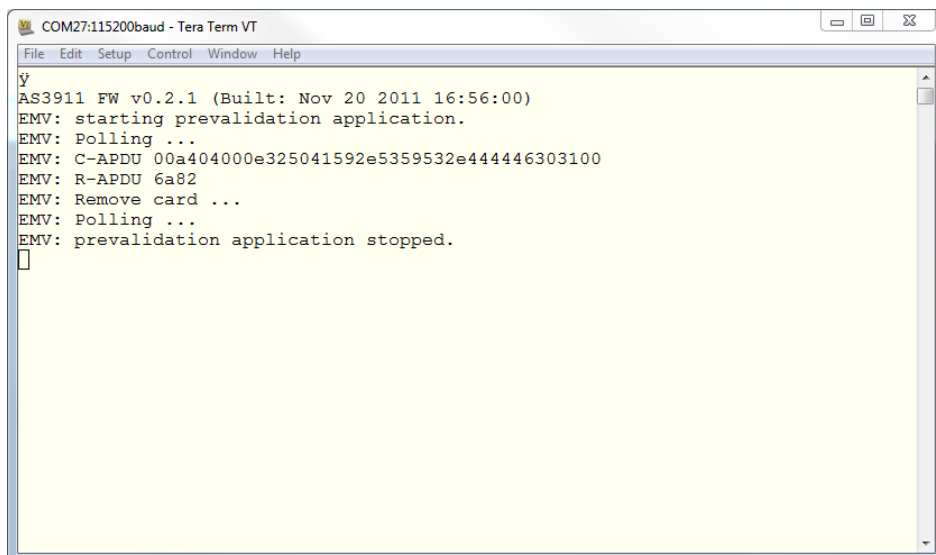


Figure 24, Test of EMVco reader



## 5 Appendix

### 5.1 Error handling procedures

EMVco describe a well-defined error handling behaviour which should ensure that the communication is not jeopardized due to the different operating states of the PICC ( EMD).

The AS3911 has an internal error handling features that takes care on the strict timing requirements of the error handling. The error handling can be grouped in the following sections.

#### 5.1.1 Detection of residual Bits

Residual Bits are additional information bits after the CRC that violates the definition of the ISO 14443 framing.

AS3911 receive the residual Bit and reports the length of the received frame Bits. Since the reception is composed out of complete bytes and in case of truncated bytes, the firmware can detect residual Bits.



Figure 25, residual Bit definition

#### 5.1.2 Deaf time Definition

The deaf time is defined as the time starting from the end of transmit until the begin of the receiving. The reader has to ignore all the data that are transmitted by the test environment during the deaf time. The tolerance on which the deaf time ends and the receiver must be ready to receive data is 9 us.

AS3911 has a timer that can be programmed and start at the end of transmission till the receiving is started.

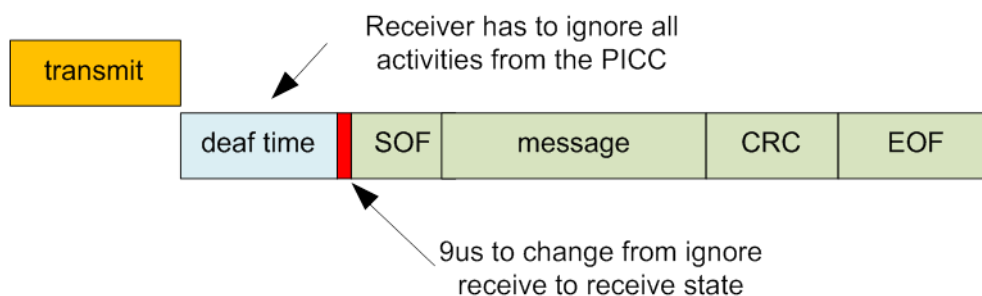


Figure 26 Deaf time definition

#### 5.1.3 Ignore faulty messages

The challenge is to pick the correct message within a certain time frame.

The AS3911 handle that requirement with continuation of the no response timer after the transmit frame. In case of a faulty message, the receive interrupt is executed and the firmware can restart he receiver.

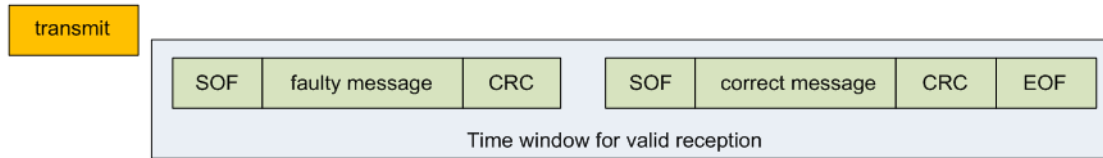


Figure 27, faulty message definition

### 5.1.4 Soft framing error

Soft frame errors are specified as errors that transport the correct message, but violate the standard definition by e.g. adding Bits to the preamble length.

The AS3911 detects soft framing errors and reports those.

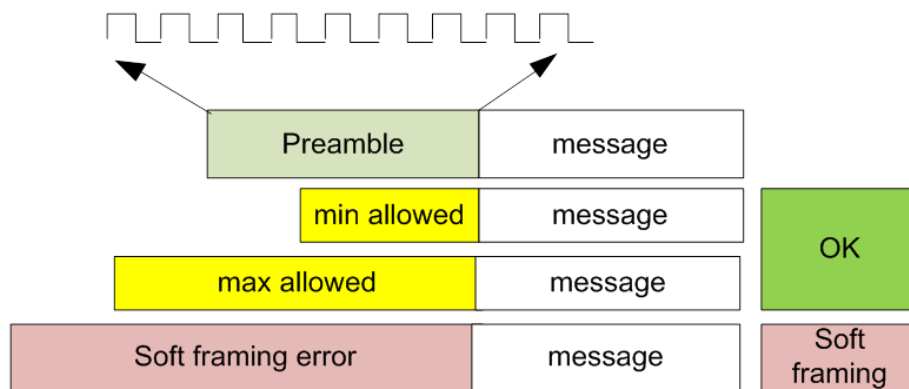
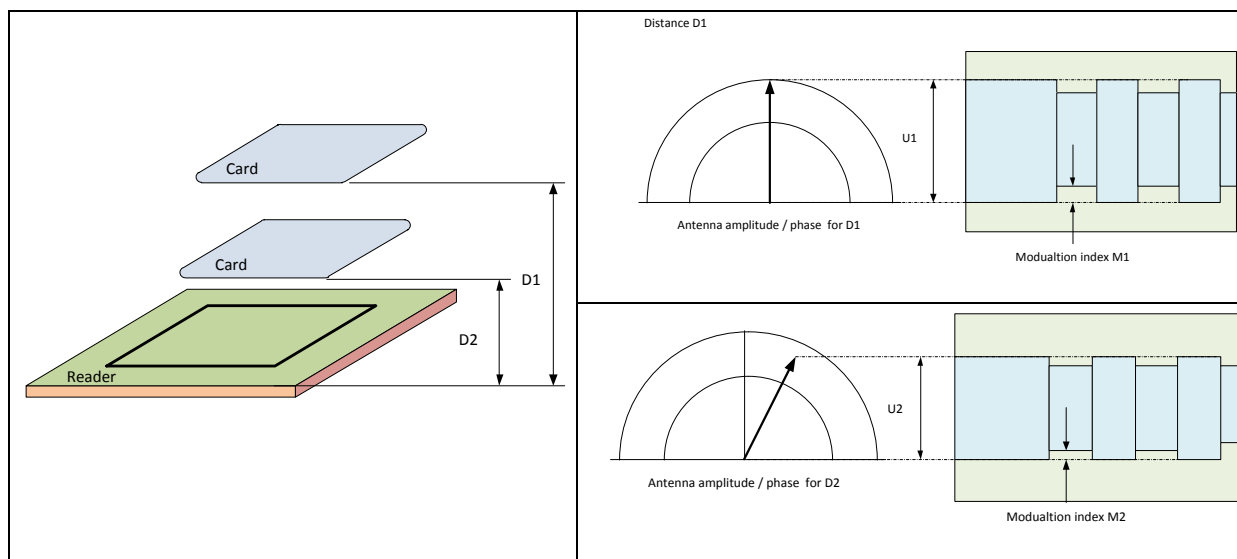


Figure 28 Soft framing error definition

## 5.2 Handling procedures for Type B load modulation

Type B modulation depth is described by EMVco specification and verification is part of tests. Since the card generates a feedback to the reader that changes the modulation depth of the reader system, The reader need to dynamically adjust the modulation depth in dependency the distance from the card to the reader. This is be done by measure the feedback on the tank circuit that the card generate. We are using the change of the resonance phase to detect the card distance.

Following picture will explain the behavior:



**Figure 29 modulation depth adjustment**

Left side show the different positions of the Tag in the field. The green block symbolize the reader and the blue one two possible positions of the card.

On position D1, the reader is assumed to be perfect tuned and the voltage on the reader is at its maximum and centered at 90 degree. The modulation depth is on its nominal value.

On position D2, the Tag is detuning the reader antenna and thus the voltage drop and changes the phase and also the modulation depth changes.

To compensate this change of modulation depth it is required to change the internal driver resistor of the modulated stage. AS3911 has a set of 8 transistors that has binary weighted Rdson. With correct setting of the transistors it is possible to adjust the modulation depth.

AS3911 offers an automatic level adjustment and a manual adjustment. In a known environment (like the EMV board) it is preferable to use the manual adjustment due to fast setting. Since the change of the modulation depth is proportional to the detuning, it is possible to generate a table that gives to each level of detuning a value of the modulation depth register.

This method requires a table of measurement values that needs to be measured in advance.

This table is generated with following steps:

- 1: measure the amplitude and phase of the unloaded board
- 2: put a card on the specified locations in the field and set the target modulation depth.
- 3: execute direct command calibrate modulation depth and note the value of amplitude/ phase and the register AM Modulation Depth Display Register.
- 4: proceed with a new location and step 2

The result is the table of modulation depth adjustment over phase and amplitude. This table will be used as a look up table prior each Type B send command to adjust the modulation depth.

Before each start of a Type B modulation, the amplitude or phase is measured and a corresponding value for the modulation depth is being set. For case in which the values are not explicit given, the values are linear interpolated between the closest amplitude/phase values.

In the EMVco reference firmware, the measurement of the amplitude is being used since the amplitude is changing more than the phase due to the card loading effect.

### 5.3 Controller programming procedure

The board contains a microchip PIC24FJ64GB002 controller. We propose to program the controller with the microchip MPLAB application suite that can be downloaded from the Internet.

After Installation, the Hex-file of the reader needs to be imported with the command File Import which will open a Box to search for the hex-file. The name of the hex file is AS3911\_EMV.hex

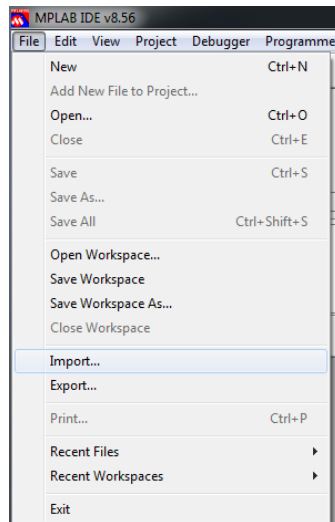


Figure 30 PIC MPLAB file dialogue

Next step is to connect the reader with the programming tool. We propose to use the PICKIT 3.

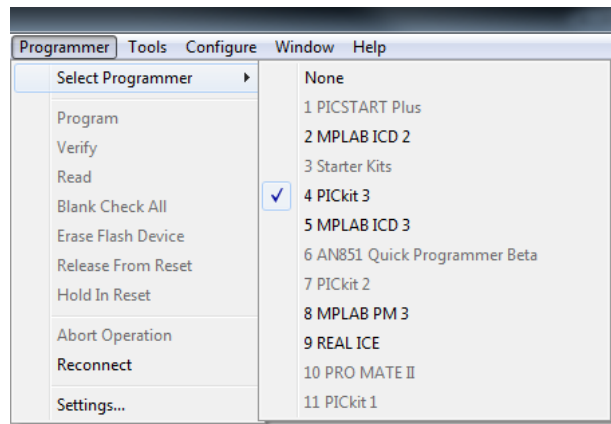


Figure 31 definition of programming tool

After connection is established, the proper controller type needs to be set. Open the Configure dialogue and select "select device" selection.

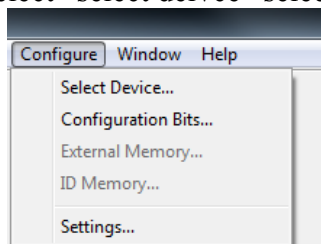
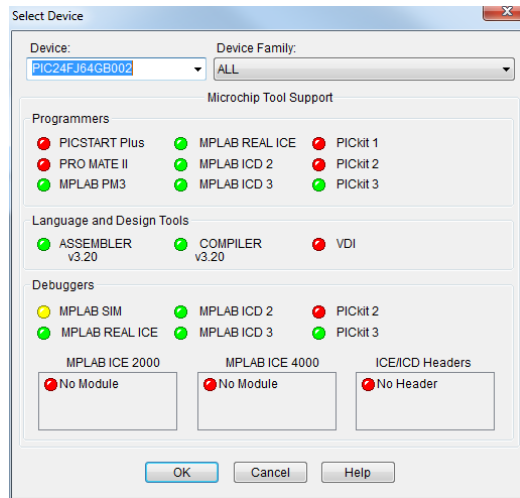


Figure 32 setting of the used controller type

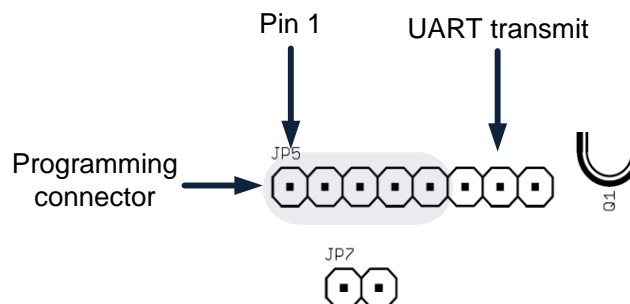


**Figure 33 Controller type selection**

Now you are ready to program the device.

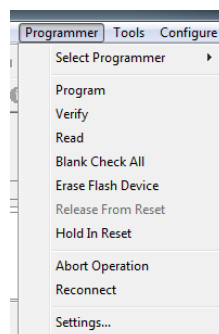
The programming connector is as well JP5

Connect the Pin one of the tool with the Pin one of JP5 from the board.



**Figure 34 Programming header position**

Activate the program selection will program the device.



**Figure 35 start of programming dialogue**

## **5.4 EMC considerations**

For rejection of EMC due the rectangular carrier field generation, special considerations need to be done in:

### **5.4.1 Power supply noise rejection.**

Noise rejection from USB is done with ferrite beads on the input and a LDO on the RF driver stage.

### **5.4.2 Antenna coil**

The HF antenna usually is a good radiating antenna for UHF due to its large dimension. Two options can be considered to shield the antenna. One is using an additional grounded PCB trace that covers the whole antenna space and is on an additional layer. The idea of that shield is to shortcut the UHF signals. The disadvantage of such solution is that the HF field strength will be jeopardized due to the eddy currents. Another option, and used on this design is to partially shield the antenna with capacitors to ground.

### **5.4.3 EMC filter**

The EMC filter is composed out of the components L1 and C20..C23 and C27 and damp the higher harmonics. Precaution on the self-resonance frequency of the filter coil needs to be made since it will change the behaviour above the self-resonance frequency. An additional criterion is the ohmic resistor of the coils at 13.56 MHz since that resistor is in series with the driver stage and thus will reduce the power.

### **5.4.4 Layout considerations**

There must be a ground plane under the device which dissipates the heat. The layout of the antenna traces must be done as symmetrical as possible and it is recommended to shield the the HF path against the remaining layout with ground vias.

## **5.5 Adaption to different controller platform**

The EMV firmware was written as a demo application. It therefore does not make use of an RTOS and was designed to run as the only application on the target platform. Nevertheless the design of the firmware should limit required changes mostly to the AS3911 module and to the emv\_io.[ch] files (which implement access from the EMV layer to the RFID hardware).

## 5.6 Reference Documents

The following reference materials may be of use to the reader of this report:

EMV Contactless Specification Requirements Reference Version

1: EMV Contactless Specifications for Payment Systems – Book D – EMV Contactless Communication Protocol Specification Version 2.1, March 2011

2: EMV Test Bench and Test Cases Requirements The following documents describe the test benches and test cases requirements used for the tests:

3: EMVCo Contactless Type Approval: PCD Analogue Test Bench and Test Case Requirements Version 2.1a, November 2011

4: EMVCo Contactless Type Approval: PCD Digital Test Bench and Tests Cases Requirements Version 2.1a, November 2011

5: EMVCo Contactless Type Approval: PCD Pre-validation Prior to Level 1 Testing Version 2.1a, November 2011

6: EMVCo Type Approval Test Report PCD template Version 2.1a, November 2011

7: AS3911 Datasheet: AS3911\_NDADatasheet\_EN\_v2.pdf

## 5.7 Revision Information

Revision	Change log	Initiator
0_01	Initial Version	tlu
0_02	Add Software infos, UART channel	tlu
0_03	Added Micro chip programming info	tlu
0_04	Changed Pictures to eagle layout, add Type B modulation index adjustment explanation	tlu
0_05	Add firmware description, error handling	tlu
0_06	Add reference documents, change firmware description, update to new GUI	tlu

## 6 Disclaimer

Devices sold by austriamicrosystems AG are covered by the warranty and patent identification provisions appearing in its Term of Sale. austriamicrosystems AG makes no warranty, express, statutory, implied, or by description regarding the information set forth herein or regarding the freedom of the described devices from patent infringement. austriamicrosystems AG reserves the right to change specifications and prices at any time and without notice. Therefore, prior to designing this product into a system, it is necessary to check with austriamicrosystems AG for current information. This product is intended for use in normal commercial applications. Applications requiring extended temperature range, unusual environmental requirements, or high reliability applications, such as military, medical life-support or life-sustaining equipment are specifically not recommended without additional processing by austriamicrosystems AG for each application.

The information furnished here by austriamicrosystems AG is believed to be correct and accurate. However, austriamicrosystems AG shall not be liable to recipient or any third party for any damages, including but not limited to personal injury, property damage, loss of profits, loss of use, interruption of business or indirect, special, incidental or consequential damages, of any kind, in connection with or arising out of the furnishing, performance or use of the technical data herein. No obligation or liability to recipient or any third party shall arise or flow out of austriamicrosystems AG rendering of technical or other services.

Copyright © 2011, austriamicrosystems AG, Schloß Premstätten, 8141 Unterpremstätten, Austria.

For further information please contact

The Wireless Business Line  
Schloss Premstaetten  
A-8141 Unterpremstaetten  
AUSTRIA  
Tel: +43-(0)3136-500-5473  
FAX: +43-(0)3136-500-4141  
[wireless@austriamicrosystems.com](mailto:wireless@austriamicrosystems.com)

Subject to change without notice