Next generation FPGA design software enables predictable design convergence with unparalleled ease of use for edge applications

The new Lattice Radiant software is a full featured FPGA design tool suite that's simple to use and is optimized for edge applications. It helps users achieve predictable FPGA design convergence with its unified design framework, rapid design exploration and timing closure capabilities. It also supports the latest industry standard IEEE1735 encryption and IP driven design flow to enrich customers' IP ecosystem support. In addition, it encompasses a redesigned user interface, highly interactive design cross probing functionality, and improved ease of use design flow. The software will significantly enable faster design closure and time to market. Lattice Radiant software is now available for download from Lattice's website, supporting both Windows and Linux. Once downloaded from the Lattice website, it can be used with a free license obtained through the License request process.

Broad Market Low Power Embedded Applications

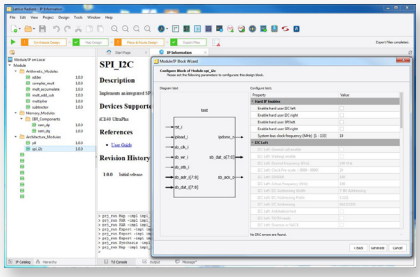
Lattice Radiant software aims to enable broad market low power embedded applications with the flagship iCE40 UltraPlus devices, the world's smallest FPGAs with enhanced memory and DSPs to enable always on, distributed processing for IoT edge applications. The software also comes pre-loaded with the necessary IPs to design for such applications.

Key Features and Benefits

- **Full Featured FPGA Design Tool Suite**
  - Predictable design convergence with unified design database, design constraint flow and timing analysis
  - Industry standard Synopsys Design Constraint (SDC) language provides support for maximum interoperability
- **Ease-of-Use Features**
  - Updated user interface provides simple, intuitive and efficient user operations
  - Ease of design navigation and debugging enabled by integrated tools set environment
  - Simple "One Click" design implementation execution enabled by a new Process Toolbar
  - Physical to logical design implementation cross-probing.
- **IP Security and Ecosystem**
  - Industry standard IEEE 1735 encryption support for IP protection
  - IP catalog provides easy access to IP cores optimized for supported Lattice devices

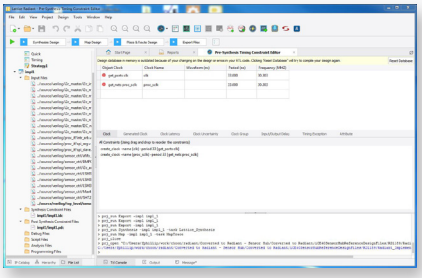
Lattice Radiant Key Tools

IP Catalog



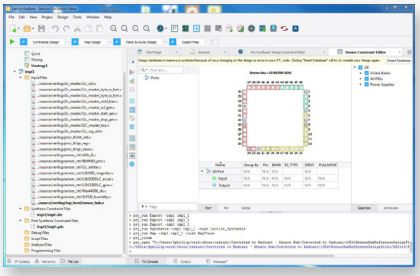
An interface to Lattice's catalog of modules and IPs optimized for Lattice devices

Timing Constraint Editor



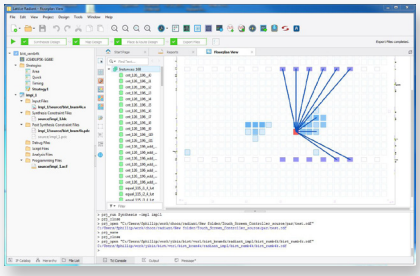
A tool to view and edit timing constraints before and after synthesis

Device Constraint Editor



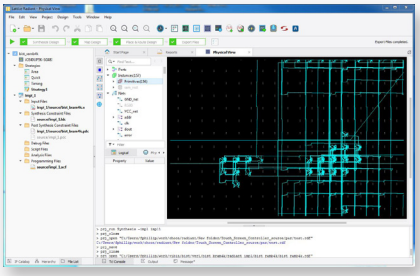
A tool to view and edit device level constraints such as I/Os, ports, global settings, etc.

Floorplan View



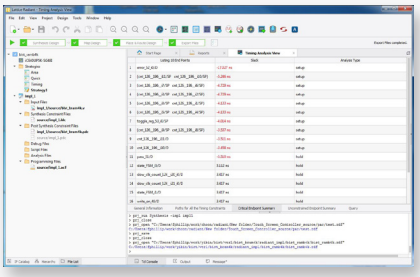
A tool to view design and edit placement constraint

Physical View



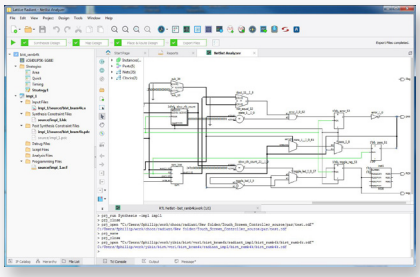
A detailed view of the physical routing paths to gain insights into timing issues

Timing Analysis



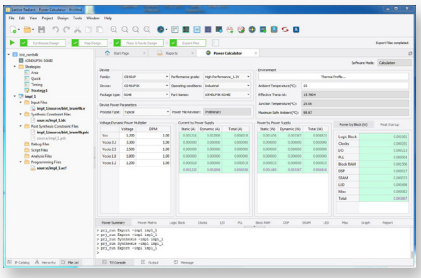
An interactive analysis of detailed timing paths to speed up the timing closure process

Netlist Analyzer



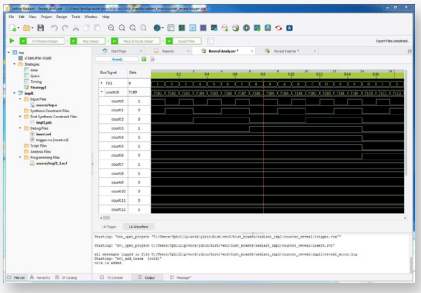
A detail schematic representation of the design before and after synthesis

Power Calculator



Accurate data driven power calculation and estimation based on silicon performance data

Reveal Hardware Debugger



A signal-centric debugger that allows easy insertion of embedded logic analyzer for real time hardware debugging

Applications Support
www.latticesemi.com/support

February 2018
Order #: I0264 Rev. 1