TB-KU-xxx-ACDC8K（Rev.2.xxx）
Hardware User Manual

Rev. 1.06

Revision History

Version	Date	Description	Publisher
Rev. 1.00	2014/10/15	Initial Release	DM
Rev. 1.01	2015/01/19	Updated content with board pictures and FMC pinout tables	DM
Rev. 1.02	2015/02/18	Updated Figure 4-1, 7-2, 7-6, 7-16	KM
Rev. 1.03	2015/07/21	Released for 060 Added Standoffs and Power Strip cord Updated Figure 5-1, 7-6, 7-8, 7-9, 7-12 Updated Table 7-16, 7-22, 7-23 Added 8.1 Default Settings	Morita Odajima
Rev. 1.04	2015/09/28	7.12.1. Updated DIP Switches polarity. (Slide in the ON position for a logic “Low”)	Morita
Rev. 1.05	2015/10/23	Changed FPGA device name from KU085 to KU115 Updated Figure 6-1, 6-2, 7-6, 7-8 Added comment for KU060 FMC4 GTH lanes and GTH reference clocks Updated Board accessories (Screw qty from 14 to 28) Added example constraint for User Assigned Clocks	Morita Odajima
Rev.1.06	2016/03/01	Updated Figure 5-1, 6-1, 7-1, 7-3, 7-13, 7-14, 7-16, 8-1 Updated Table 7-20, 7-22 Added 7.11 Note	Amano

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Introduction

Thank you for purchasing the **TB-KU-xxx-ACDC8K** board. Before using the product, be sure to carefully read this user manual and fully understand how to correctly use the product. First read through this manual, and always keep it handy.

SAFETY PRECAUTIONS

Be sure to follow these precautions

Observe the precautions listed below to prevent injuries to you or other personnel or damage to property.

- **Before using the product, read these safety precautions carefully to ensure proper use.**
- **These precautions contain serious safety instructions that must be followed.**
- **After reading through this manual, be sure to always keep it handy.**

The following conventions are used to indicate the possibility of injury/damage and classify precautions if the product is handled incorrectly.

Danger	Indicates the high possibility of serious injury or death if the product is handled incorrectly.
Warning	Indicates the possibility of serious injury or death if the product is handled incorrectly.
Caution	Indicates the possibility of injury or physical damage in connection with houses or household goods if the product is handled incorrectly.

The following graphical symbols are used to indicate and classify precautions in this manual.
(Examples)

	Turn off the power switch.
	Do not disassemble the product.
	Do not attempt this.

Warning	
	**In the event of a failure, disconnect the power supply.** If the product is used as is, a fire or electric shock may occur. Disconnect the power supply immediately and contact our sales personnel for repair.
	**If an unpleasant smell or smoking occurs, disconnect the power supply.** If the product is used as is, a fire or electric shock may occur. Disconnect the power supply immediately. After verifying that no smoking is observed, contact our sales personnel for repair.
	**Do not disassemble, repair or modify the product.** Otherwise, a fire or electric shock may occur due to a short circuit or heat generation. For inspection, modification or repair, contact our sales personnel.
	**Do not touch a cooling fan.** As a cooling fan rotates in high speed, do not put your hand close to it. Otherwise, it may cause injury to persons. Never touch a rotating cooling fan.
	**Do not place the product on unstable locations.** Otherwise, it may drop or fall, resulting in injury to persons or failure.
	**If the product is dropped or damaged, do not use it as is.** Otherwise, a fire or electric shock may occur.
	**Do not touch the product with a metallic object.** Otherwise, a fire or electric shock may occur.
	**Do not place the product in dusty or humid locations or where water may splash.** Otherwise, a fire or electric shock may occur.
	**Do not get the product wet or touch it with a wet hand.** Otherwise, the product may break down or it may cause a fire, smoking or electric shock.
	**Do not touch a connector on the product (gold-plated portion).** Otherwise, the surface of a connector may be contaminated with sweat or skin oil, resulting in contact failure of a connector or it may cause a malfunction, fire or electric shock due to static electricity.

Caution	
	Do not use or place the product in the following locations. • Humid and dusty locations • Airless locations such as closet or bookshelf • Locations which receive oily smoke or steam • Locations exposed to direct sunlight • Locations close to heating equipment • Closed inside of a car where the temperature becomes high • Staticky locations • Locations close to water or chemicals Otherwise, a fire, electric shock, accident or deformation may occur due to a short circuit or heat generation.
	Do not place heavy things on the product. Otherwise, the product may be damaged.

■ Disclaimer

This product is an evaluation board intended for development of video data with Xilinx Kintex UltraScale FPGA. Tokyo Electron Device Limited assumes no responsibility for any damages resulting from the use of this product for purposes other than those stated.

Even if the product is used properly, Tokyo Electron Device Limited assumes no responsibility for any damages caused by:

(1) Earthquake, thunder, natural disaster or fire resulting from the use beyond our responsibility, acts by a third party or other accidents, the customer's willful or accidental misuse or use under other abnormal conditions.
(2) Secondary impact arising from use of this product or its unusable state (business interruption or others)
(3) Use of this product against the instructions given in this manual.
(4) Malfunctions due to connection to other devices.

Tokyo Electron Device Limited assumes no responsibility or liability for:

(1) Erasure or corruption of data arising from use of this product.
(2) Any consequences or other abnormalities arising from use of this product, or
(3) Damage of this product not due to our responsibility or failure due to modification

This product has been developed by assuming its use for research, testing or evaluation. It is not authorized for use in any system or application that requires high reliability.

Repair of this product is carried out by replacing it on a chargeable basis, not repairing the faulty devices. However, non-chargeable replacement is offered for initial failure if such notification is received within two weeks after delivery of the product.

The specification of this product is subject to change without prior notice.

The product is subject to discontinuation without prior notice.

1. Related Documents and Accessories

Related documents:

All documents relating to this board can be downloaded from our website. Please see attached paper on the products.

Xilinx FPGA document:

http://www.xilinx.com/support/index.html/content/xilinx/en/supportNav/silicon_devices/fpga/kintex-ultrascale.html

DS892: UltraScale device data sheets: Kintex UltraScale Architecture Data Sheet: DC and AC Switching Characteristics
DS890: UltraScale Architecture and Product Overview
UG570: UltraScale Architecture Configuration User Guide
UG571: UltraScale Architecture SelectIO Resources User Guide
UG572: UltraScale Architecture Clocking Resources User Guide
UG573: UltraScale Architecture Memory Resources User Guide
UG574: UltraScale Architecture Configurable Logic Block User Guide
UG575: UltraScale Architecture Packaging and Pinouts User Guide
UG576: UltraScale Architecture GTH Transceivers User Guide
UG580: UltraScale Architecture System Monitor User Guide
UG583: UltraScale Architecture PCB and Pin Planning User Guide
PG150: UltraScale Architecture-Based Memory Interface Solutions Product Guide

Board accessories:

- Power supply brick (DC 12V) and cable to board: qty. 1
- FMC spacer set
  Standoff 2.6M x 30mm qty. 14
  Screw 2.6M x 6mm qty.28
- Power Strip Cord with Individual Switches qty. 1

2. Overview

The TB-KU-xxx-ACDC8K evaluation board for the Xilinx Kintex UltraScale provides a hardware environment with a purpose of evaluating and developing designs targeting the Kintex UltraScale XCKU060 and XCKU115 featuring a FFVA1517 package. Speed grade -2 FPGA is mounted on this board. The TB-KU-xxx-ACDC8K platform provides a common feature set including DDR4 SDRAM memory components, general purpose I/O, a USB to UART interface, four SFP+ modules, seven VITA-57 high-pin count FPGA mezzanine cards (FMC) connectors, a JTAG and a PMOD interface.

This document is applied to TB-KU-xxx-ACDC8K（Rev.2.xxx）.

Feature	
Xilinx Kintex UltraScale:	XCKU060/XCKU115 -2 speed grade in FFVA1517 package
Memory:	4GByte DDR4 SDRAM: 16Gbits (4 ICs x 32M words x 16 bits x 8 banks) x 2 banks of ICs
	256Mbit Dual Quad SPI Flash
	TI's UCD9090 power supply sequencer and monitor
FMC Connector:	7 x Samtec's ASP-134486-01 (CC-HPC-10)*1
On Board Clocks:	IDT's ICS849N202I clock generator
	IDT ICS849N202I PLL
	25MHz CMOS oscillator
	40MHz crystal
	IDT 148.50MHz LVDS oscillator
	IDT 156.25MHz LVDS oscillator
	IDT 200.00MHz LVDS oscillator
Interface:	4x SFP+ modules
	MMCX for external clocks
	Standard Xilinx JTAG 14-pin header
	Digilent Pmod™ compatible header (2x6)
	Push switches, DIP switches, jumpers and LEDs
	Single-chip USB to UART bridge
	Micro-USB 2.0 Type AB connector

Note *1: Refer to VITA 57 FMC Standard http://www.samtec.com/standards/vita.aspx

3. Block Diagram

The following figure shows the block diagram of TB-KU-xxx-ACDC8K

FMC0 does not have any high-speed GTH lanes.

XCKU060:

FMC1, 2 and 3 have 8 high-speed GTH lanes.

FMC4(*2) and 6 have 4 high-speed GTH lanes.

FMC5 and SFP+ do not have any high-speed GTH lanes.

XCKU115:

FMC1, 2, 3, 4 and 5 have 8 high-speed GTH lanes.

FMC6 and SFP+ have 4 high-speed GTH lanes.

There are two groups of FMC HP connections, LA group A and group B. LA group A has 72 I/O connected to the FPGA and group B has 12.

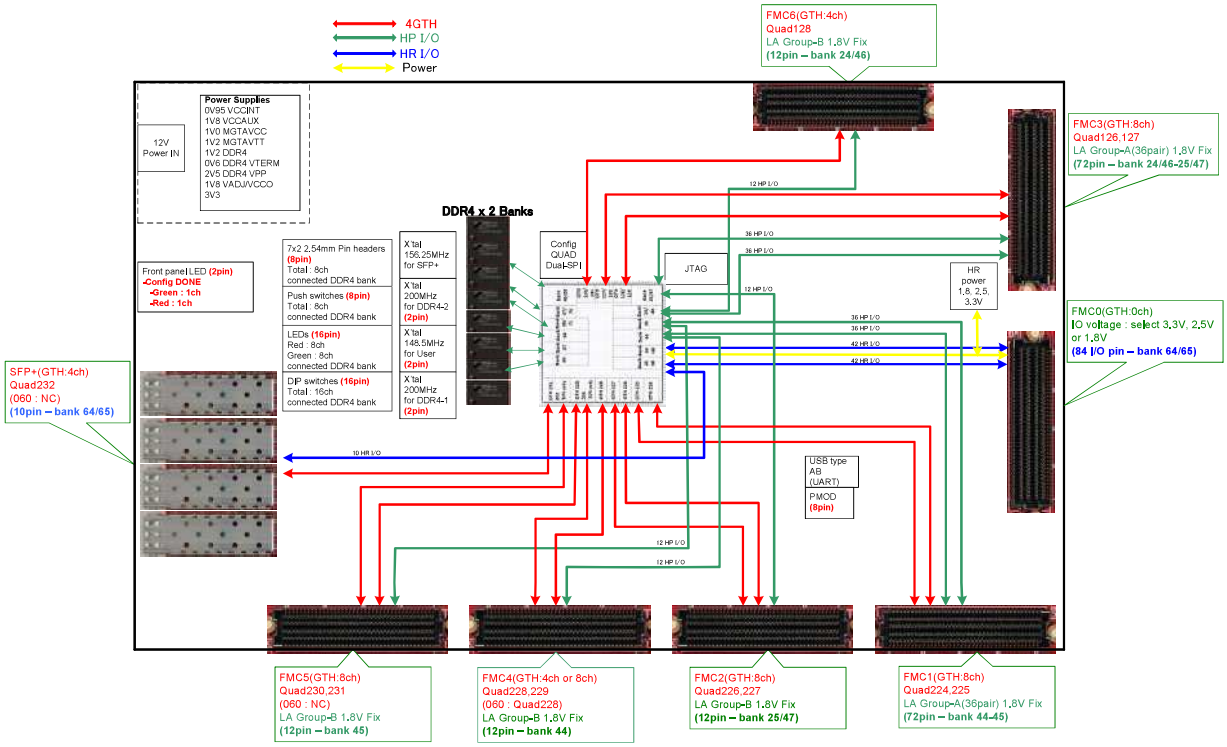
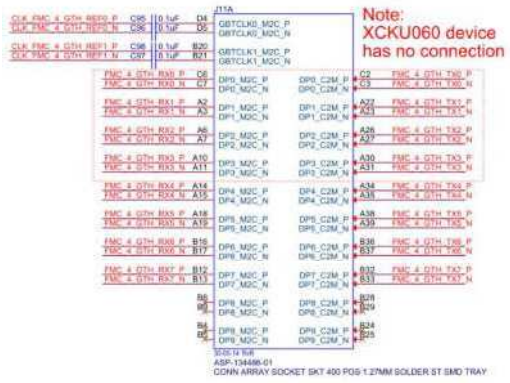


Figure 3-1 Block Diagram

*2 FMC4 connects DP4, DP5, DP6, and DP7 at XCKU060 device. (DP0, DP1, DP2, and DP3 are not connected)



4. External View of the Board

The TB-KU-xxx-ACDC8K board's components are shown on the top side view in Figure 5-1.

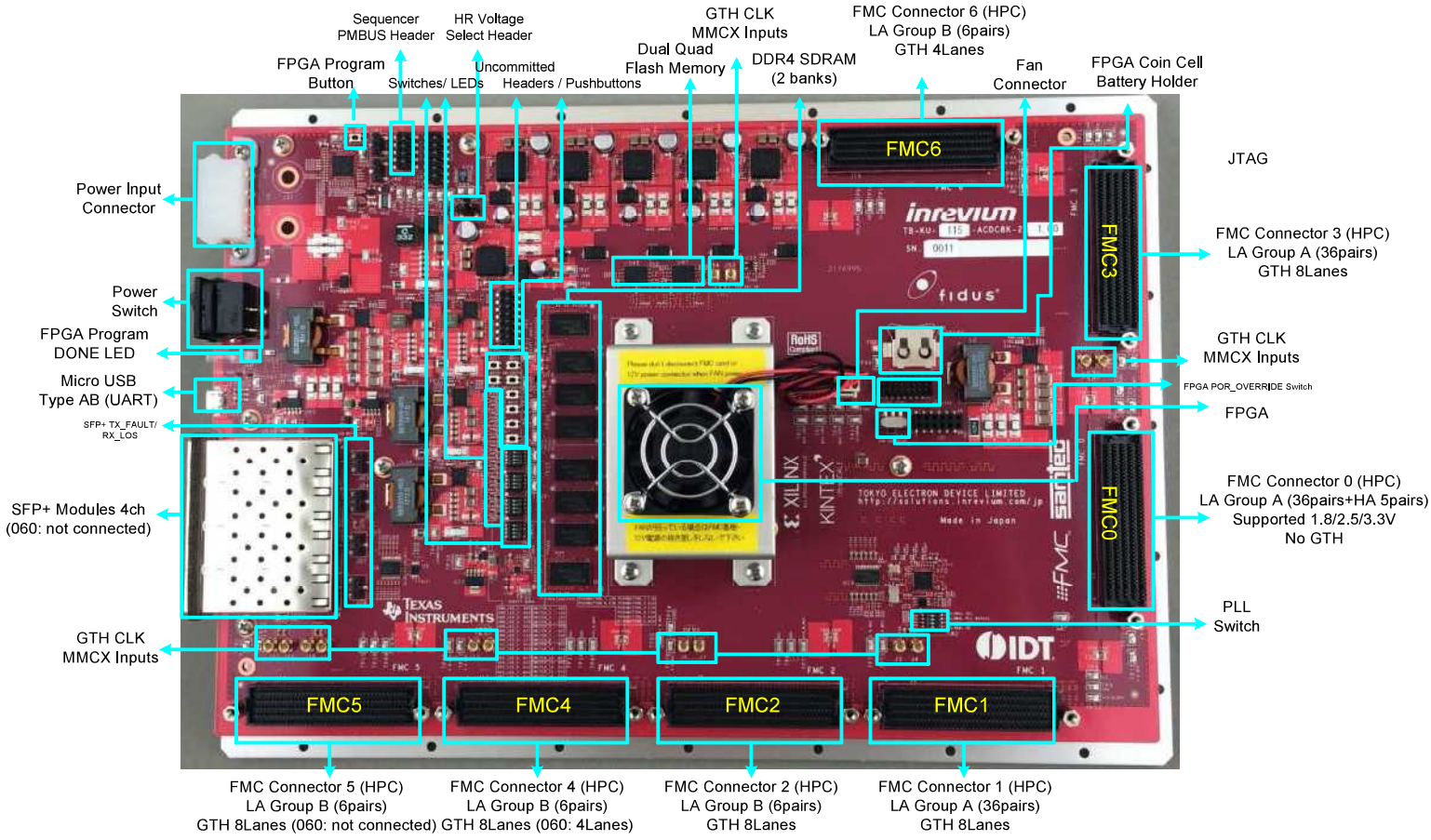


Figure 4-1 Board Top View

5. Board Specifications

Figure 6-1 shows the board specifications.

External Dimensions:	313.08 mm (W) x 208.28 mm (H)
Number of Layers:	20 layers
Board Thickness:	2.0828 mm +/- 10%
Material:	Megtron 4
FPGA:	Xilinx Kintex UltraScale XCKU060/XCKU115
	FFVA1517 (FLVA1517) package
FMC HPC CC Connector:	Samtec ASP-134486-01
Micro-USB Connector:	Hirose Electric's ZX62D-AB-5P8
Xilinx JTAG Connector:	Molex's 87832-1420
Pmod Connector:	Molex's 15912120
Power Input Connector:	TE Connectivity's 1-350948-0
	Emerson Network's 111-0702-001 and 111-0703-001

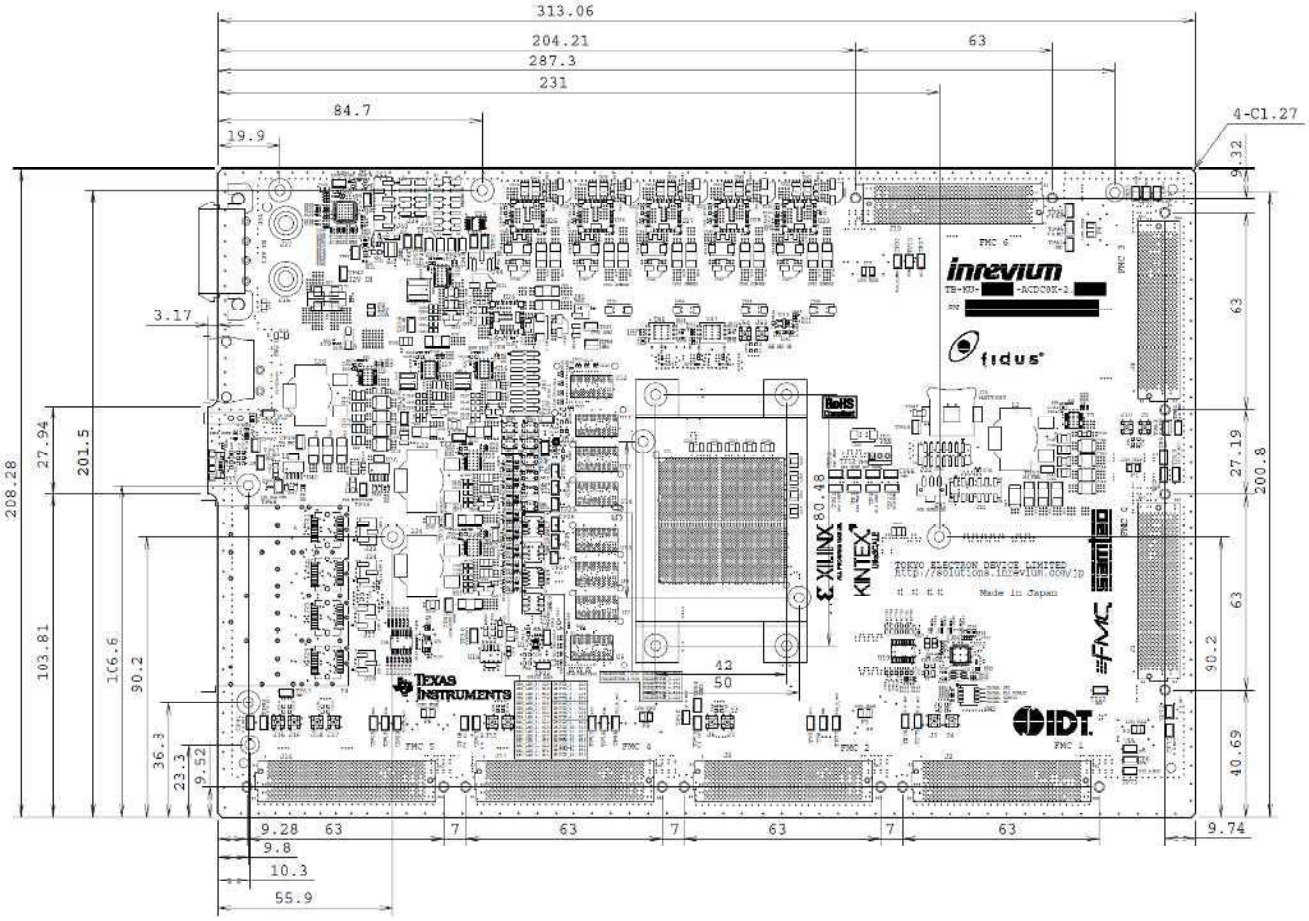


Figure 5-1 Board Dimensions (inclusive of wastable substrate, top view)

6. Description of Components

6.1. Power Supply Structure

TB-KU-xxx-ACDC8K board's power supply structure is shown in the figure below.

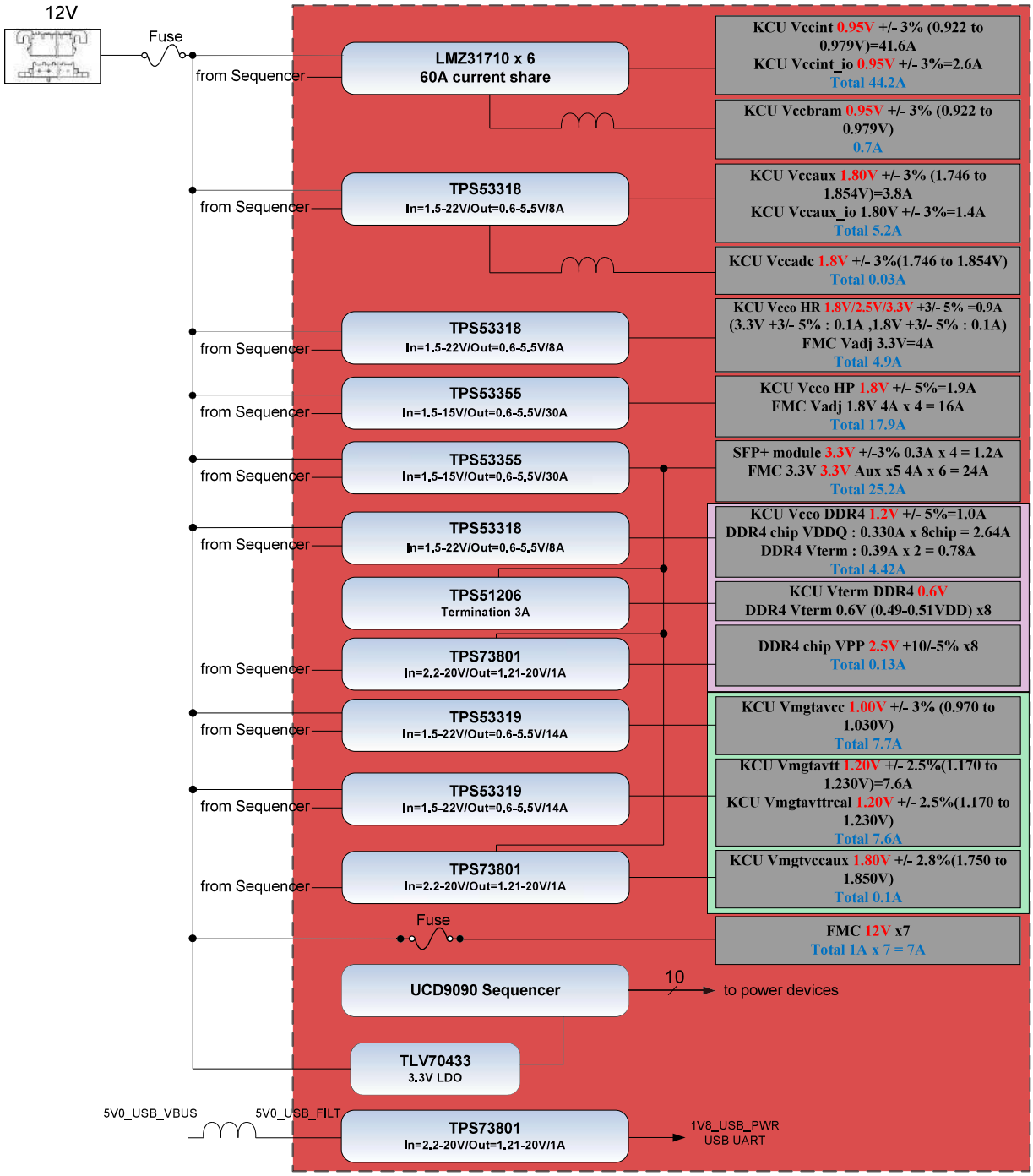


Figure 6-1 Power Supply Structure

6.1.1. Power Sequencing

The UCD9090 chip features power sequencing and monitoring of the different power supplies available on this board. The sequencer's outputs are connected to the power supplies' enable pin which activates each device.

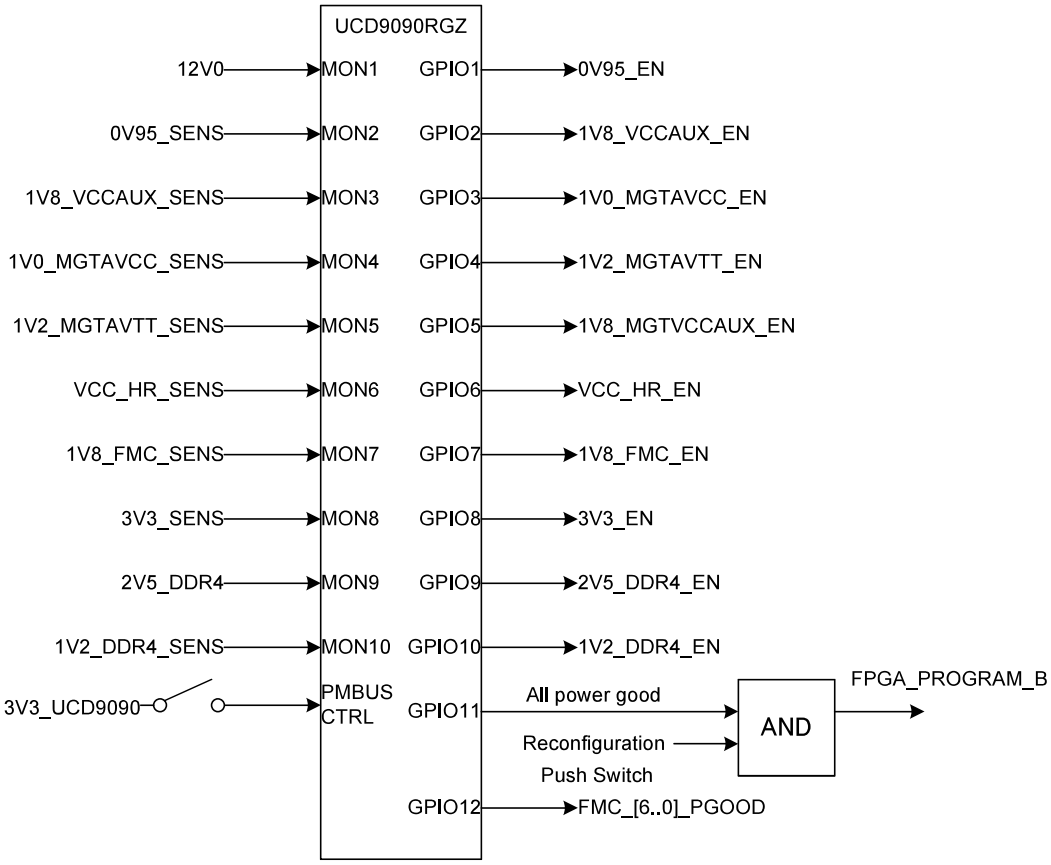


Figure 6-2 Power Sequencer

6.1.2. Power Input connectors

TB-KU-xxx-ACDC8K has two power input connectors on the board, a 4-pin header **or** red and black binding posts.

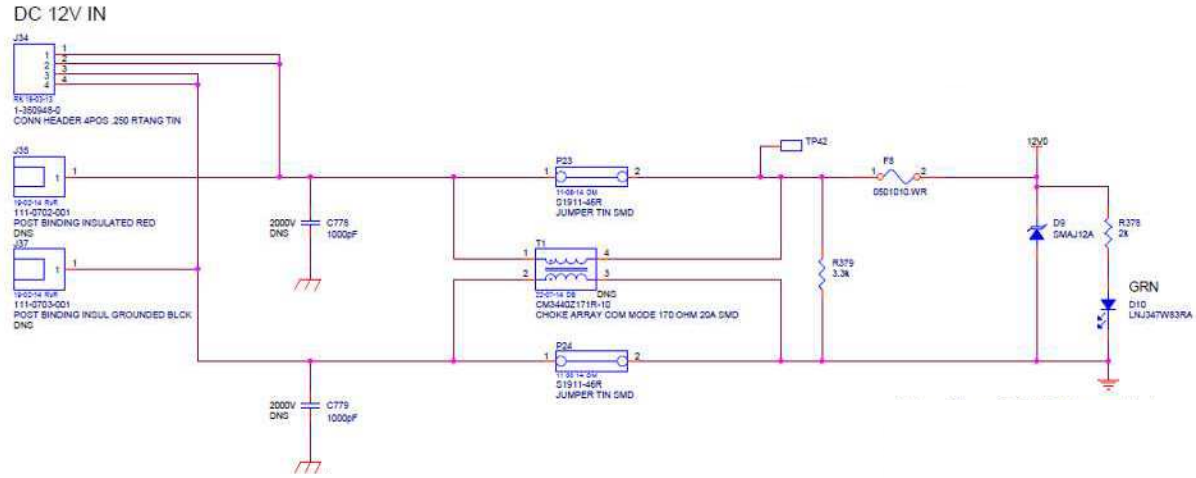


Figure 6-3 Power Input Circuit

6.1.3. Voltage Rails Test Points

Use the development board's power rail test points for board debugging and troubleshooting or for other types of measurements.

Table 6-1 Voltage Rails Test Points

Voltage Rail	Test Point #	Power Supply for
0V95	TP37	FPGA VCCINT
0V95_VCCBRAM	TP23	FPGA VCCBRAM
1V8_VCCAUX	TP40	FPGA VCCAUX & VCCAUX_IO
3V3_VCC_HR	TP36	FPGA HR I/O Banks
3V3_UCD9090	TP43	Power Sequencer and Monitor
1V8_FMC	TP19	FPGA HP I/O Banks & FMC VADJ
1V2_DDR4	TP31	DDR4 and corresponding FPGA Banks
2V5_DDR4	TP30	VPP generation
0V6_VTT_DDR4	TP32	DDR4 SDRAM 1 Termination
0V6_VREF_DDR4	TP34	DDR4 SDRAM 1 Reference
0V6_VTT_DDR4_2	TP33	DDR4 SDRAM 2 Termination
0V6_VREF_DDR4_2	TP35	DDR4 SDRAM 2 Reference
1V0_MGTAVCC	TP39	FPGA MGTAVCC
1V2_MGTAVTT	TP41	FPGA MGTAVTT
1V8_MGTVCCAUX	TP38	FPGA MGTVCCAUX
3V3	TP20	FMC and SFP+ modules
12V0	TP42	12V Master Power
VBATT	TP68	Coin Cell Battery
5V0_USB_VBUS	TP57	Micro USB 5V input
5V0_USB_FILT	TP59	Micro USB filtered 5V
1V8_USB_PWR	TP58	USB UART controller 1.8V I/O

6.1.4. Power and Miscellaneous LEDs

Shown below are the different LEDs present on the board which serve as power indication or general purpose programmable LEDs.

Table 6-2 Board LEDs

LED	Color	Used for
D1	Bicolor: Green or Red	FPGA Programming DONE signal Red: Programming in progress Green: Programming complete
D3	Green	Clock generation LOCK_IND indicator for U20
D4	Red	Clock generation CLK0 BAD indicator for U20
D5	Red	Clock generation CLK1 BAD indicator for U20
D6	Red	Clock generation XTAL BAD indicator for U20
D10	Green	12V Input
D12-D27	Green & Red	Uncommitted Green: D12, D13, D16, D17, D20, D21, D24, D25 Red: D14, D15, D18, D19, D22, D23, D26, D27

6.1.5. Board Power Button

This board features a power button rocker switch on the chassis' front panel along with 4 SFP+ connectors, a micro USB port and a green and red LED to signal the FPGA programming and idle states. The power sequencer monitors the rocker switch power button which disables power supplies on the board when turned off. The "I" position turns ON the power supplies and the "O" position turns them OFF. The FPGA's fan however will be active as long as the 12V supply is live.

Figure 6-4 Board Power Button

6.1.6. FPGA HR Bank Voltage Selection

Various different devices are connected on the FPGA HR banks. The FMC0 connector and SFP+ modules are connected to the FPGA's HR 64 and 65 banks as shown in blue on this board's block diagram (Figure 4-1). The SPI flash components are connected to HR bank 0 and bank 65.

Banks 0, 64 and 65 have a selectable voltage which is identical on these three banks.

Table 6-3 HR Banks Connected Peripherals

Bank #	Connected Peripherals	Voltage
Dedicated Config 0	Dual Quad SPI Flash (Primary)	Selectable 1.8V, 2.5V, 3.3V
HR 64	FMC0, SFP 1 and 2	
HR 65	FMC0, Dual Quad SPI Flash (Secondary), SFP 3 and 4	

6.1.7. HR Banks Voltage and SFP+ RX_LOS/TX_FAULT Selection

The 3V3_VCC_HR power can be selected through the use of a 3-pin jumper (J44).
The user can also select between RX_LOS or TX_FAULT on each of the 4 SFP+ modules.

Table 6-4 HR Banks Voltage and RX_LOS/TX_FAULT Selection

Jumper No.	Description	Status	Function
J44	HR Banks Voltage Select	No Jumper	1.8V (Default)
		1-2	2.5V
		3-2	3.3V

6.2. FPGA Banks Assignments

This board supports Xilinx Kintex Ultrascale XCKU060 and XCKU115 FPGA in the FFVA1517 (FLVA1517) packages. The figure below presents bank assignments on this board.

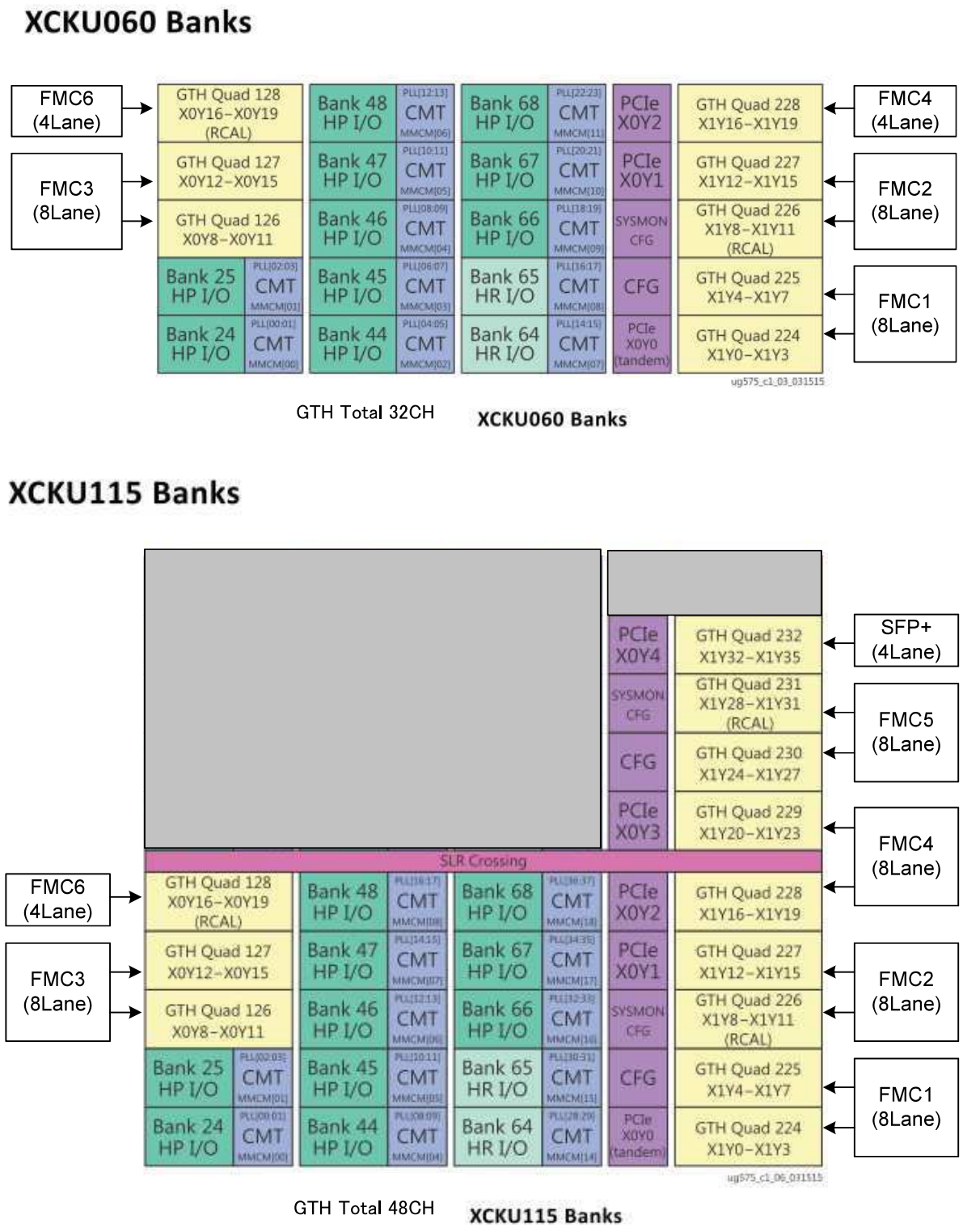


Figure 6-5 FPGA Banks Assignments

The reference clock sharing via North and South GTH Bank is limited within its own super logic region (SLR), so FMC4 cannot share reference clock between Bank228 and Bank229. (About FMC GTH reference clock connection, please refer to 7.3.2 GTH Clocks section)

6.3. Clock System

6.3.1. VCCINT Clock Architecture

The diagram below represents the clocking architecture of 6 - LMZ31710 modules interconnected to provide 60A output current sharing for the FPGA. The LTC6909 chip provides phase synchronized outputs with 60° offsets.

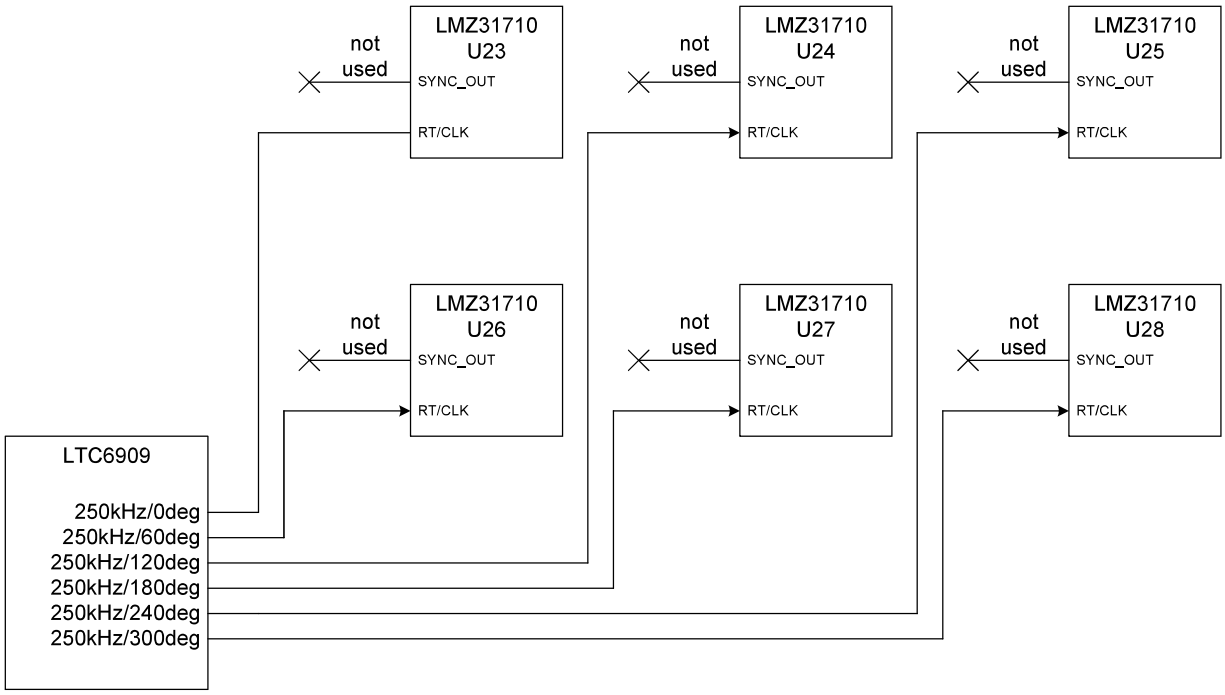


Figure 6-6 VCCINT Clock Synchronization

6.3.2. GTH Clocks

The diagram below represents the GTH clock architecture present in the TB-KU-xxx-ACDC8K board. Some clocks are internally driven by the system while others can be externally provided through MMCX connectors.

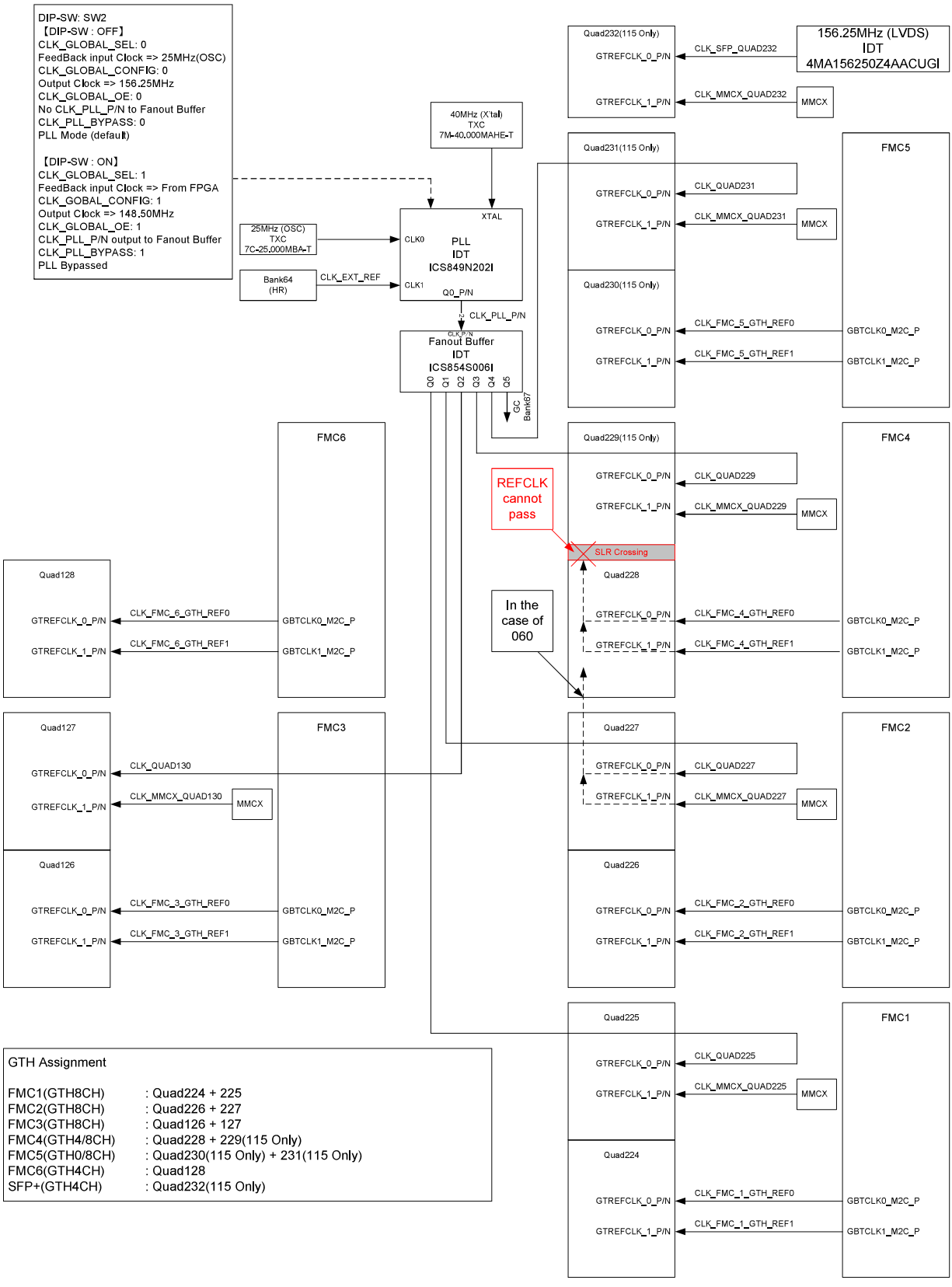


Figure 6-7 GTH and MMCX Clocks Architecture

6.3.3. User Assigned Clocks

This board provides a way to make use of dedicated LA signals on the FMC cards allowing them to be configured as global clocks on the FPGA as shown in the figure below. The figure states the GC and GBC clock assignments on the FPGA for the FMCs and the DDR4 banks.

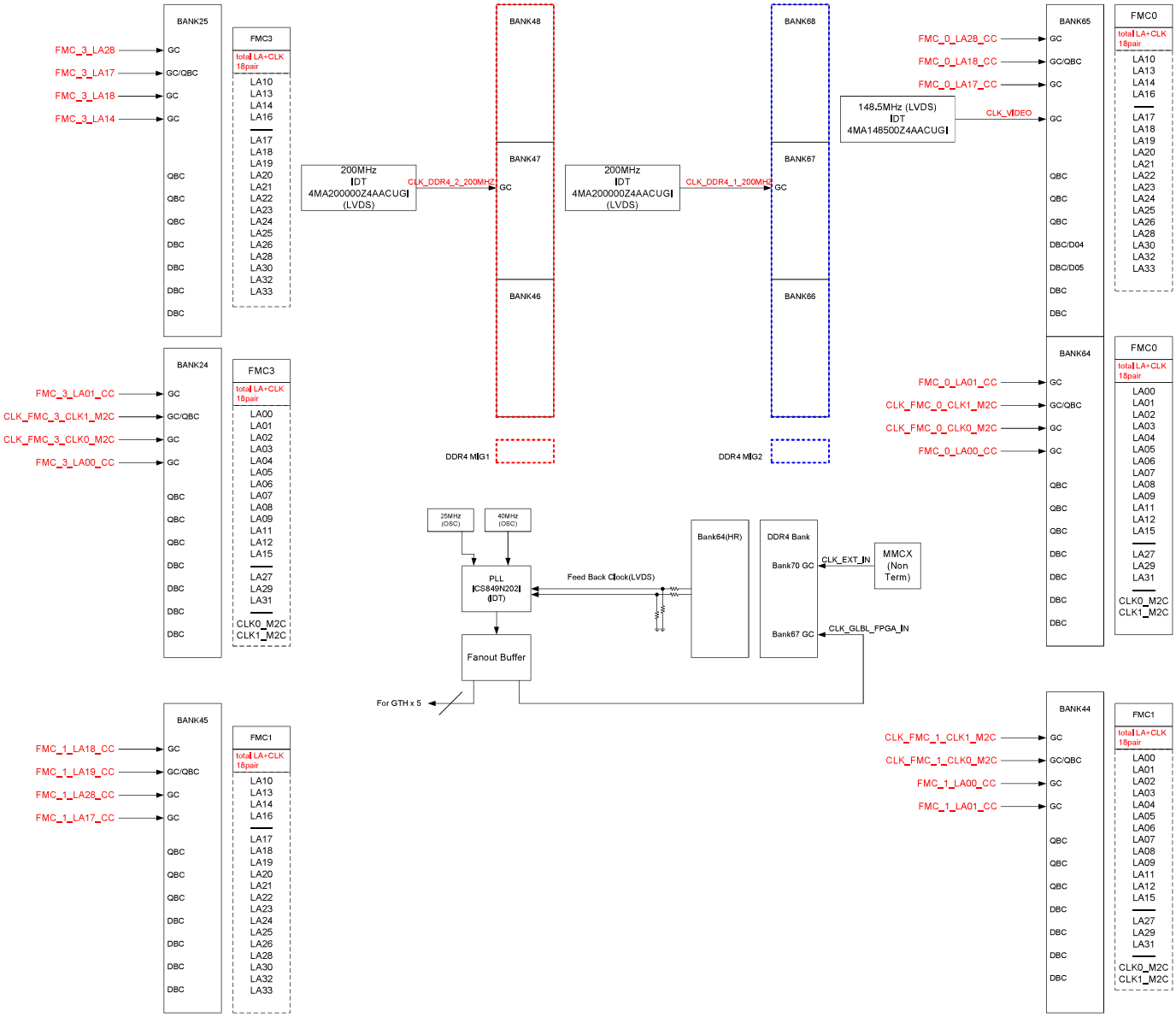


Figure 6-8 User Assigned Clocks Architecture

Note:
Clock Input

DDR clock
set_property IOSTANDARD DIFF_SSTL12_DCI [get_ports {clk_ddr4_0_clk_*}]
set_property IOSTANDARD DIFF_SSTL12_DCI [get_ports {clk_ddr4_1_clk_*}]
set_property ODT RTT_48 [get_ports {clk_ddr4_0_clk_*}]
set_property ODT RTT_48 [get_ports {clk_ddr4_1_clk_*}]

Video Clock
set_property IOSTANDARD LVDS_25 [get_ports CLK_VIDEO_clk_*]
set_property PACKAGE_PIN AN18 [get_ports CLK_VIDEO_clk_p]
set_property PACKAGE_PIN AN17 [get_ports CLK_VIDEO_clk_n]

PLL Clock
set_property IOSTANDARD DIFF_SSTL12_DCI [get_ports GLBL_FPGA_IN_CLK_*]
set_property ODT RTT_48 [get_ports {GLBL_FPGA_IN_CLK_*}]
set_property PACKAGE_PIN H19 [get_ports GLBL_FPGA_IN_CLK_P]
set_property PACKAGE_PIN G19 [get_ports GLBL_FPGA_IN_CLK_N]

PLL Reference Clock Output

CLK_EXT_REF
set_property IOSTANDARD LVDS_25 [get_ports CLK_EXT_REF_*]
set_property PACKAGE_PIN AE17 [get_ports CLK_EXT_REF_P]
set_property PACKAGE_PIN AF17 [get_ports CLK_EXT_REF_N]

6.4. FMC Connector Interface

The TB-KU-xxx-ACDC8K board has 7 high-pin count (HPC) 400 pin FMC connectors (FMC 0 to 6) on board as shown on the block diagram. These FMC connectors follow the VITA 57.1 standard with Samtec ASP-134486-01 connectors.

Presented below is the standard pin assignment on FMC HPC connectors.

Not all the pins are connected on the FMC connectors. Please follow this section for more details on all the FMC pinouts.

	K	J	H	G	F	E	D	C	B	A
1	VREF_B_M2C	GND	VREF_A_M2C	GND	PG_M2C	GND	PG_C2M	GND	CLK_DIR	GND
2	GND	CLK3_BIDIR_P	PRSNT_M2C_L	CLK1_M2C_P	GND	HA01_P_CC	GND	DP0_C2M_P	GND	DP1_M2C_P
3	GND	CLK3_BIDIR_N	GND	CLK1_M2C_N	GND	HA01_N_CC	GND	DP0_C2M_N	GND	DP1_M2C_N
4	CLK2_BIDIR_P	GND	CLK0_M2C_P	GND	HA00_P_CC	GND	GBTCLK0_M2C_P	GND	DP9_M2C_P	GND
5	CLK2_BIDIR_N	GND	CLK0_M2C_N	GND	HA00_N_CC	GND	GBTCLK0_M2C_N	GND	DP9_M2C_N	GND
6	GND	HA03_P	GND	LA00_P_CC	GND	HA05_P	GND	DP0_M2C_P	GND	DP2_M2C_P
7	HA02_P	HA03_N	LA02_P	LA00_N_CC	HA04_P	HA05_N	GND	DP0_M2C_N	GND	DP2_M2C_N
8	HA02_N	GND	LA02_N	GND	HA04_N	GND	LA01_P_CC	GND	DP8_M2C_P	GND
9	GND	HA07_P	GND	LA03_P	GND	HA09_P	LA01_N_CC	GND	DP8_M2C_N	GND
10	HA06_P	HA07_N	LA04_P	LA03_N	HA08_P	HA09_N	GND	LA06_P	GND	DP3_M2C_P
11	HA06_N	GND	LA04_N	GND	HA08_N	GND	LA05_P	LA06_N	GND	DP3_M2C_N
12	GND	HA11_P	GND	LA08_P	GND	HA13_P	LA05_N	GND	DP7_M2C_P	GND
13	HA10_P	HA11_N	LA07_P	LA08_N	HA12_P	HA13_N	GND	GND	DP7_M2C_N	GND
14	HA10_N	GND	LA07_N	GND	HA12_N	GND	LA09_P	LA10_P	GND	DP4_M2C_P
15	GND	HA14_P	GND	LA12_P	GND	HA16_P	LA09_N	LA10_N	GND	DP4_M2C_N
16	HA17_P_CC	HA14_N	LA11_P	LA12_N	HA15_P	HA16_N	GND	GND	DP6_M2C_P	GND
17	HA17_N_CC	GND	LA11_N	GND	HA15_N	GND	LA13_P	GND	DP6_M2C_N	GND
18	GND	HA18_P	GND	LA16_P	GND	HA20_P	LA13_N	LA14_P	GND	DP5_M2C_P
19	HA21_P	HA18_N	LA15_P	LA16_N	HA19_P	HA20_N	GND	LA14_N	GND	DP5_M2C_N
20	HA21_N	GND	LA15_N	GND	HA19_N	GND	LA17_P_CC	GND	GBTCLK1_M2C_P	GND
21	GND	HA22_P	GND	LA20_P	GND	HB03_P	LA17_N_CC	GND	GBTCLK1_M2C_N	GND
22	HA23_P	HA22_N	LA19_P	LA20_N	HB02_P	HB03_N	GND	LA18_P_CC	GND	DP1_C2M_P
23	HA23_N	GND	LA19_N	GND	HB02_N	GND	LA23_P	LA18_N_CC	GND	DP1_C2M_N
24	GND	HB01_P	GND	LA22_P	GND	HB05_P	LA23_N	GND	DP9_C2M_P	GND
25	HB00_P_CC	HB01_N	LA21_P	LA22_N	HB04_P	HB05_N	GND	GND	DP9_C2M_N	GND
26	HB00_N_CC	GND	LA21_N	GND	HB04_N	GND	LA26_P	LA27_P	GND	DP2_C2M_P
27	GND	HB07_P	GND	LA25_P	GND	HB09_P	LA26_N	LA27_N	GND	DP2_C2M_N
28	HB06_P_CC	HB07_N	LA24_P	LA25_N	HB08_P	HB09_N	GND	GND	DP8_C2M_P	GND
29	HB06_N_CC	GND	LA24_N	GND	HB08_N	GND	TCK	GND	DP8_C2M_N	GND
30	GND	HB11_P	GND	LA29_P	GND	HB13_P	TDI	SCL	GND	DP3_C2M_P
31	HB10_P	HB11_N	LA28_P	LA29_N	HB12_P	HB13_N	TDO	SDA	GND	DP3_C2M_N
32	HB10_N	GND	LA28_N	GND	HB12_N	GND	3P3VAUX	GND	DP7_C2M_P	GND
33	GND	HB15_P	GND	LA31_P	GND	HB19_P	TMS	GND	DP7_C2M_N	GND
34	HB14_P	HB15_N	LA30_P	LA31_N	HB16_P	HB19_N	TRST_L	GA0	GND	DP4_C2M_P
35	HB14_N	GND	LA30_N	GND	HB16_N	GND	GA1	12P0V	GND	DP4_C2M_N
36	GND	HB18_P	GND	LA33_P	GND	HB21_P	3P3V	GND	DP6_C2M_P	GND
37	HB17_P_CC	HB18_N	LA32_P	LA33_N	HB20_P	HB21_N	GND	12P0V	DP6_C2M_N	GND
38	HB17_N_CC	GND	LA32_N	GND	HB20_N	GND	3P3V	GND	GND	DP5_C2M_P
39	GND	VIO_B_M2C	GND	VADJ	GND	VADJ	GND	3P3V	GND	DP5_C2M_N
40	VIO_B_M2C	GND	VADJ	GND	VADJ	GND	3P3V	GND	RES0	GND
			LPC Connector	LPC Connector			LPC Connector	LPC Connector		

Figure 6-9 High Pin Count FMC

6.4.1. FMC HPC 0 (J1)

This FMC connects all of the available LA signals and 6 HA differential pairs to banks on the FPGA.

High Speed:

No GTH channels connected

Low Speed:

Bank 64:

- 18 differential LA pairs
- 3 differential HA pairs

Bank 65:

- 2 differential clock pairs
- 16 differential LA pairs
- 3 differential HA pair

Table 6-5 FMC 0 (J1) to FPGA Pinout

Bank#	Pin#	A		B	Pin#	Bank#
		GND	1	CLK_DIR	-	
	-	DP1_M2C_P	2	GND		
	-	DP1_M2C_N	3	GND		
		GND	4	DP9_M2C_P	-	
		GND	5	DP9_M2C_N	-	
	-	DP2_M2C_P	6	GND		
	-	DP2_M2C_N	7	GND		
		GND	8	DP8_M2C_P	-	
		GND	9	DP8_M2C_N	-	
	-	DP3_M2C_P	10	GND		
	-	DP3_M2C_N	11	GND		
		GND	12	DP7_M2C_P	-	
		GND	13	DP7_M2C_N	-	
	-	DP4_M2C_P	14	GND		
	-	DP4_M2C_N	15	GND		
		GND	16	DP6_M2C_P	-	
		GND	17	DP6_M2C_N	-	
	-	DP5_M2C_P	18	GND		
	-	DP5_M2C_N	19	GND		
		GND	20	*1 GBTCLK1_M2C_P	-	
		GND	21	*1 GBTCLK1_M2C_N	-	
	-	DP1_C2M_P	22	GND		
	-	DP1_C2M_N	23	GND		
		GND	24	DP9_C2M_P	-	
		GND	25	DP9_C2M_N	-	
	-	DP2_C2M_P	26	GND		
	-	DP2_C2M_N	27	GND		
		GND	28	DP8_C2M_P	-	
		GND	29	DP8_C2M_N	-	
	-	DP3_C2M_P	30	GND		
	-	DP3_C2M_N	31	GND		
		GND	32	DP7_C2M_P	-	
		GND	33	DP7_C2M_N	-	
	-	DP4_C2M_P	34	GND		
	-	DP4_C2M_N	35	GND		
		GND	36	DP6_C2M_P	-	
		GND	37	DP6_C2M_N	-	
	-	DP5_C2M_P	38	GND		
	-	DP5_C2M_N	39	GND		
		GND	40	RES0	-	

FMC 0 (J1)

Bank#	Pin#	C		D	Pin#	Bank#
		GND	1	*5 PG_C2M	-	
	-	DP0_C2M_P	2	GND		
	-	DP0_C2M_N	3	GND		
		GND	4	*1 GBTCLK0_M2C_P	-	
		GND	5	*1 GBTCLK0_M2C_N	-	
	-	DP0_M2C_P	6	GND		
	-	DP0_M2C_N	7	GND		
		GND	8	LA01_P_CC	AL14	65
		GND	9	LA01_N_CC	AL13	65
65	AU12	LA06_P	10	GND		
65	AV12	LA06_N	11	LA05_P	AV13	65
		GND	12	LA05_N	AW13	65
		GND	13	GND		
64	AJ16	LA10_P	14	LA09_P	AK13	65
64	AK16	LA10_N	15	LA09_N	AK12	65
		GND	16	GND		
		GND	17	LA13_P	AK18	64
64	AP19	LA14_P	18	LA13_N	AK17	64
64	AP18	LA14_N	19	GND		
		GND	20	LA17_P_CC	AM19	64
		GND	21	LA17_N_CC	AN19	64
64	AL17	LA18_P_CC	22	GND		
64	AM17	LA18_N_CC	23	LA23_P	AR18	64
		GND	24	LA23_N	AR17	64
		GND	25	GND		
65	AT15	LA27_P	26	LA26_P	AP16	64
65	AU15	LA27_N	27	LA26_N	AR16	64
		GND	28	GND		
		GND	29	TCK	-	
	-	*2 SCL	30	*4 TDI	-	
	-	*2 SDA	31	*4 TDO	-	
		GND	32	*6 3P3VAUX	-	
		GND	33	TMS	-	
	-	*3 GA0	34	TRST_L	-	
	-	*6 12P0V	35	*3 GA1	-	
		GND	36	*6 3P3V	-	
	-	*6 12P0V	37	GND		
		GND	38	*6 3P3V	-	
	-	*6 3P3V	39	GND		
		GND	40	*6 3P3V	-	

FMC 0 (J1)

Bank#	Pin#	E		F	Pin#	Bank#
		GND	1	*5 PG_M2C	-	
65	AD14	HA01_P_CC	2	GND		
65	AD13	HA01_N_CC	3	GND		
		GND	4	HA00_P_CC	AE12	65
		GND	5	HA00_N_CC	AF12	65
64	AE18	HA05_P	6	GND		
64	AF18	HA05_N	7	HA04_P	AP15	65
		GND	8	HA04_N	AR15	65
	-	HA09_P	9	GND		
	-	HA09_N	10	HA08_P	-	
		GND	11	HA08_N	-	
	-	HA13_P	12	GND		
	-	HA13_N	13	HA12_P	-	
		GND	14	HA12_N	-	
	-	HA16_P	15	GND		
	-	HA16_N	16	HA15_P	-	
		GND	17	HA15_N	-	
	-	HA20_P	18	GND		
	-	HA20_N	19	HA19_P	-	
		GND	20	HA19_N	-	
	-	HB03_P	21	GND		
	-	HB03_N	22	HB02_P	-	
		GND	23	HB02_N	-	
	-	HB05_P	24	GND		
	-	HB05_N	25	HB04_P	-	
		GND	26	HB04_N	-	
	-	HB09_P	27	GND		
	-	HB09_N	28	HB08_P	-	
		GND	29	HB08_N	-	
	-	HB13_P	30	GND		
	-	HB13_N	31	HB12_P	-	
		GND	32	HB12_N	-	
	-	HB19_P	33	GND		
	-	HB19_N	34	HB16_P	-	
		GND	35	HB16_N	-	
	-	HB21_P	36	GND		
	-	HB21_N	37	HB20_P	-	
		GND	38	HB20_N	-	
	-	*6 VADJ	39	GND		
		GND	40	*6 VADJ	-	

FMC 0 (J1)

Bank#	Pin#	G		H	Pin#	Bank#
		GND	1	*7 VREF_A_M2C	-	
65	AL12	CLK1_M2C_P	2	*5 PRSNT_M2C_L	-	
65	AM12	CLK1_M2C_N	3	GND		
		GND	4	CLK0_M2C_P	AM14	65
		GND	5	CLK0_M2C_N	AN14	65
65	AN13	LA00_P_CC	6	GND		
65	AN12	LA00_N_CC	7	LA02_P	AR12	65
		GND	8	LA02_N	AT12	65
65	AR13	LA03_P	9	GND		
65	AT13	LA03_N	10	LA04_P	AT14	65
		GND	11	LA04_N	AU14	65
65	AV14	LA08_P	12	GND		
65	AW14	LA08_N	13	LA07_P	AH13	65
		GND	14	LA07_N	AJ13	65
65	AH14	LA12_P	15	GND		
65	AJ14	LA12_N	16	LA11_P	AP14	65
		GND	17	LA11_N	AP13	65
64	AH19	LA16_P	18	GND		
64	AH18	LA16_N	19	LA15_P	AJ15	65
		GND	20	LA15_N	AK15	65
64	AU17	LA20_P	21	GND		
64	AU16	LA20_N	22	LA19_P	AT19	64
		GND	23	LA19_N	AU19	64
64	AJ19	LA22_P	24	GND		
64	AJ18	LA22_N	25	LA21_P	AH17	64
		GND	26	LA21_N	AH16	64
64	AT18	LA25_P	27	GND		
64	AT17	LA25_N	28	LA24_P	AV18	64
		GND	29	LA24_N	AV17	64
65	AG12	LA29_P	30	GND		
65	AH12	LA29_N	31	LA28_P	AL19	64
		GND	32	LA28_N	AL18	64
65	AF15	LA31_P	33	GND		
65	AG15	LA31_N	34	LA30_P	AV19	64
		GND	35	LA30_N	AW18	64
64	AR20	LA33_P	36	GND		
64	AT20	LA33_N	37	LA32_P	AW20	64
		GND	38	LA32_N	AW19	64
	-	*6 VADJ	39	GND		
		GND	40	*6 VADJ	-	

FMC 0 (J1)

Bank#	Pin#	J		K	Pin#	Bank#
		GND	1	*7 VREF_B_M2C	-	
	-	CLK3_M2C_P	2	GND		
	-	CLK3_M2C_N	3	GND		
		GND	4	CLK2_M2C_P	-	
		GND	5	CLK2_M2C_N	-	
64	AD16	HA03_P	6	GND		
64	AE16	HA03_N	7	HA02_P	AG17	64
		GND	8	HA02_N	AG16	64
	-	HA07_P	9	GND		
	-	HA07_N	10	HA06_P	-	
		GND	11	HA06_N	-	
	-	HA11_P	12	GND		
	-	HA11_N	13	HA10_P	-	
		GND	14	HA10_N	-	
	-	HA14_P	15	GND		
	-	HA14_N	16	HA17_P_CC	-	
		GND	17	HA17_N_CC	-	
	-	HA18_P	18	GND		
	-	HA18_N	19	HA21_P	-	
		GND	20	HA21_N	-	
	-	HA22_P	21	GND		
	-	HA22_N	22	HA23_P	-	
		GND	23	HA23_N	-	
	-	HB01_P	24	GND		
	-	HB01_N	25	HB00_P_CC	-	
		GND	26	HB00_N_CC	-	
	-	HB07_P	27	GND		
	-	HB07_N	28	HB06_P_CC	-	
		GND	29	HB06_N_CC	-	
	-	HB11_P	30	GND		
	-	HB11_N	31	HB10_P	-	
		GND	32	HB10_N	-	
	-	HB15_P	33	GND		
	-	HB15_N	34	HB14_P	-	
		GND	35	HB14_N	-	
	-	HB18_P	36	GND		
	-	HB18_N	37	HB17_P_CC	-	
		GND	38	HB17_N_CC	-	
	-	*8 VIO_B_M2C	39	GND		
		GND	40	*8 VIO_B_M2C	-	

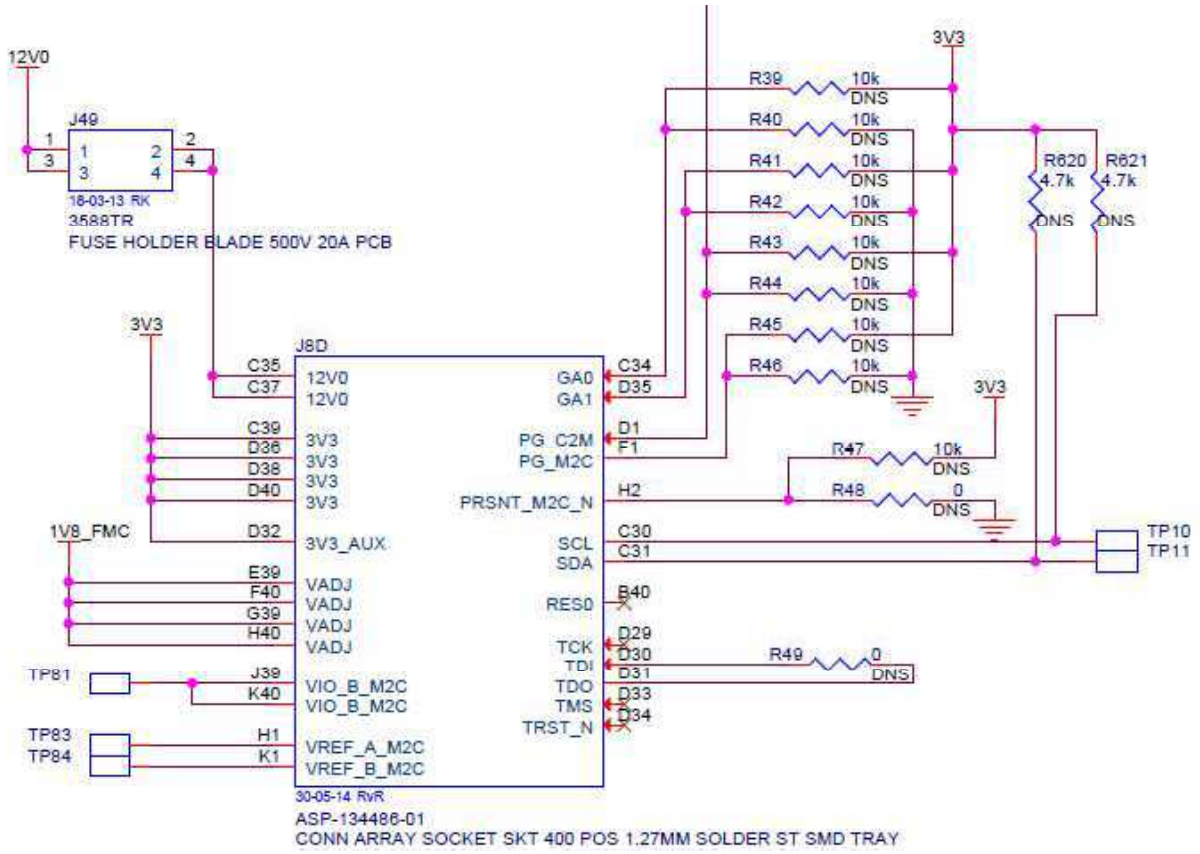


Figure 6-10 FMC 0 to 6 SCL/SDA, GA0/GA1, TDI/TDO

Note: The above structure is identical for all FMC connectors on this board, with the exception of test points and reference designators being different per FMC.

For FMC 0 (J1):

*1: There are no GTH channels on this connector so the GBTCLK1_M2C_P/N signals are not connected.

*2: SCL, SDA

The board provides test points with pull-up options to enable I2C communication with the FPGA. By default, the pull-ups are not populated.

*3: GA0, GA1

This board provides pull-up or pull-down options for these connections, by default they are floating.

*4: TDI, TDO

The JTAG TDO pin is connected with a loopback to TDI through a 0 ohm resistor that is not populated by default.

*5: PG_C2M, PG_M2C, PRSNT_M2C_N

Referring to the figure above, they all have a resistor option for either pull-up or pull-down. However, the resistors are not populated by default, these pins are floating.

*6: Power Rails

This card provides a 12V output through the 12V0 pins and 3.3V output through the 3V3 and 3V3_AUX pins. It is important to note that all the FMC connectors present on this board are equipped with a fuse on the 12V0 rail. Lastly, the VADJ pins provide a 1.8V/2.5V/3.3V rail to FPGA mezzanine cards.

*7: VREF_A_M2C, VREF_B_M2C

These terminals can be monitored by test points **TP83** and **TP84**.

*8: VIO_B_M2C

Both pins J39 and K40 for this terminal can also be monitored by test point **TP81**.

6.4.2. FMC HPC 1 (J2)

This FMC connects GTH lanes and all of the available LA signals to banks on the FPGA.

High Speed:

Quad 224 and 225:

- 8 GTH lanes
- 2 differential clock pairs

Low Speed:

Bank 44:

- 16 differential LA pairs
- 2 differential clock pairs

Bank 45:

- 18 differential LA pairs

Table 6-6 FMC 1 (J2) to FPGA Pinout

Bank#	Pin#	A		B	Pin#	Bank#
		GND	1	CLK_DIR	-	
225	AN4	DP1_M2C_P	2	GND		
225	AN3	DP1_M2C_N	3	GND		
		GND	4	DP9_M2C_P	-	
		GND	5	DP9_M2C_N	-	
225	AP2	DP2_M2C_P	6	GND		
225	AP1	DP2_M2C_N	7	GND		
		GND	8	DP8_M2C_P	-	
		GND	9	DP8_M2C_N	-	
225	AR4	DP3_M2C_P	10	GND		
225	AR3	DP3_M2C_N	11	GND		
		GND	12	DP7_M2C_P	AT2	224
		GND	13	DP7_M2C_N	AT1	224
224	AU4	DP4_M2C_P	14	GND		
224	AU3	DP4_M2C_N	15	GND		
		GND	16	DP6_M2C_P	AV2	224
		GND	17	DP6_M2C_N	AV1	224
224	AW4	DP5_M2C_P	18	GND		
224	AW3	DP5_M2C_N	19	GND		
		GND	20	*1 GBTCLK1_M2C_P	AP10	224
		GND	21	*1 GBTCLK1_M2C_N	AP9	224
225	AN8	DP1_C2M_P	22	GND		
225	AN7	DP1_C2M_N	23	GND		
		GND	24	DP9_C2M_P	-	
		GND	25	DP9_C2M_N	-	
225	AP6	DP2_C2M_P	26	GND		
225	AP5	DP2_C2M_N	27	GND		
		GND	28	DP8_C2M_P	-	
		GND	29	DP8_C2M_N	-	
225	AR8	DP3_C2M_P	30	GND		
225	AR7	DP3_C2M_N	31	GND		
		GND	32	DP7_C2M_P	AT6	224
		GND	33	DP7_C2M_N	AT5	224
224	AU8	DP4_C2M_P	34	GND		
224	AU7	DP4_C2M_N	35	GND		
		GND	36	DP6_C2M_P	AV6	224
		GND	37	DP6_C2M_N	AV5	224
224	AW8	DP5_C2M_P	38	GND		
224	AW7	DP5_C2M_N	39	GND		
		GND	40	RES0	-	

FMC 1 (J2)

Bank#	Pin#	C		D	Pin#	Bank#
		GND	1	*5 PG_C2M	-	
225	AM6	DP0_C2M_P	2	GND		
225	AM5	DP0_C2M_N	3	GND		
		GND	4	*1 GBTCLK0_M2C_P	AT10	224
		GND	5	*1 GBTCLK0_M2C_N	AT9	224
225	AM2	DP0_M2C_P	6	GND		
225	AM1	DP0_M2C_N	7	GND		
		GND	8	LA01_P_CC	AM22	44
		GND	9	LA01_N_CC	AN22	44
44	AR22	LA06_P	10	GND		
44	AR23	LA06_N	11	LA05_P	AT22	44
		GND	12	LA05_N	AU22	44
		GND	13	GND		
45	AW25	LA10_P	14	LA09_P	AV23	44
45	AW26	LA10_N	15	LA09_N	AW23	44
		GND	16	GND		
		GND	17	LA13_P	AH24	45
45	AJ25	LA14_P	18	LA13_N	AJ24	45
45	AK25	LA14_N	19	GND		
		GND	20	LA17_P_CC	AM27	45
		GND	21	LA17_N_CC	AN27	45
45	AL27	LA18_P_CC	22	GND		
45	AL28	LA18_N_CC	23	LA23_P	AT27	45
		GND	24	LA23_N	AU27	45
		GND	25	GND		
44	AK20	LA27_P	26	LA26_P	AM24	45
44	AK21	LA27_N	27	LA26_N	AM25	45
		GND	28	GND		
		GND	29	TCK	-	
	-	*2 SCL	30	*4 TDI	-	
	-	*2 SDA	31	*4 TDO	-	
		GND	32	*6 3P3VAUX	-	
		GND	33	TMS	-	
	-	*3 GA0	34	TRST_L	-	
	-	*6 12P0V	35	*3 GA1	-	
		GND	36	*6 3P3V	-	
	-	*6 12P0V	37	GND		
		GND	38	*6 3P3V	-	
	-	*6 3P3V	39	GND		
		GND	40	*6 3P3V	-	

FMC 1 (J2)

Bank#	Pin#	E		F	Pin#	Bank#
		GND	1	*5 PG_M2C	-	
	-	HA01_P_CC	2	GND		
	-	HA01_N_CC	3	GND		
		GND	4	HA00_P_CC	-	
		GND	5	HA00_N_CC	-	
	-	HA05_P	6	GND		
	-	HA05_N	7	HA04_P	-	
		GND	8	HA04_N	-	
	-	HA09_P	9	GND		
	-	HA09_N	10	HA08_P	-	
		GND	11	HA08_N	-	
	-	HA13_P	12	GND		
	-	HA13_N	13	HA12_P	-	
		GND	14	HA12_N	-	
	-	HA16_P	15	GND		
	-	HA16_N	16	HA15_P	-	
		GND	17	HA15_N	-	
	-	HA20_P	18	GND		
	-	HA20_N	19	HA19_P	-	
		GND	20	HA19_N	-	
	-	HB03_P	21	GND		
	-	HB03_N	22	HB02_P	-	
		GND	23	HB02_N	-	
	-	HB05_P	24	GND		
	-	HB05_N	25	HB04_P	-	
		GND	26	HB04_N	-	
	-	HB09_P	27	GND		
	-	HB09_N	28	HB08_P	-	
		GND	29	HB08_N	-	
	-	HB13_P	30	GND		
	-	HB13_N	31	HB12_P	-	
		GND	32	HB12_N	-	
	-	HB19_P	33	GND		
	-	HB19_N	34	HB16_P	-	
		GND	35	HB16_N	-	
	-	HB21_P	36	GND		
	-	HB21_N	37	HB20_P	-	
		GND	38	HB20_N	-	
	-	*6 VADJ	39	GND		
		GND	40	*6 VADJ	-	

FMC 1 (J2)

Bank#	Pin#	G		H	Pin#	Bank#
		GND	1	*7 VREF_A_M2C	-	
44	AK22	CLK1_M2C_P	2	*5 PRSNT_M2C_L	-	
44	AL22	CLK1_M2C_N	3	GND		
		GND	4	CLK0_M2C_P	AK23	44
		GND	5	CLK0_M2C_N	AL23	44
44	AM21	LA00_P_CC	6	GND		
44	AN21	LA00_N_CC	7	LA02_P	AJ20	44
		GND	8	LA02_N	AJ21	44
44	AP21	LA03_P	9	GND		
44	AR21	LA03_N	10	LA04_P	AH22	44
		GND	11	LA04_N	AH23	44
44	AV21	LA08_P	12	GND		
44	AW21	LA08_N	13	LA07_P	AU21	44
		GND	14	LA07_N	AV22	44
44	AV24	LA12_P	15	GND		
44	AW24	LA12_N	16	LA11_P	AT23	44
		GND	17	LA11_N	AT24	44
45	AV26	LA16_P	18	GND		
45	AV27	LA16_N	19	LA15_P	AL20	44
		GND	20	LA15_N	AM20	44
45	AH26	LA20_P	21	GND		
45	AJ26	LA20_N	22	LA19_P	AK27	45
		GND	23	LA19_N	AK28	45
45	AR28	LA22_P	24	GND		
45	AT28	LA22_N	25	LA21_P	AL24	45
		GND	26	LA21_N	AL25	45
45	AN28	LA25_P	27	GND		
45	AP28	LA25_N	28	LA24_P	AV28	45
		GND	29	LA24_N	AW28	45
44	AN23	LA29_P	30	GND		
44	AP23	LA29_N	31	LA28_P	AM26	45
		GND	32	LA28_N	AN26	45
44	AN24	LA31_P	33	GND		
44	AP24	LA31_N	34	LA30_P	AP25	45
		GND	35	LA30_N	AR25	45
45	AU25	LA33_P	36	GND		
45	AU26	LA33_N	37	LA32_P	AR26	45
		GND	38	LA32_N	AR27	45
	-	*6 VADJ	39	GND		
		GND	40	*6 VADJ	-	

FMC 1 (J2)

Bank#	Pin#	J		K	Pin#	Bank#
		GND	1	*7 VREF_B_M2C	-	
	-	CLK3_M2C_P	2	GND		
	-	CLK3_M2C_N	3	GND		
		GND	4	CLK2_M2C_P	-	
		GND	5	CLK2_M2C_N	-	
	-	HA03_P	6	GND		
	-	HA03_N	7	HA02_P	-	
		GND	8	HA02_N	-	
	-	HA07_P	9	GND		
	-	HA07_N	10	HA06_P	-	
		GND	11	HA06_N	-	
	-	HA11_P	12	GND		
	-	HA11_N	13	HA10_P	-	
		GND	14	HA10_N	-	
	-	HA14_P	15	GND		
	-	HA14_N	16	HA17_P_CC	-	
		GND	17	HA17_N_CC	-	
	-	HA18_P	18	GND		
	-	HA18_N	19	HA21_P	-	
		GND	20	HA21_N	-	
	-	HA22_P	21	GND		
	-	HA22_N	22	HA23_P	-	
		GND	23	HA23_N	-	
	-	HB01_P	24	GND		
	-	HB01_N	25	HB00_P_CC	-	
		GND	26	HB00_N_CC	-	
	-	HB07_P	27	GND		
	-	HB07_N	28	HB06_P_CC	-	
		GND	29	HB06_N_CC	-	
	-	HB11_P	30	GND		
	-	HB11_N	31	HB10_P	-	
		GND	32	HB10_N	-	
	-	HB15_P	33	GND		
	-	HB15_N	34	HB14_P	-	
		GND	35	HB14_N	-	
	-	HB18_P	36	GND		
	-	HB18_N	37	HB17_P_CC	-	
		GND	38	HB17_N_CC	-	
	-	*8 VIO_B_M2C	39	GND		
		GND	40	*8 VIO_B_M2C	-	

For FMC 1 (J2):

*1: GBTCLK[0:1]_M2C_P/N

These clocks are connected to Quad 224 of the FPGA while this board provides an MMCX interface for one pair of clocks on Quad 225. The other pair is provided by the system clock buffer.

*2: SCL, SDA

The board provides test points with pull-up options to enable I2C communication with the FPGA. By default, the pull-ups are not populated.

*3: GA0, GA1

This board provides pull-up or pull-down options for these connections, by default they are floating.

*4: TDI, TDO

The JTAG TDO pin is connected with a loopback to TDI through a 0 ohm resistor that is not populated by default.

*5: PG_C2M, PG_M2C, PRSNT_M2C_N

These all have a pull-up or pull-down resistor option. However, the resistors are not populated by default, these pins are floating.

*6: Power Rails

This card provides a 12V output through the 12V0 pins and 3.3V output through the 3V3 and 3V3_AUX pins. It is important to note that all the FMC connectors present on this board are equipped with a fuse on the 12V0 rail. Lastly, the VADJ pins provide a 1.8V rail to FPGA mezzanine cards.

*7: VREF_A_M2C, VREF_B_M2C

These terminals can be monitored by test points **TP75** and **TP76**.

*8: VIO_B_M2C

Both pins J39 and K40 for this terminal can also be monitored by test point **TP73**.

6.4.3. FMC HPC 2 (J5)

This FMC connects GTH lanes and 6 differential pairs of LA signals to banks on the FPGA.

High Speed:

Quad 226 and 227:

- 8 GTH lanes
- 2 differential clock pairs

Low Speed:

Bank 25:

- 6 differential LA pairs

Table 6-7 FMC 2 (J5) to FPGA Pinout

Bank#	Pin#	A		B	Pin#	Bank#
		GND	1	CLK_DIR	-	
227	AD2	DP1_M2C_P	2	GND		
227	AD1	DP1_M2C_N	3	GND		
		GND	4	DP9_M2C_P	-	
		GND	5	DP9_M2C_N	-	
227	AF2	DP2_M2C_P	6	GND		
227	AF1	DP2_M2C_N	7	GND		
		GND	8	DP8_M2C_P	-	
		GND	9	DP8_M2C_N	-	
227	AG4	DP3_M2C_P	10	GND		
227	AG3	DP3_M2C_N	11	GND		
		GND	12	DP7_M2C_P	AH2	226
		GND	13	DP7_M2C_N	AH1	226
226	AJ4	DP4_M2C_P	14	GND		
226	AJ3	DP4_M2C_N	15	GND		
		GND	16	DP6_M2C_P	AK2	226
		GND	17	DP6_M2C_N	AK1	226
226	AL4	DP5_M2C_P	18	GND		
226	AL3	DP5_M2C_N	19	GND		
		GND	20	*1 GBTCLK1_M2C_P	AF10	226
		GND	21	*1 GBTCLK1_M2C_N	AF9	226
227	AE4	DP1_C2M_P	22	GND		
227	AE3	DP1_C2M_N	23	GND		
		GND	24	DP9_C2M_P	-	
		GND	25	DP9_C2M_N	-	
227	AF6	DP2_C2M_P	26	GND		
227	AF5	DP2_C2M_N	27	GND		
		GND	28	DP8_C2M_P	-	
		GND	29	DP8_C2M_N	-	
227	AG8	DP3_C2M_P	30	GND		
227	AG7	DP3_C2M_N	31	GND		
		GND	32	DP7_C2M_P	AH6	226
		GND	33	DP7_C2M_N	AH5	226
226	AJ8	DP4_C2M_P	34	GND		
226	AJ7	DP4_C2M_N	35	GND		
		GND	36	DP6_C2M_P	AK6	226
		GND	37	DP6_C2M_N	AK5	226
226	AL8	DP5_C2M_P	38	GND		
226	AL7	DP5_C2M_N	39	GND		
		GND	40	RES0	-	

FMC 2 (J5)

Bank#	Pin#	C		D	Pin#	Bank#
		GND	1	*5 PG_C2M	-	
227	AD6	DP0_C2M_P	2	GND		
227	AD5	DP0_C2M_N	3	GND		
		GND	4	*1 GBTCLK0_M2C_P	AH10	226
		GND	5	*1 GBTCLK0_M2C_N	AH9	226
227	AC4	DP0_M2C_P	6	GND		
227	AC3	DP0_M2C_N	7	GND		
		GND	8	LA01_P_CC	-	
		GND	9	LA01_N_CC	-	
	-	LA06_P	10	GND		
	-	LA06_N	11	LA05_P	-	
		GND	12	LA05_N	-	
		GND	13	GND		
	-	LA10_P	14	LA09_P	-	
	-	LA10_N	15	LA09_N	-	
		GND	16	GND		
		GND	17	LA13_P	-	
	-	LA14_P	18	LA13_N	-	
	-	LA14_N	19	GND		
		GND	20	LA17_P_CC	-	
		GND	21	LA17_N_CC	-	
	-	LA18_P_CC	22	GND		
	-	LA18_N_CC	23	LA23_P	-	
		GND	24	LA23_N	-	
		GND	25	GND		
	-	LA27_P	26	LA26_P	-	
	-	LA27_N	27	LA26_N	-	
		GND	28	GND		
		GND	29	TCK	-	
	-	*2 SCL	30	*4 TDI	-	
	-	*2 SDA	31	*4 TDO	-	
		GND	32	*6 3P3VAUX	-	
		GND	33	TMS	-	
	-	*3 GA0	34	TRST_L	-	
	-	*6 12P0V	35	*3 GA1	-	
		GND	36	*6 3P3V	-	
	-	*6 12P0V	37	GND		
		GND	38	*6 3P3V	-	
	-	*6 3P3V	39	GND		
		GND	40	*6 3P3V	-	

FMC 2 (J5)

Bank#	Pin#	E		F	Pin#	Bank#
		GND	1	*5 PG_M2C	-	
	-	HA01_P_CC	2	GND		
	-	HA01_N_CC	3	GND		
		GND	4	HA00_P_CC	-	
		GND	5	HA00_N_CC	-	
	-	HA05_P	6	GND		
	-	HA05_N	7	HA04_P	-	
		GND	8	HA04_N	-	
	-	HA09_P	9	GND		
	-	HA09_N	10	HA08_P	-	
		GND	11	HA08_N	-	
	-	HA13_P	12	GND		
	-	HA13_N	13	HA12_P	-	
		GND	14	HA12_N	-	
	-	HA16_P	15	GND		
	-	HA16_N	16	HA15_P	-	
		GND	17	HA15_N	-	
	-	HA20_P	18	GND		
	-	HA20_N	19	HA19_P	-	
		GND	20	HA19_N	-	
	-	HB03_P	21	GND		
	-	HB03_N	22	HB02_P	-	
		GND	23	HB02_N	-	
	-	HB05_P	24	GND		
	-	HB05_N	25	HB04_P	-	
		GND	26	HB04_N	-	
	-	HB09_P	27	GND		
	-	HB09_N	28	HB08_P	-	
		GND	29	HB08_N	-	
	-	HB13_P	30	GND		
	-	HB13_N	31	HB12_P	-	
		GND	32	HB12_N	-	
	-	HB19_P	33	GND		
	-	HB19_N	34	HB16_P	-	
		GND	35	HB16_N	-	
	-	HB21_P	36	GND		
	-	HB21_N	37	HB20_P	-	
		GND	38	HB20_N	-	
	-	*6 VADJ	39	GND		
		GND	40	*6 VADJ	-	

FMC 2 (J5)

Bank#	Pin#	G		H	Pin#	Bank#
		GND	1	*7 VREF_A_M2C	-	
	-	CLK1_M2C_P	2	*5 PRSNT_M2C_L	-	
	-	CLK1_M2C_N	3	GND		
		GND	4	CLK0_M2C_P	-	
		GND	5	CLK0_M2C_N	-	
25	AW33	LA00_P_CC	6	GND		
25	AW34	LA00_N_CC	7	LA02_P	-	
		GND	8	LA02_N	-	
25	AR33	LA03_P	9	GND		
25	AT33	LA03_N	10	LA04_P	-	
		GND	11	LA04_N	-	
25	AT34	LA08_P	12	GND		
25	AU34	LA08_N	13	LA07_P	-	
		GND	14	LA07_N	-	
25	AV33	LA12_P	15	GND		
25	AV34	LA12_N	16	LA11_P	-	
		GND	17	LA11_N	-	
25	AT35	LA16_P	18	GND		
25	AU35	LA16_N	19	LA15_P	-	
		GND	20	LA15_N	-	
	-	LA20_P	21	GND		
	-	LA20_N	22	LA19_P	-	
		GND	23	LA19_N	-	
25	AW35	LA22_P	24	GND		
25	AW36	LA22_N	25	LA21_P	-	
		GND	26	LA21_N	-	
	-	LA25_P	27	GND		
	-	LA25_N	28	LA24_P	-	
		GND	29	LA24_N	-	
	-	LA29_P	30	GND		
	-	LA29_N	31	LA28_P	-	
		GND	32	LA28_N	-	
	-	LA31_P	33	GND		
	-	LA31_N	34	LA30_P	-	
		GND	35	LA30_N	-	
	-	LA33_P	36	GND		
	-	LA33_N	37	LA32_P	-	
		GND	38	LA32_N	-	
	-	*6 VADJ	39	GND		
		GND	40	*6 VADJ	-	

FMC 2 (J5)

Bank#	Pin#	J		K	Pin#	Bank#
		GND	1	*7 VREF_B_M2C	-	
	-	CLK3_M2C_P	2	GND		
	-	CLK3_M2C_N	3	GND		
		GND	4	CLK2_M2C_P	-	
		GND	5	CLK2_M2C_N	-	
	-	HA03_P	6	GND		
	-	HA03_N	7	HA02_P	-	
		GND	8	HA02_N	-	
	-	HA07_P	9	GND		
	-	HA07_N	10	HA06_P	-	
		GND	11	HA06_N	-	
	-	HA11_P	12	GND		
	-	HA11_N	13	HA10_P	-	
		GND	14	HA10_N	-	
	-	HA14_P	15	GND		
	-	HA14_N	16	HA17_P_CC	-	
		GND	17	HA17_N_CC	-	
	-	HA18_P	18	GND		
	-	HA18_N	19	HA21_P	-	
		GND	20	HA21_N	-	
	-	HA22_P	21	GND		
	-	HA22_N	22	HA23_P	-	
		GND	23	HA23_N	-	
	-	HB01_P	24	GND		
	-	HB01_N	25	HB00_P_CC	-	
		GND	26	HB00_N_CC	-	
	-	HB07_P	27	GND		
	-	HB07_N	28	HB06_P_CC	-	
		GND	29	HB06_N_CC	-	
	-	HB11_P	30	GND		
	-	HB11_N	31	HB10_P	-	
		GND	32	HB10_N	-	
	-	HB15_P	33	GND		
	-	HB15_N	34	HB14_P	-	
		GND	35	HB14_N	-	
	-	HB18_P	36	GND		
	-	HB18_N	37	HB17_P_CC	-	
		GND	38	HB17_N_CC	-	
	-	*8 VIO_B_M2C	39	GND		
		GND	40	*8 VIO_B_M2C	-	

For FMC 2 (J5):

*1: GBTCLK[0:1]_M2C_P/N

These clocks are connected to Quad 226 of the FPGA while this board provides an MMCX interface for one pair of clocks on Quad 227. The other pair is provided by the system clock buffer.

*2: SCL, SDA

The board provides test points with pull-up options to enable I2C communication with the FPGA. By default, the pull-ups are not populated.

*3: GA0, GA1

This board provides pull-up or pull-down options for these connections, by default they are floating.

*4: TDI, TDO

The JTAG TDO pin is connected with a loopback to TDI through a 0 ohm resistor that is not populated by default.

*5: PG_C2M, PG_M2C, PRSNT_M2C_N

These all have a pull-up or pull-down resistor option. However, the resistors are not populated by default, these pins are floating.

*6: Power Rails

This card provides a 12V output through the 12V0 pins and 3.3V output through the 3V3 and 3V3_AUX pins. It is important to note that all the FMC connectors present on this board are equipped with a fuse on the 12V0 rail. Lastly, the VADJ pins provide a 1.8V rail to FPGA mezzanine cards.

*7: VREF_A_M2C, VREF_B_M2C

These terminals can be monitored by test points **TP79** and **TP80**.

*8: VIO_B_M2C

Both pins J39 and K40 for this terminal can also be monitored by test point **TP77**.

6.4.4. FMC HPC 3 (J8)

This FMC connects GTH lanes and all of the available LA signals to banks on the FPGA.

High Speed:

Quad 126 and 127:

- 8 GTH lanes
- 2 differential clock pairs

Low Speed:

Bank 24:

- 16 differential LA pairs
- 2 differential clock pairs

Bank 25:

- 18 differential LA pairs

Table 6-8 FMC 3 (J8) to FPGA Pinout

Bank#	Pin#	A		B	Pin#	Bank#
		GND	1	CLK_DIR	-	
126	AF36	DP1_M2C_P	2	GND		
126	AF37	DP1_M2C_N	3	GND		
		GND	4	DP9_M2C_P	-	
		GND	5	DP9_M2C_N	-	
126	AE38	DP2_M2C_P	6	GND		
126	AE39	DP2_M2C_N	7	GND		
		GND	8	DP8_M2C_P	-	
		GND	9	DP8_M2C_N	-	
126	AC38	DP3_M2C_P	10	GND		
126	AC39	DP3_M2C_N	11	GND		
		GND	12	DP7_M2C_P	AB36	127
		GND	13	DP7_M2C_N	AB37	127
127	AA38	DP4_M2C_P	14	GND		
127	AA39	DP4_M2C_N	15	GND		
		GND	16	DP6_M2C_P	W38	127
		GND	17	DP6_M2C_N	W39	127
127	V36	DP5_M2C_P	18	GND		
127	V37	DP5_M2C_N	19	GND		
		GND	20	*1 GBTCLK1_M2C_P	AB32	126
		GND	21	*1 GBTCLK1_M2C_N	AB33	126
126	AG34	DP1_C2M_P	22	GND		
126	AG35	DP1_C2M_N	23	GND		
		GND	24	DP9_C2M_P	-	
		GND	25	DP9_C2M_N	-	
126	AE34	DP2_C2M_P	26	GND		
126	AE35	DP2_C2M_N	27	GND		
		GND	28	DP8_C2M_P	-	
		GND	29	DP8_C2M_N	-	
126	AD36	DP3_C2M_P	30	GND		
126	AD37	DP3_C2M_N	31	GND		
		GND	32	DP7_C2M_P	AC34	127
		GND	33	DP7_C2M_N	AC35	127
127	AA34	DP4_C2M_P	34	GND		
127	AA35	DP4_C2M_N	35	GND		
		GND	36	DP6_C2M_P	Y36	127
		GND	37	DP6_C2M_N	Y37	127
127	W34	DP5_C2M_P	38	GND		
127	W35	DP5_C2M_N	39	GND		
		GND	40	RES0	-	

FMC 3 (J8)

Bank#	Pin#	C		D	Pin#	Bank#
		GND	1	*5 PG_C2M	-	
126	AH36	DP0_C2M_P	2	GND		
126	AH37	DP0_C2M_N	3	GND		
		GND	4	*1 GBTCLK0_M2C_P	AD32	126
		GND	5	*1 GBTCLK0_M2C_N	AD33	126
126	AG38	DP0_M2C_P	6	GND		
126	AG39	DP0_M2C_N	7	GND		
		GND	8	LA01_P_CC	AL29	24
		GND	9	LA01_N_CC	AM29	24
24	AP29	LA06_P	10	GND		
24	AR30	LA06_N	11	LA05_P	AK32	24
		GND	12	LA05_N	AL32	24
		GND	13	GND		
25	AM36	LA10_P	14	LA09_P	AU32	24
25	AM37	LA10_N	15	LA09_N	AV32	24
		GND	16	GND		
		GND	17	LA13_P	AU37	25
25	AR37	LA14_P	18	LA13_N	AV37	25
25	AT37	LA14_N	19	GND		
		GND	20	LA17_P_CC	AP36	25
		GND	21	LA17_N_CC	AR36	25
25	AR38	LA18_P_CC	22	GND		
25	AT38	LA18_N_CC	23	LA23_P	AN34	25
		GND	24	LA23_N	AP34	25
		GND	25	GND		
24	AJ30	LA27_P	26	LA26_P	AL37	25
24	AK30	LA27_N	27	LA26_N	AL38	25
		GND	28	GND		
		GND	29	TCK	-	
	-	*2 SCL	30	*4 TDI	-	
	-	*2 SDA	31	*4 TDO	-	
		GND	32	*6 3P3VAUX	-	
		GND	33	TMS	-	
	-	*3 GA0	34	TRST_L	-	
	-	*6 12P0V	35	*3 GA1	-	
		GND	36	*6 3P3V	-	
	-	*6 12P0V	37	GND		
		GND	38	*6 3P3V	-	
	-	*6 3P3V	39	GND		
		GND	40	*6 3P3V	-	

FMC 3 (J8)

Bank#	Pin#	E		F	Pin#	Bank#
		GND	1	*5 PG_M2C	-	
	-	HA01_P_CC	2	GND		
	-	HA01_N_CC	3	GND		
		GND	4	HA00_P_CC	-	
		GND	5	HA00_N_CC	-	
	-	HA05_P	6	GND		
	-	HA05_N	7	HA04_P	-	
		GND	8	HA04_N	-	
	-	HA09_P	9	GND		
	-	HA09_N	10	HA08_P	-	
		GND	11	HA08_N	-	
	-	HA13_P	12	GND		
	-	HA13_N	13	HA12_P	-	
		GND	14	HA12_N	-	
	-	HA16_P	15	GND		
	-	HA16_N	16	HA15_P	-	
		GND	17	HA15_N	-	
	-	HA20_P	18	GND		
	-	HA20_N	19	HA19_P	-	
		GND	20	HA19_N	-	
	-	HB03_P	21	GND		
	-	HB03_N	22	HB02_P	-	
		GND	23	HB02_N	-	
	-	HB05_P	24	GND		
	-	HB05_N	25	HB04_P	-	
		GND	26	HB04_N	-	
	-	HB09_P	27	GND		
	-	HB09_N	28	HB08_P	-	
		GND	29	HB08_N	-	
	-	HB13_P	30	GND		
	-	HB13_N	31	HB12_P	-	
		GND	32	HB12_N	-	
	-	HB19_P	33	GND		
	-	HB19_N	34	HB16_P	-	
		GND	35	HB16_N	-	
	-	HB21_P	36	GND		
	-	HB21_N	37	HB20_P	-	
		GND	38	HB20_N	-	
	-	*6 VADJ	39	GND		
		GND	40	*6 VADJ	-	

FMC 3 (J8)

Bank#	Pin#	G		H	Pin#	Bank#
		GND	1	*7 VREF_A_M2C	-	
24	AL30	CLK1_M2C_P	2	*5 PRSNT_M2C_L	-	
24	AM30	CLK1_M2C_N	3	GND		
		GND	4	CLK0_M2C_P	AM31	24
		GND	5	CLK0_M2C_N	AN31	24
24	AM32	LA00_P_CC	6	GND		
24	AN32	LA00_N_CC	7	LA02_P	AT29	24
		GND	8	LA02_N	AT30	24
24	AV29	LA03_P	9	GND		
24	AW29	LA03_N	10	LA04_P	AU29	24
		GND	11	LA04_N	AU30	24
24	AW30	LA08_P	12	GND		
24	AW31	LA08_N	13	LA07_P	AU31	24
		GND	14	LA07_N	AV31	24
24	AP30	LA12_P	15	GND		
24	AP31	LA12_N	16	LA11_P	AR31	24
		GND	17	LA11_N	AR32	24
25	AU36	LA16_P	18	GND		
25	AV36	LA16_N	19	LA15_P	AN33	24
		GND	20	LA15_N	AP33	24
25	AV38	LA20_P	21	GND		
25	AV39	LA20_N	22	LA19_P	AT39	25
		GND	23	LA19_N	AU39	25
25	AN38	LA22_P	24	GND		
25	AP38	LA22_N	25	LA21_P	AN39	25
		GND	26	LA21_N	AP39	25
25	AL39	LA25_P	27	GND		
25	AM39	LA25_N	28	LA24_P	AM34	25
		GND	29	LA24_N	AM35	25
24	AJ31	LA29_P	30	GND		
24	AK31	LA29_N	31	LA28_P	AN36	25
		GND	32	LA28_N	AN37	25
24	AJ33	LA31_P	33	GND		
24	AK33	LA31_N	34	LA30_P	AK37	25
		GND	35	LA30_N	AK38	25
25	AK35	LA33_P	36	GND		
25	AK36	LA33_N	37	LA32_P	AL34	25
		GND	38	LA32_N	AL35	25
	-	*6 VADJ	39	GND		
		GND	40	*6 VADJ	-	

FMC 3 (J8)

Bank#	Pin#	J		K	Pin#	Bank#
		GND	1	*7 VREF_B_M2C	-	
	-	CLK3_M2C_P	2	GND		
	-	CLK3_M2C_N	3	GND		
		GND	4	CLK2_M2C_P	-	
		GND	5	CLK2_M2C_N	-	
	-	HA03_P	6	GND		
	-	HA03_N	7	HA02_P	-	
		GND	8	HA02_N	-	
	-	HA07_P	9	GND		
	-	HA07_N	10	HA06_P	-	
		GND	11	HA06_N	-	
	-	HA11_P	12	GND		
	-	HA11_N	13	HA10_P	-	
		GND	14	HA10_N	-	
	-	HA14_P	15	GND		
	-	HA14_N	16	HA17_P_CC	-	
		GND	17	HA17_N_CC	-	
	-	HA18_P	18	GND		
	-	HA18_N	19	HA21_P	-	
		GND	20	HA21_N	-	
	-	HA22_P	21	GND		
	-	HA22_N	22	HA23_P	-	
		GND	23	HA23_N	-	
	-	HB01_P	24	GND		
	-	HB01_N	25	HB00_P_CC	-	
		GND	26	HB00_N_CC	-	
	-	HB07_P	27	GND		
	-	HB07_N	28	HB06_P_CC	-	
		GND	29	HB06_N_CC	-	
	-	HB11_P	30	GND		
	-	HB11_N	31	HB10_P	-	
		GND	32	HB10_N	-	
	-	HB15_P	33	GND		
	-	HB15_N	34	HB14_P	-	
		GND	35	HB14_N	-	
	-	HB18_P	36	GND		
	-	HB18_N	37	HB17_P_CC	-	
		GND	38	HB17_N_CC	-	
	-	*8 VIO_B_M2C	39	GND		
		GND	40	*8 VIO_B_M2C	-	

For FMC 3 (J8):

*1: GBTCLK[0:1]_M2C_P/N

These clocks are connected to Quad 126 of the FPGA while this board provides an MMCX interface for one pair of clocks on Quad 127. The other pair is provided by the system clock buffer.

*2: SCL, SDA

The board provides test points with pull-up options to enable I2C communication with the FPGA. By default, the pull-ups are not populated.

*3: GA0, GA1

This board provides pull-up or pull-down options for these connections, by default they are floating.

*4: TDI, TDO

The JTAG TDO pin is connected with a loopback to TDI through a 0 ohm resistor that is not populated by default.

*5: PG_C2M, PG_M2C, PRSNT_M2C_N

These all have a pull-up or pull-down resistor option. However, the resistors are not populated by default, these pins are floating.

*6: Power Rails

This card provides a 12V output through the 12V0 pins and 3.3V output through the 3V3 and 3V3_AUX pins. It is important to note that all the FMC connectors present on this board are equipped with a fuse on the 12V0 rail. Lastly, the VADJ pins provide a 1.8V rail to FPGA mezzanine cards.

*7: VREF_A_M2C, VREF_B_M2C

These terminals can be monitored by test points **TP83** and **TP84**.

*8: VIO_B_M2C

Both pins J39 and K40 for this terminal can also be monitored by test point **TP81**.

6.4.5. FMC HPC 4 (J11)

This FMC connects GTH lanes and 6 differential pairs of LA signals to banks on the FPGA.

High Speed:

Quad 228(XCKU060) / Quad 228 and 229(XCKU115):

- 4 GTH lanes (XCKU060) / 8 GTH lanes (XCKU115)
- 2 differential clock pairs

Low Speed:

Bank 44:

- 6 differential LA pairs

FMC4 connects DP4, DP5, DP6, and DP7 at XCKU060 device. (DP0, DP1, DP2, and DP3 are not connected)

Table 6-9 FMC 4 (J11) to FPGA Pinout

Bank#	Pin#	A		B	Pin#	Bank#
		GND	1	CLK_DIR	-	
229(115)	P2	DP1_M2C_P	2	GND		
229(115)	P1	DP1_M2C_N	3	GND		
		GND	4	DP9_M2C_P	-	
		GND	5	DP9_M2C_N	-	
229(115)	R4	DP2_M2C_P	6	GND		
229(115)	R3	DP2_M2C_N	7	GND		
		GND	8	DP8_M2C_P	-	
		GND	9	DP8_M2C_N	-	
229(115)	T2	DP3_M2C_P	10	GND		
229(115)	T1	DP3_M2C_N	11	GND		
		GND	12	DP7_M2C_P	V2	228
		GND	13	DP7_M2C_N	V1	228
228	W4	DP4_M2C_P	14	GND		
228	W3	DP4_M2C_N	15	GND		
		GND	16	DP6_M2C_P	Y2	228
		GND	17	DP6_M2C_N	Y1	228
228	AB2	DP5_M2C_P	18	GND		
228	AB1	DP5_M2C_N	19	GND		
		GND	20	*1 GBTCLK1_M2C_P	W8	228
		GND	21	*1 GBTCLK1_M2C_N	W7	228
229(115)	P6	DP1_C2M_P	22	GND		
229(115)	P5	DP1_C2M_N	23	GND		
		GND	24	DP9_C2M_P	-	
		GND	25	DP9_C2M_N	-	
229(115)	T6	DP2_C2M_P	26	GND		
229(115)	T5	DP2_C2M_N	27	GND		
		GND	28	DP8_C2M_P	-	
		GND	29	DP8_C2M_N	-	
229(115)	U4	DP3_C2M_P	30	GND		
229(115)	U3	DP3_C2M_N	31	GND		
		GND	32	DP7_C2M_P	V6	228
		GND	33	DP7_C2M_N	V5	228
228	Y6	DP4_C2M_P	34	GND		
228	Y5	DP4_C2M_N	35	GND		
		GND	36	DP6_C2M_P	AA4	228
		GND	37	DP6_C2M_N	AA3	228
228	AB6	DP5_C2M_P	38	GND		
228	AB5	DP5_C2M_N	39	GND		
		GND	40	RES0	-	

FMC 4 (J11)

Bank#	Pin#	C		D	Pin#	Bank#
		GND	1	*5 PG_C2M	-	
229(115)	N8	DP0_C2M_P	2	GND		
229(115)	N7	DP0_C2M_N	3	GND		
		GND	4	*1 GBTCLK0_M2C_P	AA8	228
		GND	5	*1 GBTCLK0_M2C_N	AA7	228
229(115)	N4	DP0_M2C_P	6	GND		
229(115)	N3	DP0_M2C_N	7	GND		
		GND	8	LA01_P_CC	-	
		GND	9	LA01_N_CC	-	
	-	LA06_P	10	GND		
	-	LA06_N	11	LA05_P	-	
		GND	12	LA05_N	-	
		GND	13	GND		
	-	LA10_P	14	LA09_P	-	
	-	LA10_N	15	LA09_N	-	
		GND	16	GND		
		GND	17	LA13_P	-	
	-	LA14_P	18	LA13_N	-	
	-	LA14_N	19	GND		
		GND	20	LA17_P_CC	-	
		GND	21	LA17_N_CC	-	
	-	LA18_P_CC	22	GND		
	-	LA18_N_CC	23	LA23_P	-	
		GND	24	LA23_N	-	
		GND	25	GND		
	-	LA27_P	26	LA26_P	-	
	-	LA27_N	27	LA26_N	-	
		GND	28	GND		
		GND	29	TCK	-	
	-	*2 SCL	30	*4 TDI	-	
	-	*2 SDA	31	*4 TDO	-	
		GND	32	*6 3P3VAUX	-	
		GND	33	TMS	-	
	-	*3 GA0	34	TRST_L	-	
	-	*6 12P0V	35	*3 GA1	-	
		GND	36	*6 3P3V	-	
	-	*6 12P0V	37	GND		
		GND	38	*6 3P3V	-	
	-	*6 3P3V	39	GND		
		GND	40	*6 3P3V	-	

FMC 4 (J11)

Bank#	Pin#	E		F	Pin#	Bank#
		GND	1	*5 PG_M2C	-	
	-	HA01_P_CC	2	GND		
	-	HA01_N_CC	3	GND		
		GND	4	HA00_P_CC	-	
		GND	5	HA00_N_CC	-	
	-	HA05_P	6	GND		
	-	HA05_N	7	HA04_P	-	
		GND	8	HA04_N	-	
	-	HA09_P	9	GND		
	-	HA09_N	10	HA08_P	-	
		GND	11	HA08_N	-	
	-	HA13_P	12	GND		
	-	HA13_N	13	HA12_P	-	
		GND	14	HA12_N	-	
	-	HA16_P	15	GND		
	-	HA16_N	16	HA15_P	-	
		GND	17	HA15_N	-	
	-	HA20_P	18	GND		
	-	HA20_N	19	HA19_P	-	
		GND	20	HA19_N	-	
	-	HB03_P	21	GND		
	-	HB03_N	22	HB02_P	-	
		GND	23	HB02_N	-	
	-	HB05_P	24	GND		
	-	HB05_N	25	HB04_P	-	
		GND	26	HB04_N	-	
	-	HB09_P	27	GND		
	-	HB09_N	28	HB08_P	-	
		GND	29	HB08_N	-	
	-	HB13_P	30	GND		
	-	HB13_N	31	HB12_P	-	
		GND	32	HB12_N	-	
	-	HB19_P	33	GND		
	-	HB19_N	34	HB16_P	-	
		GND	35	HB16_N	-	
	-	HB21_P	36	GND		
	-	HB21_N	37	HB20_P	-	
		GND	38	HB20_N	-	
	-	*6 VADJ	39	GND		
		GND	40	*6 VADJ	-	

FMC 4 (J11)

Bank#	Pin#	G		H	Pin#	Bank#
		GND	1	*7 VREF_A_M2C	-	
	-	CLK1_M2C_P	2	*5 PRSNT_M2C_L	-	
	-	CLK1_M2C_N	3	GND		
		GND	4	CLK0_M2C_P	-	
		GND	5	CLK0_M2C_N	-	
44	AG21	LA00_P_CC	6	GND		
44	AG22	LA00_N_CC	7	LA02_P	-	
		GND	8	LA02_N	-	
44	AE23	LA03_P	9	GND		
44	AF23	LA03_N	10	LA04_P	-	
		GND	11	LA04_N	-	
44	AD20	LA08_P	12	GND		
44	AD21	LA08_N	13	LA07_P	-	
		GND	14	LA07_N	-	
44	AE20	LA12_P	15	GND		
44	AE21	LA12_N	16	LA11_P	-	
		GND	17	LA11_N	-	
44	AE22	LA16_P	18	GND		
44	AF22	LA16_N	19	LA15_P	-	
		GND	20	LA15_N	-	
	-	LA20_P	21	GND		
	-	LA20_N	22	LA19_P	-	
		GND	23	LA19_N	-	
44	AF20	LA22_P	24	GND		
44	AG20	LA22_N	25	LA21_P	-	
		GND	26	LA21_N	-	
	-	LA25_P	27	GND		
	-	LA25_N	28	LA24_P	-	
		GND	29	LA24_N	-	
	-	LA29_P	30	GND		
	-	LA29_N	31	LA28_P	-	
		GND	32	LA28_N	-	
	-	LA31_P	33	GND		
	-	LA31_N	34	LA30_P	-	
		GND	35	LA30_N	-	
	-	LA33_P	36	GND		
	-	LA33_N	37	LA32_P	-	
		GND	38	LA32_N	-	
	-	*6 VADJ	39	GND		
		GND	40	*6 VADJ	-	

FMC 4 (J11)

Bank#	Pin#	J		K	Pin#	Bank#
		GND	1	*7 VREF_B_M2C	-	
	-	CLK3_M2C_P	2	GND		
	-	CLK3_M2C_N	3	GND		
		GND	4	CLK2_M2C_P	-	
		GND	5	CLK2_M2C_N	-	
	-	HA03_P	6	GND		
	-	HA03_N	7	HA02_P	-	
		GND	8	HA02_N	-	
	-	HA07_P	9	GND		
	-	HA07_N	10	HA06_P	-	
		GND	11	HA06_N	-	
	-	HA11_P	12	GND		
	-	HA11_N	13	HA10_P	-	
		GND	14	HA10_N	-	
	-	HA14_P	15	GND		
	-	HA14_N	16	HA17_P_CC	-	
		GND	17	HA17_N_CC	-	
	-	HA18_P	18	GND		
	-	HA18_N	19	HA21_P	-	
		GND	20	HA21_N	-	
	-	HA22_P	21	GND		
	-	HA22_N	22	HA23_P	-	
		GND	23	HA23_N	-	
	-	HB01_P	24	GND		
	-	HB01_N	25	HB00_P_CC	-	
		GND	26	HB00_N_CC	-	
	-	HB07_P	27	GND		
	-	HB07_N	28	HB06_P_CC	-	
		GND	29	HB06_N_CC	-	
	-	HB11_P	30	GND		
	-	HB11_N	31	HB10_P	-	
		GND	32	HB10_N	-	
	-	HB15_P	33	GND		
	-	HB15_N	34	HB14_P	-	
		GND	35	HB14_N	-	
	-	HB18_P	36	GND		
	-	HB18_N	37	HB17_P_CC	-	
		GND	38	HB17_N_CC	-	
	-	*8 VIO_B_M2C	39	GND		
		GND	40	*8 VIO_B_M2C	-	

For FMC 4 (J11):

*1: GBTCLK[0:1]_M2C_P/N

These clocks are connected to Quad 228 (XCKU060 and 115) of the FPGA while this board provides an MMCX interface for one pair of clocks on Quad 229 (XCKU115). The other pair is provided by the system clock buffer.

*2: SCL, SDA

The board provides test points with pull-up options to enable I2C communication with the FPGA. By default, the pull-ups are not populated.

*3: GA0, GA1

This board provides pull-up or pull-down options for these connections, by default they are floating.

*4: TDI, TDO

The JTAG TDO pin is connected with a loopback to TDI through a 0 ohm resistor that is not populated by default.

*5: PG_C2M, PG_M2C, PRSNT_M2C_N

These all have a pull-up or pull-down resistor option. However, the resistors are not populated by default, these pins are floating.

*6: Power Rails

This card provides a 12V output through the 12V0 pins and 3.3V output through the 3V3 and 3V3_AUX pins. It is important to note that all the FMC connectors present on this board are equipped with a fuse on the 12V0 rail. Lastly, the VADJ pins provide a 1.8V rail to FPGA mezzanine cards.

*7: VREF_A_M2C, VREF_B_M2C

These terminals can be monitored by test points **TP87** and **TP88**.

*8: VIO_B_M2C

Both pins J39 and K40 for this terminal can also be monitored by test point **TP85**.

6.4.6. FMC HPC 5 (J14)

This FMC connects GTH lanes (XCKU115 only) and 6 differential pairs of LA signals to banks on the FPGA.

High Speed:

No GTH (XCKU060) / Quad 230 and 231 (XCKU115):

- 8 GTH lanes (XCKU115)
- 2 differential clock pairs

Low Speed:

Bank 45:

- 6 differential LA pairs

Table 6-10 FMC 5 (J14) to FPGA Pinout

Bank#	Pin#	A		B	Pin#	Bank#
		GND	1	CLK_DIR	-	
231(115)	F2	DP1_M2C_P	2	GND		
231(115)	F1	DP1_M2C_N	3	GND		
		GND	4	DP9_M2C_P	-	
		GND	5	DP9_M2C_N	-	
231(115)	G4	DP2_M2C_P	6	GND		
231(115)	G3	DP2_M2C_N	7	GND		
		GND	8	DP8_M2C_P	-	
		GND	9	DP8_M2C_N	-	
231(115)	H2	DP3_M2C_P	10	GND		
231(115)	H1	DP3_M2C_N	11	GND		
		GND	12	DP7_M2C_P	J4	230(115)
		GND	13	DP7_M2C_N	J3	230(115)
230(115)	K2	DP4_M2C_P	14	GND		
230(115)	K1	DP4_M2C_N	15	GND		
		GND	16	DP6_M2C_P	L4	230(115)
		GND	17	DP6_M2C_N	L3	230(115)
230(115)	M2	DP5_M2C_P	18	GND		
230(115)	M1	DP5_M2C_N	19	GND		
		GND	20	*1 GBTCLK1_M2C_P	M10	230(115)
		GND	21	*1 GBTCLK1_M2C_N	M9	230(115)
231(115)	F6	DP1_C2M_P	22	GND		
231(115)	F5	DP1_C2M_N	23	GND		
		GND	24	DP9_C2M_P	-	
		GND	25	DP9_C2M_N	-	
231(115)	G8	DP2_C2M_P	26	GND		
231(115)	G7	DP2_C2M_N	27	GND		
		GND	28	DP8_C2M_P	-	
		GND	29	DP8_C2M_N	-	
231(115)	H6	DP3_C2M_P	30	GND		
231(115)	H5	DP3_C2M_N	31	GND		
		GND	32	DP7_C2M_P	J8	230(115)
		GND	33	DP7_C2M_N	J7	230(115)
230(115)	K6	DP4_C2M_P	34	GND		
230(115)	K5	DP4_C2M_N	35	GND		
		GND	36	DP6_C2M_P	L8	230(115)
		GND	37	DP6_C2M_N	L7	230(115)
230(115)	M6	DP5_C2M_P	38	GND		
230(115)	M5	DP5_C2M_N	39	GND		
		GND	40	RES0	-	

FMC 5 (J14)

Bank#	Pin#	C		D	Pin#	Bank#
		GND	1	*5 PG_C2M	-	
231(115)	E8	DP0_C2M_P	2	GND		
231(115)	E7	DP0_C2M_N	3	GND		
		GND	4	*1 GBTCLK0_M2C_P	P10	230(115)
		GND	5	*1 GBTCLK0_M2C_N	P9	230(115)
231(115)	E4	DP0_M2C_P	6	GND		
231(115)	E3	DP0_M2C_N	7	GND		
		GND	8	LA01_P_CC	-	
		GND	9	LA01_N_CC	-	
	-	LA06_P	10	GND		
	-	LA06_N	11	LA05_P	-	
		GND	12	LA05_N	-	
		GND	13	GND		
	-	LA10_P	14	LA09_P	-	
	-	LA10_N	15	LA09_N	-	
		GND	16	GND		
		GND	17	LA13_P	-	
	-	LA14_P	18	LA13_N	-	
	-	LA14_N	19	GND		
		GND	20	LA17_P_CC	-	
		GND	21	LA17_N_CC	-	
	-	LA18_P_CC	22	GND		
	-	LA18_N_CC	23	LA23_P	-	
		GND	24	LA23_N	-	
		GND	25	GND		
	-	LA27_P	26	LA26_P	-	
	-	LA27_N	27	LA26_N	-	
		GND	28	GND		
		GND	29	TCK	-	
	-	*2 SCL	30	*4 TDI	-	
	-	*2 SDA	31	*4 TDO	-	
		GND	32	*6 3P3VAUX	-	
		GND	33	TMS	-	
	-	*3 GA0	34	TRST_L	-	
	-	*6 12P0V	35	*3 GA1	-	
		GND	36	*6 3P3V	-	
	-	*6 12P0V	37	GND		
		GND	38	*6 3P3V	-	
	-	*6 3P3V	39	GND		
		GND	40	*6 3P3V	-	

FMC 5 (J14)

Bank#	Pin#	E		F	Pin#	Bank#
		GND	1	*5 PG_M2C	-	
	-	HA01_P_CC	2	GND		
	-	HA01_N_CC	3	GND		
		GND	4	HA00_P_CC	-	
		GND	5	HA00_N_CC	-	
	-	HA05_P	6	GND		
	-	HA05_N	7	HA04_P	-	
		GND	8	HA04_N	-	
	-	HA09_P	9	GND		
	-	HA09_N	10	HA08_P	-	
		GND	11	HA08_N	-	
	-	HA13_P	12	GND		
	-	HA13_N	13	HA12_P	-	
		GND	14	HA12_N	-	
	-	HA16_P	15	GND		
	-	HA16_N	16	HA15_P	-	
		GND	17	HA15_N	-	
	-	HA20_P	18	GND		
	-	HA20_N	19	HA19_P	-	
		GND	20	HA19_N	-	
	-	HB03_P	21	GND		
	-	HB03_N	22	HB02_P	-	
		GND	23	HB02_N	-	
	-	HB05_P	24	GND		
	-	HB05_N	25	HB04_P	-	
		GND	26	HB04_N	-	
	-	HB09_P	27	GND		
	-	HB09_N	28	HB08_P	-	
		GND	29	HB08_N	-	
	-	HB13_P	30	GND		
	-	HB13_N	31	HB12_P	-	
		GND	32	HB12_N	-	
	-	HB19_P	33	GND		
	-	HB19_N	34	HB16_P	-	
		GND	35	HB16_N	-	
	-	HB21_P	36	GND		
	-	HB21_N	37	HB20_P	-	
		GND	38	HB20_N	-	
	-	*6 VADJ	39	GND		
		GND	40	*6 VADJ	-	

FMC 5 (J14)

Bank#	Pin#	G		H	Pin#	Bank#
		GND	1	*7 VREF_A_M2C	-	
	-	CLK1_M2C_P	2	*5 PRSNT_M2C_L	-	
	-	CLK1_M2C_N	3	GND		
		GND	4	CLK0_M2C_P	-	
		GND	5	CLK0_M2C_N	-	
45	AD25	LA00_P_CC	6	GND		
45	AE25	LA00_N_CC	7	LA02_P	-	
		GND	8	LA02_N	-	
45	AG26	LA03_P	9	GND		
45	AG27	LA03_N	10	LA04_P	-	
		GND	11	LA04_N	-	
45	AE27	LA08_P	12	GND		
45	AF27	LA08_N	13	LA07_P	-	
		GND	14	LA07_N	-	
45	AD26	LA12_P	15	GND		
45	AE26	LA12_N	16	LA11_P	-	
		GND	17	LA11_N	-	
45	AF25	LA16_P	18	GND		
45	AG25	LA16_N	19	LA15_P	-	
		GND	20	LA15_N	-	
	-	LA20_P	21	GND		
	-	LA20_N	22	LA19_P	-	
		GND	23	LA19_N	-	
45	AF24	LA22_P	24	GND		
45	AG24	LA22_N	25	LA21_P	-	
		GND	26	LA21_N	-	
	-	LA25_P	27	GND		
	-	LA25_N	28	LA24_P	-	
		GND	29	LA24_N	-	
	-	LA29_P	30	GND		
	-	LA29_N	31	LA28_P	-	
		GND	32	LA28_N	-	
	-	LA31_P	33	GND		
	-	LA31_N	34	LA30_P	-	
		GND	35	LA30_N	-	
	-	LA33_P	36	GND		
	-	LA33_N	37	LA32_P	-	
		GND	38	LA32_N	-	
	-	*6 VADJ	39	GND		
		GND	40	*6 VADJ	-	

FMC 5 (J14)

Bank#	Pin#	J		K	Pin#	Bank#
		GND	1	*7 VREF_B_M2C	-	
	-	CLK3_M2C_P	2	GND		
	-	CLK3_M2C_N	3	GND		
		GND	4	CLK2_M2C_P	-	
		GND	5	CLK2_M2C_N	-	
	-	HA03_P	6	GND		
	-	HA03_N	7	HA02_P	-	
		GND	8	HA02_N	-	
	-	HA07_P	9	GND		
	-	HA07_N	10	HA06_P	-	
		GND	11	HA06_N	-	
	-	HA11_P	12	GND		
	-	HA11_N	13	HA10_P	-	
		GND	14	HA10_N	-	
	-	HA14_P	15	GND		
	-	HA14_N	16	HA17_P_CC	-	
		GND	17	HA17_N_CC	-	
	-	HA18_P	18	GND		
	-	HA18_N	19	HA21_P	-	
		GND	20	HA21_N	-	
	-	HA22_P	21	GND		
	-	HA22_N	22	HA23_P	-	
		GND	23	HA23_N	-	
	-	HB01_P	24	GND		
	-	HB01_N	25	HB00_P_CC	-	
		GND	26	HB00_N_CC	-	
	-	HB07_P	27	GND		
	-	HB07_N	28	HB06_P_CC	-	
		GND	29	HB06_N_CC	-	
	-	HB11_P	30	GND		
	-	HB11_N	31	HB10_P	-	
		GND	32	HB10_N	-	
	-	HB15_P	33	GND		
	-	HB15_N	34	HB14_P	-	
		GND	35	HB14_N	-	
	-	HB18_P	36	GND		
	-	HB18_N	37	HB17_P_CC	-	
		GND	38	HB17_N_CC	-	
	-	*8 VIO_B_M2C	39	GND		
		GND	40	*8 VIO_B_M2C	-	

For FMC 5 (J14):

*1: GBTCLK[0:1]_M2C_P/N

These clocks are connected to Quad 230 (XCKU115 only) of the FPGA while this board provides an MMCX interface for one pair of clocks on Quad 231 (XCKU115 only). The other pair is provided by the system clock buffer.

*2: SCL, SDA

The board provides test points with pull-up options to enable I2C communication with the FPGA. By default, the pull-ups are not populated.

*3: GA0, GA1

This board provides pull-up or pull-down options for these connections, by default they are floating.

*4: TDI, TDO

The JTAG TDO pin is connected with a loopback to TDI through a 0 ohm resistor that is not populated by default.

*5: PG_C2M, PG_M2C, PRSNT_M2C_N

These all have a pull-up or pull-down resistor option. However, the resistors are not populated by default, these pins are floating.

*6: Power Rails

This card provides a 12V output through the 12V0 pins and 3.3V output through the 3V3 and 3V3_AUX pins. It is important to note that all the FMC connectors present on this board are equipped with a fuse on the 12V0 rail. Lastly, the VADJ pins provide a 1.8V rail to FPGA mezzanine cards.

*7: VREF_A_M2C, VREF_B_M2C

These terminals can be monitored by test points **TP91** and **TP92**.

*8: VIO_B_M2C

Both pins J39 and K40 for this terminal can also be monitored by test point **TP89**.

6.4.7. FMC HPC 6 (J19)

This FMC connects GTH lanes and 6 differential pairs of LA signals to banks on the FPGA.

High Speed:

Quad 128:

- 4 GTH lanes
- 2 differential clock pairs

Low Speed:

Bank 24:

- 6 differential LA pairs

Table 6-11 FMC 6 (J19) to FPGA Pinout

Bank#	Pin#	A		B	Pin#	Bank#
		GND	1	CLK_DIR	-	
128	U38	DP1_M2C_P	2	GND		
128	U39	DP1_M2C_N	3	GND		
		GND	4	DP9_M2C_P	-	
		GND	5	DP9_M2C_N	-	
128	R38	DP2_M2C_P	6	GND		
128	R39	DP2_M2C_N	7	GND		
		GND	8	DP8_M2C_P	-	
		GND	9	DP8_M2C_N	-	
128	N38	DP3_M2C_P	10	GND		
128	N39	DP3_M2C_N	11	GND		
		GND	12	DP7_M2C_P	-	
		GND	13	DP7_M2C_N	-	
	-	DP4_M2C_P	14	GND		
	-	DP4_M2C_N	15	GND		
		GND	16	DP6_M2C_P	-	
		GND	17	DP6_M2C_N	-	
	-	DP5_M2C_P	18	GND		
	-	DP5_M2C_N	19	GND		
		GND	20	*1 GBTCLK1_M2C_P	P32	128
		GND	21	*1 GBTCLK1_M2C_N	P33	128
128	U34	DP1_C2M_P	22	GND		
128	U35	DP1_C2M_N	23	GND		
		GND	24	DP9_C2M_P	-	
		GND	25	DP9_C2M_N	-	
128	T36	DP2_C2M_P	26	GND		
128	T37	DP2_C2M_N	27	GND		
		GND	28	DP8_C2M_P	-	
		GND	29	DP8_C2M_N	-	
128	N34	DP3_C2M_P	30	GND		
128	N35	DP3_C2M_N	31	GND		
		GND	32	DP7_C2M_P	-	
		GND	33	DP7_C2M_N	-	
	-	DP4_C2M_P	34	GND		
	-	DP4_C2M_N	35	GND		
		GND	36	DP6_C2M_P	-	
		GND	37	DP6_C2M_N	-	
	-	DP5_C2M_P	38	GND		
	-	DP5_C2M_N	39	GND		
		GND	40	RES0	-	

FMC 6 (J19)

Bank#	Pin#	C		D	Pin#	Bank#
		GND	1	*5 PG_C2M	-	
128	R34	DP0_C2M_P	2	GND		
128	R35	DP0_C2M_N	3	GND		
		GND	4	*1 GBTCLK0_M2C_P	T32	128
		GND	5	*1 GBTCLK0_M2C_N	T33	128
128	P36	DP0_M2C_P	6	GND		
128	P37	DP0_M2C_N	7	GND		
		GND	8	LA01_P_CC	-	
		GND	9	LA01_N_CC	-	
	-	LA06_P	10	GND		
	-	LA06_N	11	LA05_P	-	
		GND	12	LA05_N	-	
		GND	13	GND		
	-	LA10_P	14	LA09_P	-	
	-	LA10_N	15	LA09_N	-	
		GND	16	GND		
		GND	17	LA13_P	-	
	-	LA14_P	18	LA13_N	-	
	-	LA14_N	19	GND		
		GND	20	LA17_P_CC	-	
		GND	21	LA17_N_CC	-	
	-	LA18_P_CC	22	GND		
	-	LA18_N_CC	23	LA23_P	-	
		GND	24	LA23_N	-	
		GND	25	GND		
	-	LA27_P	26	LA26_P	-	
	-	LA27_N	27	LA26_N	-	
		GND	28	GND		
		GND	29	TCK	-	
	-	*2 SCL	30	*4 TDI	-	
	-	*2 SDA	31	*4 TDO	-	
		GND	32	*6 3P3VAUX	-	
		GND	33	TMS	-	
	-	*3 GA0	34	TRST_L	-	
	-	*6 12P0V	35	*3 GA1	-	
		GND	36	*6 3P3V	-	
	-	*6 12P0V	37	GND		
		GND	38	*6 3P3V	-	
	-	*6 3P3V	39	GND		
		GND	40	*6 3P3V	-	

FMC 6 (J19)

Bank#	Pin#	E		F	Pin#	Bank#
		GND	1	*5 PG_M2C	-	
	-	HA01_P_CC	2	GND		
	-	HA01_N_CC	3	GND		
		GND	4	HA00_P_CC	-	
		GND	5	HA00_N_CC	-	
	-	HA05_P	6	GND		
	-	HA05_N	7	HA04_P	-	
		GND	8	HA04_N	-	
	-	HA09_P	9	GND		
	-	HA09_N	10	HA08_P	-	
		GND	11	HA08_N	-	
	-	HA13_P	12	GND		
	-	HA13_N	13	HA12_P	-	
		GND	14	HA12_N	-	
	-	HA16_P	15	GND		
	-	HA16_N	16	HA15_P	-	
		GND	17	HA15_N	-	
	-	HA20_P	18	GND		
	-	HA20_N	19	HA19_P	-	
		GND	20	HA19_N	-	
	-	HB03_P	21	GND		
	-	HB03_N	22	HB02_P	-	
		GND	23	HB02_N	-	
	-	HB05_P	24	GND		
	-	HB05_N	25	HB04_P	-	
		GND	26	HB04_N	-	
	-	HB09_P	27	GND		
	-	HB09_N	28	HB08_P	-	
		GND	29	HB08_N	-	
	-	HB13_P	30	GND		
	-	HB13_N	31	HB12_P	-	
		GND	32	HB12_N	-	
	-	HB19_P	33	GND		
	-	HB19_N	34	HB16_P	-	
		GND	35	HB16_N	-	
	-	HB21_P	36	GND		
	-	HB21_N	37	HB20_P	-	
		GND	38	HB20_N	-	
	-	*6 VADJ	39	GND		
		GND	40	*6 VADJ	-	

FMC 6 (J19)

Bank#	Pin#	G		H	Pin#	Bank#
		GND	1	*7 VREF_A_M2C	-	
	-	CLK1_M2C_P	2	*5 PRSNT_M2C_L	-	
	-	CLK1_M2C_N	3	GND		
		GND	4	CLK0_M2C_P	-	
		GND	5	CLK0_M2C_N	-	
24	AH29	LA00_P_CC	6	GND		
24	AJ29	LA00_N_CC	7	LA02_P	-	
		GND	8	LA02_N	-	
24	AH31	LA03_P	9	GND		
24	AH32	LA03_N	10	LA04_P	-	
		GND	11	LA04_N	-	
24	AH28	LA08_P	12	GND		
24	AJ28	LA08_N	13	LA07_P	-	
		GND	14	LA07_N	-	
24	AE30	LA12_P	15	GND		
24	AF30	LA12_N	16	LA11_P	-	
		GND	17	LA11_N	-	
24	AF29	LA16_P	18	GND		
24	AG29	LA16_N	19	LA15_P	-	
		GND	20	LA15_N	-	
	-	LA20_P	21	GND		
	-	LA20_N	22	LA19_P	-	
		GND	23	LA19_N	-	
24	AE28	LA22_P	24	GND		
24	AF28	LA22_N	25	LA21_P	-	
		GND	26	LA21_N	-	
	-	LA25_P	27	GND		
	-	LA25_N	28	LA24_P	-	
		GND	29	LA24_N	-	
	-	LA29_P	30	GND		
	-	LA29_N	31	LA28_P	-	
		GND	32	LA28_N	-	
	-	LA31_P	33	GND		
	-	LA31_N	34	LA30_P	-	
		GND	35	LA30_N	-	
	-	LA33_P	36	GND		
	-	LA33_N	37	LA32_P	-	
		GND	38	LA32_N	-	
	-	*6 VADJ	39	GND		
		GND	40	*6 VADJ	-	

FMC 6 (J19)

Bank#	Pin#	J		K	Pin#	Bank#
		GND	1	*7 VREF_B_M2C	-	
	-	CLK3_M2C_P	2	GND		
	-	CLK3_M2C_N	3	GND		
		GND	4	CLK2_M2C_P	-	
		GND	5	CLK2_M2C_N	-	
	-	HA03_P	6	GND		
	-	HA03_N	7	HA02_P	-	
		GND	8	HA02_N	-	
	-	HA07_P	9	GND		
	-	HA07_N	10	HA06_P	-	
		GND	11	HA06_N	-	
	-	HA11_P	12	GND		
	-	HA11_N	13	HA10_P	-	
		GND	14	HA10_N	-	
	-	HA14_P	15	GND		
	-	HA14_N	16	HA17_P_CC	-	
		GND	17	HA17_N_CC	-	
	-	HA18_P	18	GND		
	-	HA18_N	19	HA21_P	-	
		GND	20	HA21_N	-	
	-	HA22_P	21	GND		
	-	HA22_N	22	HA23_P	-	
		GND	23	HA23_N	-	
	-	HB01_P	24	GND		
	-	HB01_N	25	HB00_P_CC	-	
		GND	26	HB00_N_CC	-	
	-	HB07_P	27	GND		
	-	HB07_N	28	HB06_P_CC	-	
		GND	29	HB06_N_CC	-	
	-	HB11_P	30	GND		
	-	HB11_N	31	HB10_P	-	
		GND	32	HB10_N	-	
	-	HB15_P	33	GND		
	-	HB15_N	34	HB14_P	-	
		GND	35	HB14_N	-	
	-	HB18_P	36	GND		
	-	HB18_N	37	HB17_P_CC	-	
		GND	38	HB17_N_CC	-	
	-	*8 VIO_B_M2C	39	GND		
		GND	40	*8 VIO_B_M2C	-	

For FMC 6 (J19):

*1: GBTCLK[0:1]_M2C_P/N

These clocks are connected to Quad 128 of the FPGA while this board provides an MMCX interface for one pair of clocks on Quad 232 (XCKU115 only). The other pair is provided by the system clock buffer.

*2: SCL, SDA

The board provides test points with pull-up options to enable I2C communication with the FPGA. By default, the pull-ups are not populated.

*3: GA0, GA1

This board provides pull-up or pull-down options for these connections, by default they are floating.

*4: TDI, TDO

The JTAG TDO pin is connected with a loopback to TDI through a 0 ohm resistor that is not populated by default.

*5: PG_C2M, PG_M2C, PRSNT_M2C_N

These all have a pull-up or pull-down resistor option. However, the resistors are not populated by default, these pins are floating.

*6: Power Rails

This card provides a 12V output through the 12V0 pins and 3.3V output through the 3V3 and 3V3_AUX pins. It is important to note that all the FMC connectors present on this board are equipped with a fuse on the 12V0 rail. Lastly, the VADJ pins provide a 1.8V rail to FPGA mezzanine cards.

*7: VREF_A_M2C, VREF_B_M2C

These terminals can be monitored by test points **TP95** and **TP96**.

*8: VIO_B_M2C

Both pins J39 and K40 for this terminal can also be monitored by test point **TP93**.

6.5. DDR4 SDRAM

This TB-KU-xxx-ACDC8K development board includes 8 DDR4 SDRAM memory components (Micron EDY4016AABG-DR-F). Control and address signals are wired in a fly-by routing topology.

DDR4 SDRAM

Capacity: 4Gbit (32M words x 16 bits x 8) x 8 components

Address Bus: 15bit (Row Address: 15bit, Column Address: 10bit)

Bank Address: 2bit

Bank Group: 1bit

Data Bus: Byte access with data strobe (DQS), Data Mask for each byte.

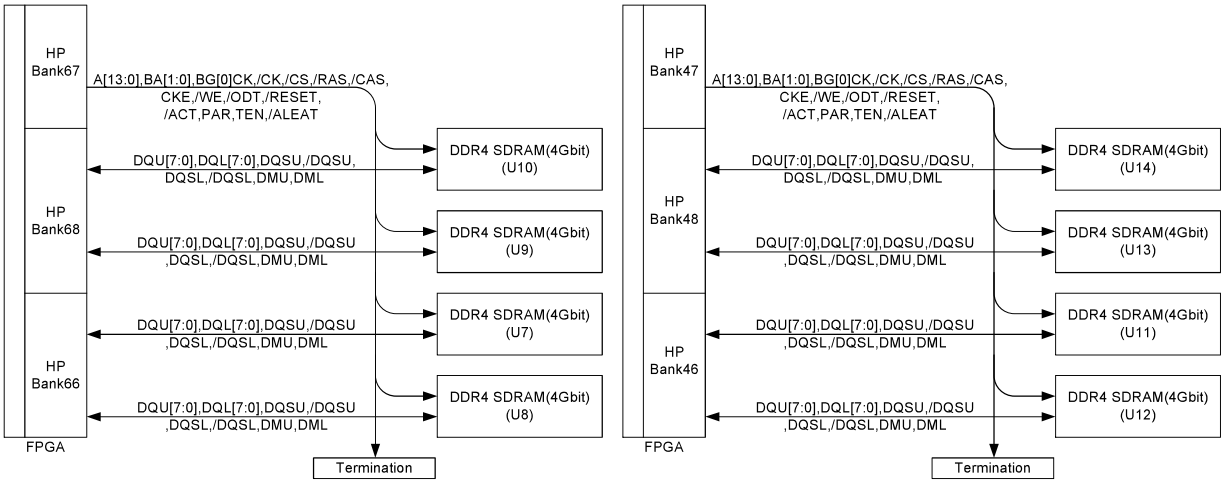
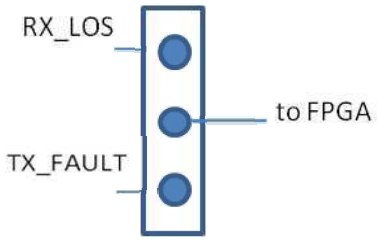


Figure 6-11 DDR4 SDRAM Structure

6.6. SFP+ Connectors

Located on the front panel of the TB-KU-xxx-ACDC8K are 4 SFP+ slots available to the user. These ports are standard single SFP+ modules. For each of these modules, a 3-pin connector is available to jumper between either RX_LOS or TX_FAULT. A jumper between pins 1-2 connects RX_LOS and between 3-2 connects TX_FAULT.



Each SFP+ connector has a TX and an RX differential data pair that connect to Quad 232 on the FPGA. They also connect to an I2C bus through TI's PCA9544A 4-to-1 I2C MUX with four available interrupt inputs for each of the downstream pairs. Available on the same component is a global interrupt input pin which acts as a logic AND for the four interrupts. The PCA9544A chip's I2C address can be set through the A[0:2] inputs through available 4.7k resistors on the board.

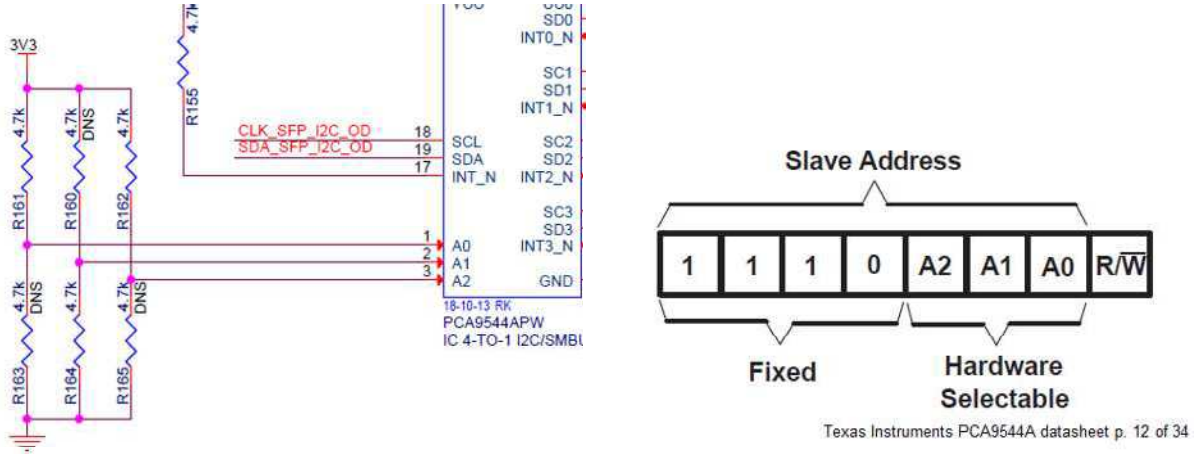


Figure 6-12 I2C MUX Hardware-selectable Address Pins

By default, the I2C address for this device is: 1110101_. If the last bit of the address is set to a logic 1, a read is selected and 0 for a write. Please refer to TI's PCA9544A datasheet for additional information concerning this component.

The SFP+ I2C multiplexed data and multiplexed clocks are connected to the FPGA's Bank 64.

Table 6-12 SFP+ I2C Bus Pin Assignment

I2C	Signal Name	FPGA Bank	Pin
SCL	CLK_SFP_I2C_FPGA_OD	64	AF19
SDA	SDA_SFP_I2C_FPGA_OD	64	AG19

Also, pins RS0 and RS1 have been connected together to efficiently make use of available connections. By connecting these together the optical transmit and receive signals operate at the same rate. They both have a 0 ohm resistor option on each of the SFP+ connectors which can be depopulated as required.

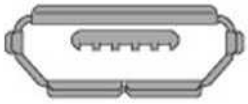
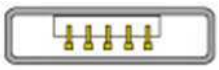
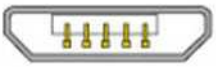
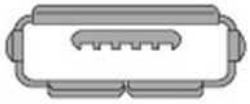
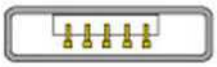
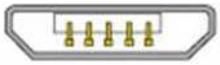
Table 6-13 RX_LOS, TX_FAULT and RS Pin Assignment

SFP Connector	Signal Name	Description	FPGA Bank	Pin
1 (J21)	SFP_1_RX_L/TX_FA_FPGA_OD	Selected RX_LOS or TX_FAULT signal	64	AD18
	SFP_1_RS_FPGA	RS optical transmit and receive signaling rate	64	AM16
2 (J22)	SFP_2_RX_L/TX_FA_FPGA_OD	Selected RX_LOS or TX_FAULT signal	64	AN16
	SFP_2_RS_FPGA	RS optical transmit and receive signaling rate	64	AU20
3 (J25)	SFP_3_RX_L/TX_FA_FPGA_OD	Selected RX_LOS or TX_FAULT signal	65	AE15
	SFP_3_RS_FPGA	RS optical transmit and receive signaling rate	65	AL15
4 (J26)	SFP_4_RX_L/TX_FA_FPGA_OD	Selected RX_LOS or TX_FAULT signal	65	AM15
	SFP_4_RS_FPGA	RS optical transmit and receive signaling rate	65	AW15

6.7. USB to UART Controller

The TB-KU-xxx-ACDC8K features a Silicon Labs CP2103 USB to UART interface to communicate with a PC. This module creates a virtual COM port on the computer to allow the user to connect through standard USB. The USB interface on this card is Micro USB **Type AB** which mates with either Micro-A or Micro-B cables.

Table 6-14 Micro-USB Type B and AB Compatibility

Receptacle	Plug
Micro-B 	Micro-A  
	Micro-B  
Micro-AB 	Micro-A  
	Micro-B  

The UART signals are connected to the FPGA's single-ended pins on Bank 24. Provided below is a table indicating where the signals connect. Both the UART transmit and receive data signals are connected as well as flow control signals. Using the PC's virtual COM port drivers, there are different supported baud rates that are compatible with this controller and can be set during the COM port configuration.

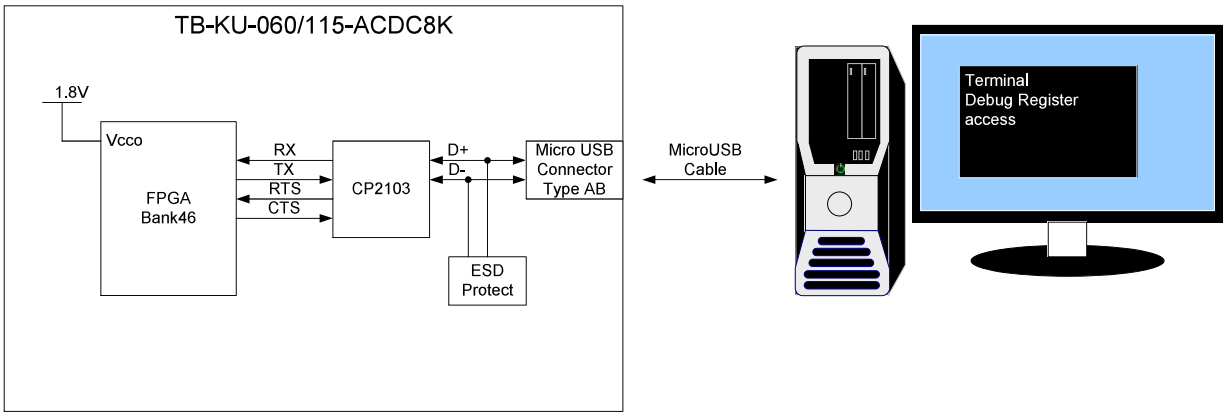


Figure 6-13 USB UART Interface

Table 6-15 UART Interface Pin Assignment

FPGA Bank	USB_UART_TX	USB_UART_RX	USB_UART_RTS_N	USB_UART_CTS_N
24	AG30	AL33	AN29	AT32

6.8. Battery

This board contains an 11.6 mm coin cell battery connected to the VBATT pin which serves as a battery backup supply for the FPGA's internal volatile memory that stores the key for AES decryption. More information is available in Xilinx's UltraScale configuration UG570 document. It is possible to monitor the battery's voltage through test point TP68.

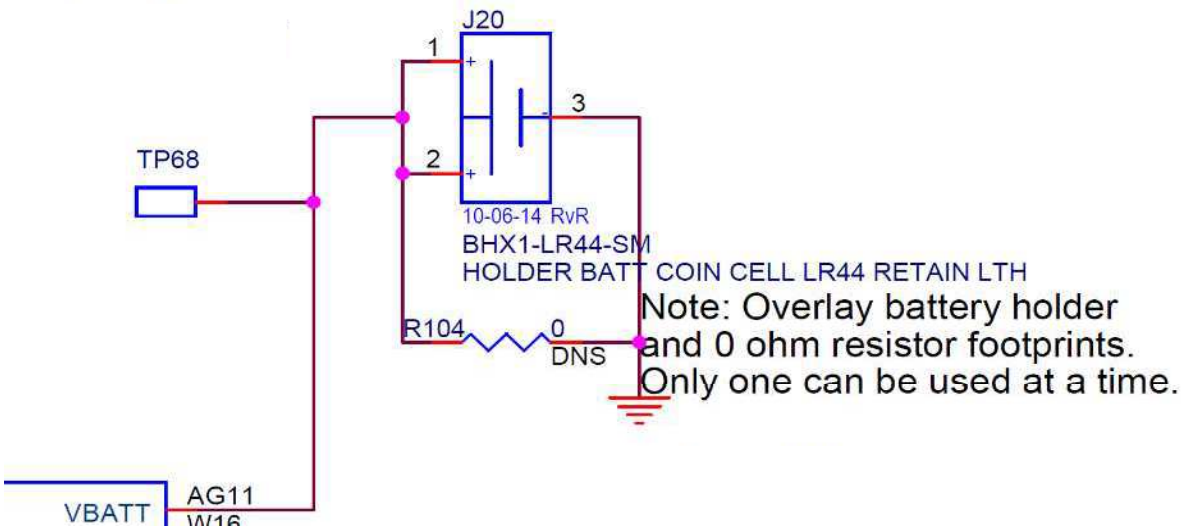


Figure 6-14 Battery Circuit

6.9. Dual Quad (x8) SPI Flash

This board has a 256Mbit dual quad SPI flash (x8) memory for FPGA configuration purposes. Please refer to Xilinx's UltraScale configuration UG570 document on Master SPI Dual Quad (x8) for more information. The multi-I/O SPI Flash memory is used to provide non-volatile code and data storage. Access to programming the FPGA Flash has been provided to the Xilinx core and can be programmed through GPIO pins (UserIO shown on figure below).

Devices: N25Q256A11EF840E (Micron) 256Mbit, x1/x2/x4/x8 support
Devices Data Rate: 108 MHz (maximum) clock frequency in single transfer rate mode

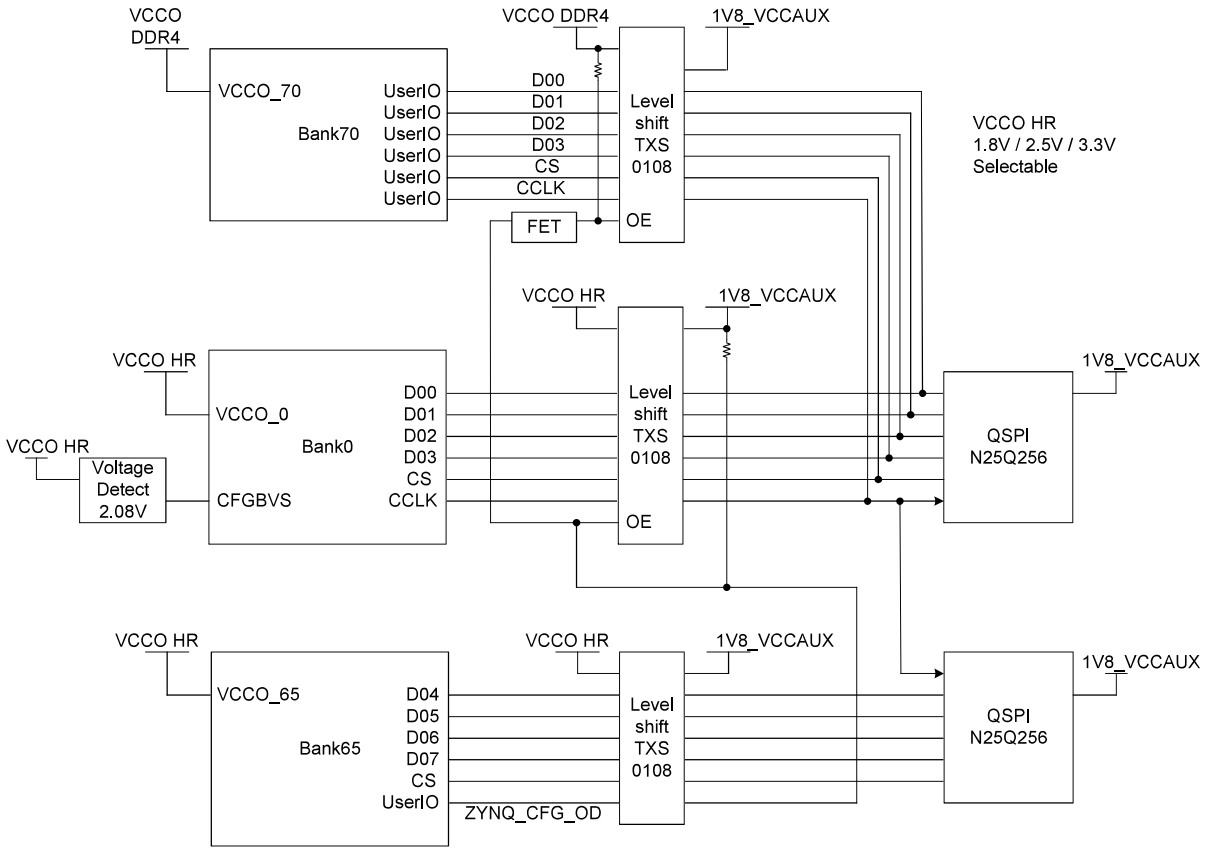


Figure 6-15 FPGA SPI Flash Configuration Structure

In order to pre-configure the flash using the Zynq's interface via JTAG, it is necessary that the user drives signal SPIFLASH_ZYNQ_CFG_OD "low" prior to programming using JTAG.
SPIFLASH_ZYNQ_CFG_OD is "high" (default): Bank 0 used for configuration.
SPIFLASH_ZYNQ_CFG_OD is "low": Zynq UserIO programs flash through JTAG.

Table 6-16 SPI Flash Memory Pin Assignment

Signal Name	FPGA Bank	FPGA Pin
Primary Flash		
SPIFLASH_HR_1_CS_N	0	AB9
SPIFLASH_HR_1_IO_0	0	AE11
SPIFLASH_HR_1_IO_1	0	AD10
SPIFLASH_HR_1_IO_2	0	AC9
SPIFLASH_HR_1_IO_3	0	AD9
CLK_FPGA_CCLK	0	AC11
Secondary Flash		
SPIFLASH_HR_2_CS_N	65	AW16
SPIFLASH_HR_2_IO_0	65	AF14
SPIFLASH_HR_2_IO_1	65	AG14
SPIFLASH_HR_2_IO_2	65	AE13
SPIFLASH_HR_2_IO_3	65	AF13
CLK_FPGA_CCLK	0	AC11
Xilinx Core User IO		
SPIFLASH_ZYNQ_CS_N	47	P29
SPIFLASH_ZYNQ_IO_0	47	N29
SPIFLASH_ZYNQ_IO_1	47	L32
SPIFLASH_ZYNQ_IO_2	47	L33
SPIFLASH_ZYNQ_IO_3	47	R30
SPIFLASH_ZYNQ_CFG_OD	65	AV16
CLK_ZYNQ_CONFIG_CCLK	47	P30

6.10. JTAG and Pmod Interface

6.10.1. JTAG Connector

The TB-KU-xxx-ACDC8K provides a JTAG interface that follows the Xilinx 14-pin JTAG standard.

Table 6-17 Xilinx 14-pin JTAG Pinout

Pin	Xilinx 14-pin JTAG		Pin
1	GND	VREF	2
3	GND	TMS	4
5	GND	TCK	6
7	GND	TDO	8
9	GND	TDI	10
11	GND	NC	12
13	GND	NC	14

Table 6-18 FPGA Bank 0 JTAG Pin Assignment

Signal Name	TMS	TCK	TDO	TDI
FPGA Bank 0 Pin	W11	AA11	T10	U11

6.10.2. Pmod Interface

Digilent's Pmod standard for system boards that provide I2C connectors is to use a male header. This board features a 0.1" straight 2x6 male header for Pmod connections which includes 3.3V and ground signals and eight I/O.

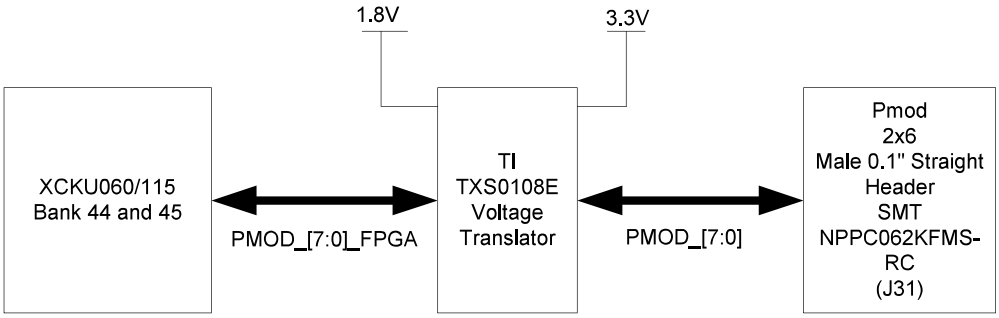


Figure 6-16 Pmod Connection

Table 6-19 Pmod Pin Assignment

Pmod Pin	Signal Name	FPGA Pin	Pmod Pin	Signal Name	FPGA Pin
1	PMOD_0	AU24	7	PMOD_4	AT25
2	PMOD_1	AP20	8	PMOD_5	AP26
3	PMOD_2	AJ23	9	PMOD_6	AK26
4	PMOD_3	AH21	10	PMOD_7	AH27
5	GND	GND	11	GND	GND
6	VCC	3V3 <-> 1V8_FMC	12	VCC	3V3 <-> 1V8_FMC

6.11. General Purpose LEDs

The TB-KU-xxx-ACDC8K has 16 user programmable LEDs. There are 8 green colored LEDs and 8 red ones. The FPGA can be programmed to output a logic “high” to turn on a LED and a logic “low” to turn it off.

Table 6-20 Uncommitted LEDs Pin Assignment

LED RefDes	Color	Signal Name	FPGA Bank	FPGA Pin
D12	Green	GRN_LED_1	67	D20
D13	Green	GRN_LED_5	67	H16
D14	Red	RED_LED_1	66	H13
D15	Red	RED_LED_5	66	G12
D16	Green	GRN_LED_2	67	N19
D17	Green	GRN_LED_6	67	K17
D18	Red	RED_LED_2	66	A12
D19	Red	RED_LED_6	66	H12
D20	Green	GRN_LED_3	47	M32
D21	Green	GRN_LED_7	66	E15
D22	Red	RED_LED_3	67	R18
D23	Red	RED_LED_7	67	M16
D24	Green	GRN_LED_4	66	C16
D25	Green	GRN_LED_8	67	L17
D26	Red	RED_LED_4	67	R17
D27	Red	RED_LED_8	66	N13

Note:
Please set drive and iostandard as follows.

```
## led
set_property DRIVE           8          [get_ports led]
set_property IOSTANDARD      LVCMOS12   [get_ports led]
set_property PACKAGE_PIN     D20        [get_ports led[ 0]]    ;# GRN_LED_1
set_property PACKAGE_PIN     N19        [get_ports led[ 1]]    ;# GRN_LED_2
set_property PACKAGE_PIN     M32        [get_ports led[ 2]]    ;# GRN_LED_3
set_property PACKAGE_PIN     C16        [get_ports led[ 3]]    ;# GRN_LED_4
set_property PACKAGE_PIN     H16        [get_ports led[ 4]]    ;# GRN_LED_5
set_property PACKAGE_PIN     K17        [get_ports led[ 5]]    ;# GRN_LED_6
set_property PACKAGE_PIN     E15        [get_ports led[ 6]]    ;# GRN_LED_7
set_property PACKAGE_PIN     L17        [get_ports led[ 7]]    ;# GRN_LED_8
set_property PACKAGE_PIN     H13        [get_ports led[ 8]]    ;# RED_LED_1
set_property PACKAGE_PIN     A12        [get_ports led[ 9]]    ;# RED_LED_2
set_property PACKAGE_PIN     R18        [get_ports led[10]]    ;# RED_LED_3
set_property PACKAGE_PIN     R17        [get_ports led[11]]    ;# RED_LED_4
set_property PACKAGE_PIN     G12        [get_ports led[12]]    ;# RED_LED_5
set_property PACKAGE_PIN     H12        [get_ports led[13]]    ;# RED_LED_6
set_property PACKAGE_PIN     M16        [get_ports led[14]]    ;# RED_LED_7
set_property PACKAGE_PIN     N13        [get_ports led[15]]    ;# RED_LED_8
```

6.12. General Purpose Switches

6.12.1. DIP Switches

This board is equipped of 4 Copal Electronics CHS-04TA SPST 4-positions DIP switches. Slide in the ON position for a logic “Low”.

Table 6-21 DIP Switches Pin Assignment

Switch RefDes	Signal Name	FPGA Bank	FPGA Pin
SW17	SWITCH_1	67	N18
	SWITCH_2	67	T18
	SWITCH_3	67	T17
	SWITCH_4	67	N17
SW18	SWITCH_5	67	N16
	SWITCH_6	67	R16
	SWITCH_7	67	P16
	SWITCH_8	67	P19
SW19	SWITCH_9	67	P18
	SWITCH_10	68	A23
	SWITCH_11	68	C24
	SWITCH_12	68	F22
SW20	SWITCH_13	68	H22
	SWITCH_14	68	L22
	SWITCH_15	68	J21
	SWITCH_16	68	R23

6.12.2. Push Switches

The board also features 8 C&K Components KMR211GLFS push buttons. Pressing the button sends logic “low”, in the default position they are set to logic “high”.

Table 6-22 Push-button Switches Pin Assignment

Push-button RefDes	Signal Name	FPGA Bank	FPGA Pin
SW7	PUSHBUTTON_1	46	F39
SW8	PUSHBUTTON_5	46	A33
SW9	PUSHBUTTON_6	47	B29
SW11	PUSHBUTTON_2	46	D36
SW12	PUSHBUTTON_3	46	F35
SW13	PUSHBUTTON_7	46	J36
SW15	PUSHBUTTON_4	46	F34
SW16	PUSHBUTTON_8	46	E38

6.12.3. Jumper Switches

Lastly, 8 jumper switches were conveniently placed at the user's disposal available as a standard 16-pin header. It provides uncommitted GPOs that connect to the board's FPGA.

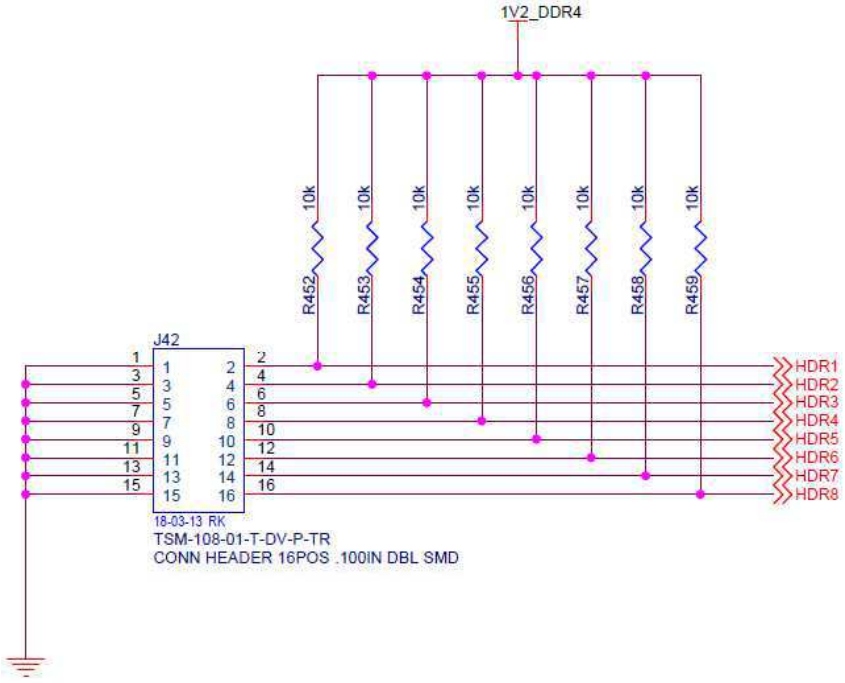


Figure 6-17 Jumper Switches Structure

The signals output logic "high" by default (when there is no jumper connected). Connect an odd-numbered pin to the even-numbered pin across from it to output a logic "low" to the FPGA. The header's reference designator on the board is **J42**.

Table 6-23 Jumper Switches Pin Assignment

Jumper Option	Signal Name	FPGA Bank	FPGA Pin
1-2	HDR1	47	J29
3-4	HDR2	47	H33
5-6	HDR3	47	J30
7-8	HDR4	47	J31
9-10	HDR5	47	M30
11-12	HDR6	47	L30
13-14	HDR7	47	M29
15-16	HDR8	47	L29

7. Appendix

7.1. Default Settings

Following Figure shows a setting Jumper and DIP switches.

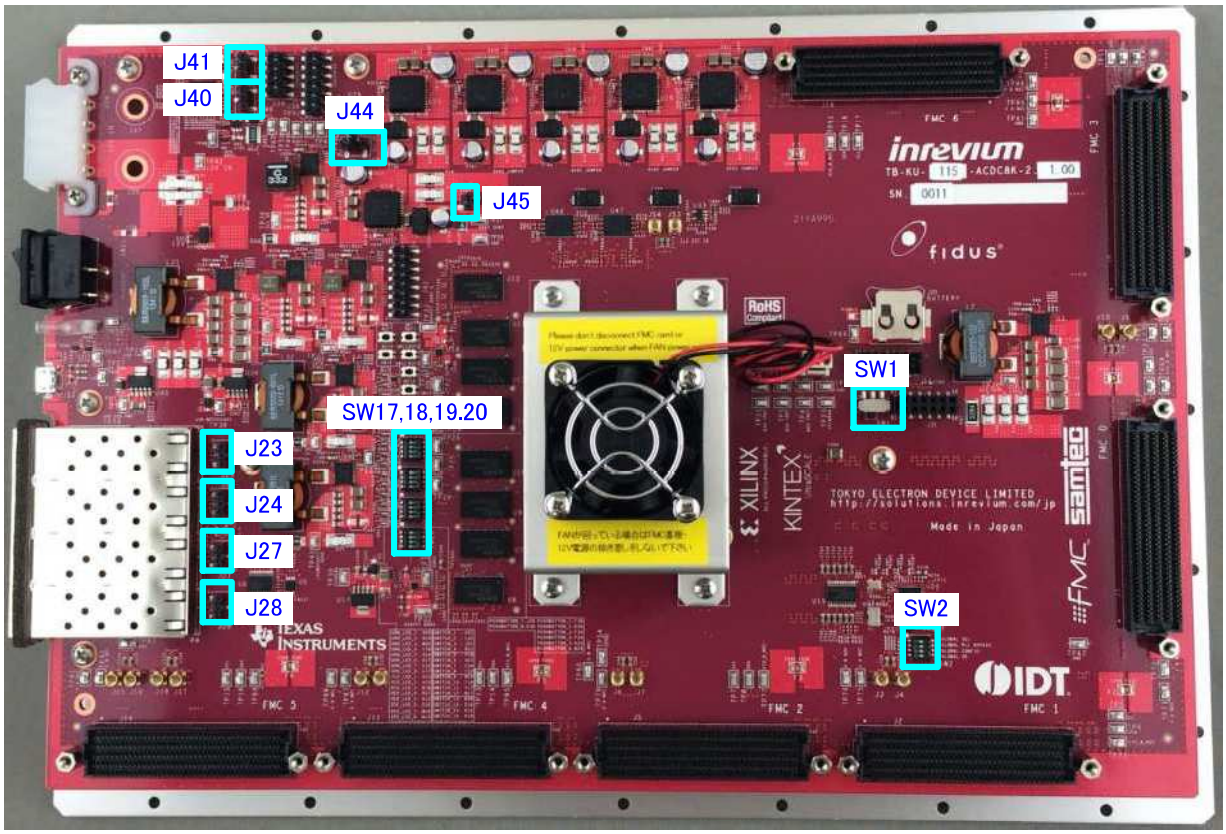


Figure 7-1 Jumper and Switch location (Component Side)

Table 7-1 Default Settings

No.	Silk No.	Initial Setting	Function
1	SW1	1-2	POR Override (**ON**/OFF)
2	SW2	ALL OFF	Video Clock setting
3	SW17,18,19,20	ALL OFF	User DIP Switches setting
4	J44	Open	FMC_HR_Bank voltage(**1.8V** / 2.5V / 3.3V)
5	J40	Open	PMBUS_ADDR0(GND_90.9K,1% / GND_41.2K,1% / **No Supply**)
6	J41	Open	PMBUS_ADDR1(GND_90.9K,1% / GND_41.2K,1% / **No Supply**)
7	J23	Open	SFP 1 (RX_LOS / TX_FAULT / **No Supply**)
8	J24	Open	SFP 2 (RX_LOS / TX_FAULT / **No Supply**)
9	J27	Open	SFP 3 (RX_LOS / TX_FAULT / **No Supply**)
10	J28	Open	SFP 4 (RX_LOS / TX_FAULT / **No Supply**)
11	J45	Open	VCCINT Sense (A jumper must be installed when links removed)

7.2. Power Sequencer Timings

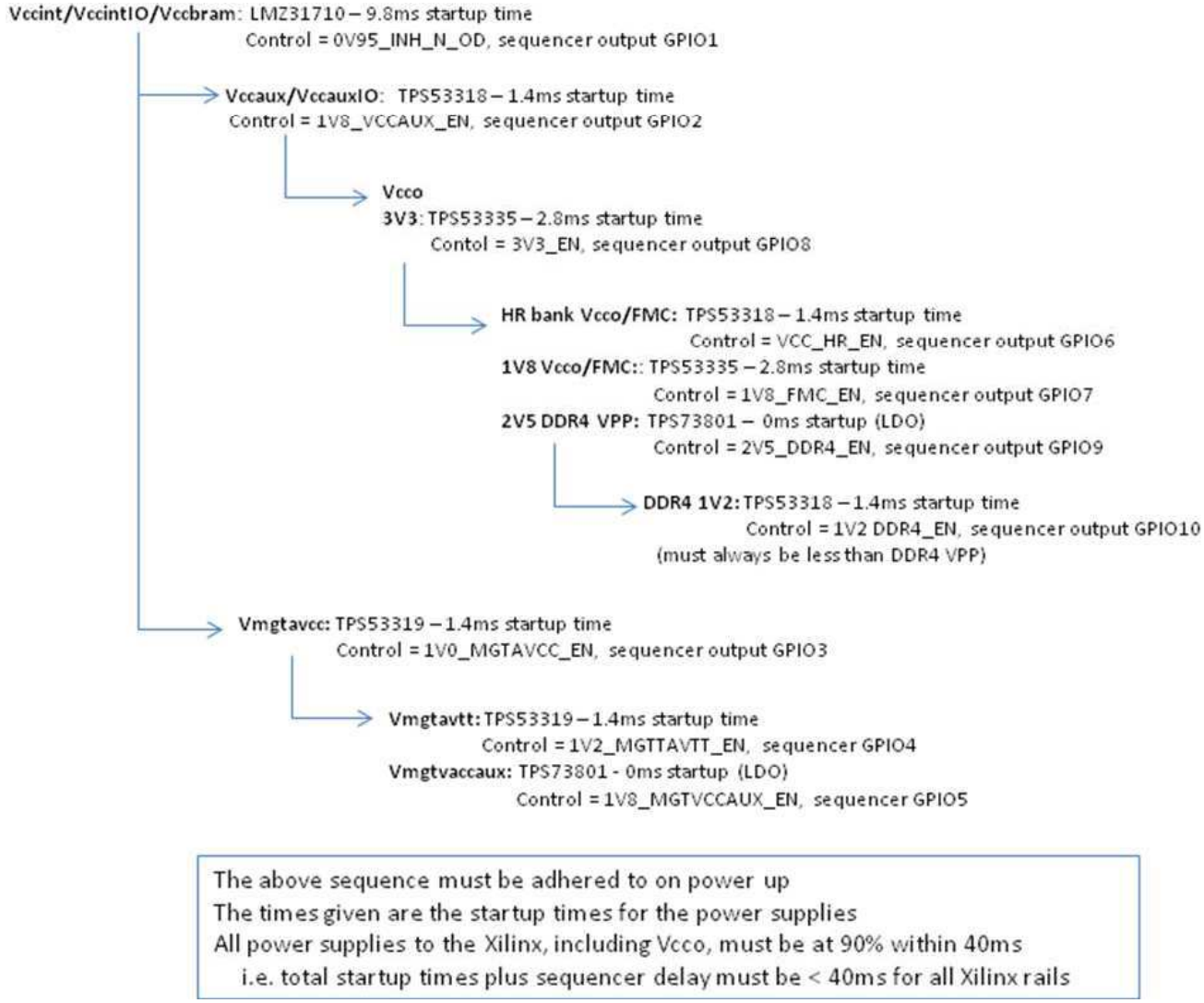


Figure 7-2 Power Sequencer Default Settings

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